Update on CSIC activities on LGAD & 3D sensors

4th AIDA-2020 Annual meeting

St. Anne's College, Oxford, UK

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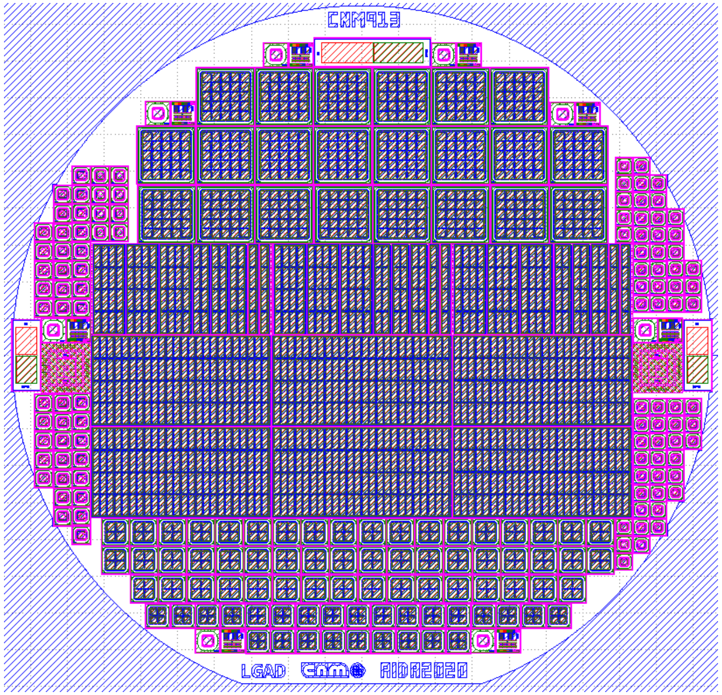
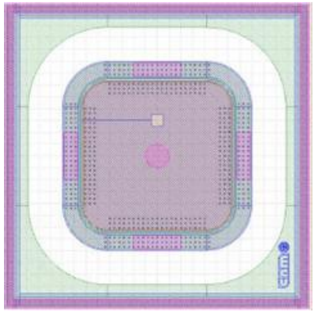
Outline - 1 / Thin LGAD run from IMB-CNM

- Radiation tolerance of thin LGADs (AIDA-2020)
  - Motivation & sample description
  - Electrical characterization: IV & CV
  - Charge collection vs fluence.
  - Slewing rate vs fluence.
- On the high-leakage current issue
  - Identification of the high-leakage current.
  - New manufacturing run with AIDA-2020 layout.

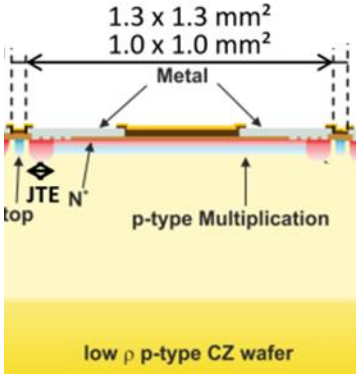
Motivation , Samples & Irradiation points

- Compare the radiation tolerance (protons) of LGAD with **two different active thickness: 50 and 35 μm**.
- Samples form CNM Run#11748 (AIDA-2020 WP7)





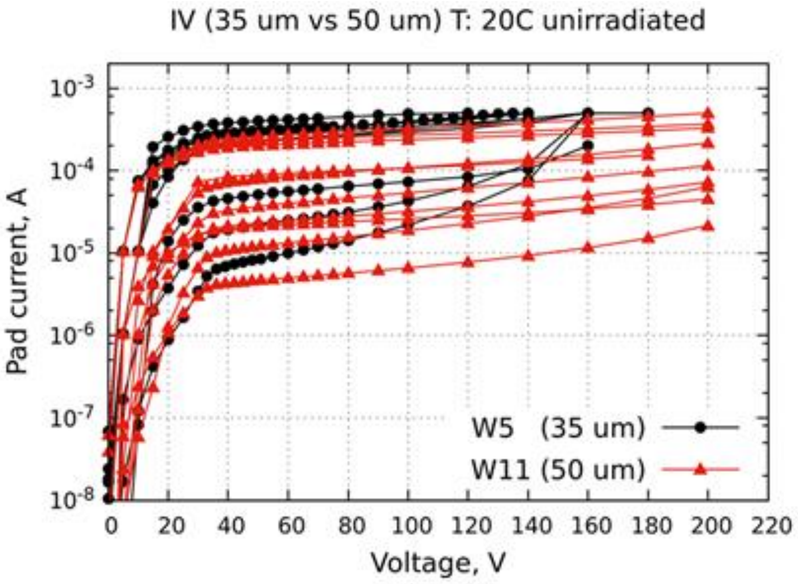
Total area of 2.6x2.6 mm^2
Active area of 1.3x1.3 mm^2
Intermediate gain



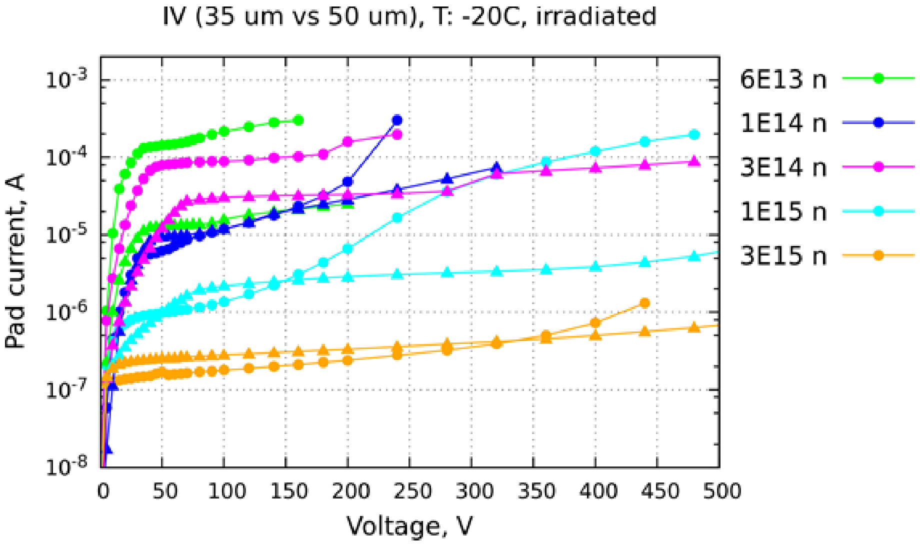
- Irradiated at CERN PS with 24 GeV protons at **5 different fluences.**
  - 6E13 n_{eq}/cm2
  - 1E14 n_{eq}/cm2
  - 3E14 n_{eq}/cm2
  - 1E15 n_{eq}/cm2
  - 3E15 n_{eq}/cm2

Electrical Characterization: IV Curves

- Large reverse current (unexpected).
- The reverse current is suppressed by irradiation.
- Originated at the at diode periphery (see next slides).



BEFORE IRRADIATION



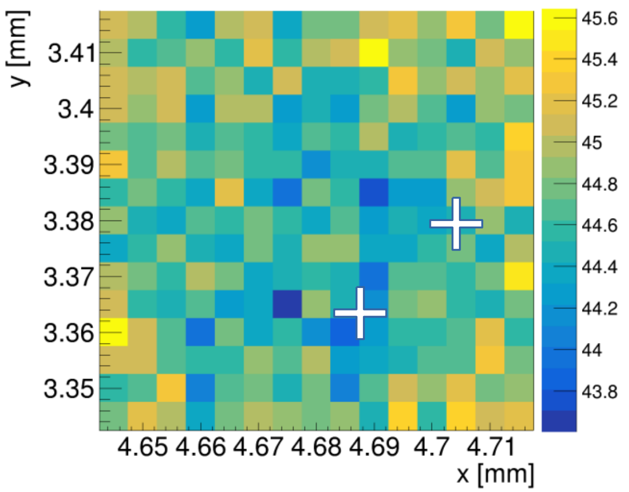
AFTER IRRADIATION

ivan.vila@csic.es, 4th Annual Meeting, Oxford, April 2019

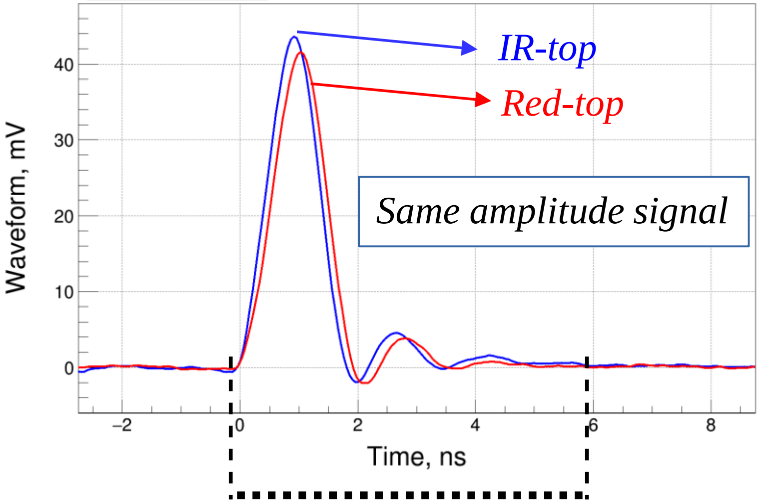
TCT Characterization: Charge Collection Uniformity

- IR laser and red laser
- Top illumination
- Same laser intensity in both cases
- Temperature: -20 C
- Amplifier: CIVIDEC C2, 2 GHz, 40 dB
- Oscilloscope: Agilent DSO 9254, 2.5 GHz, 20 GSa/s
- Averaging of 256.

2D amplitude map, mV

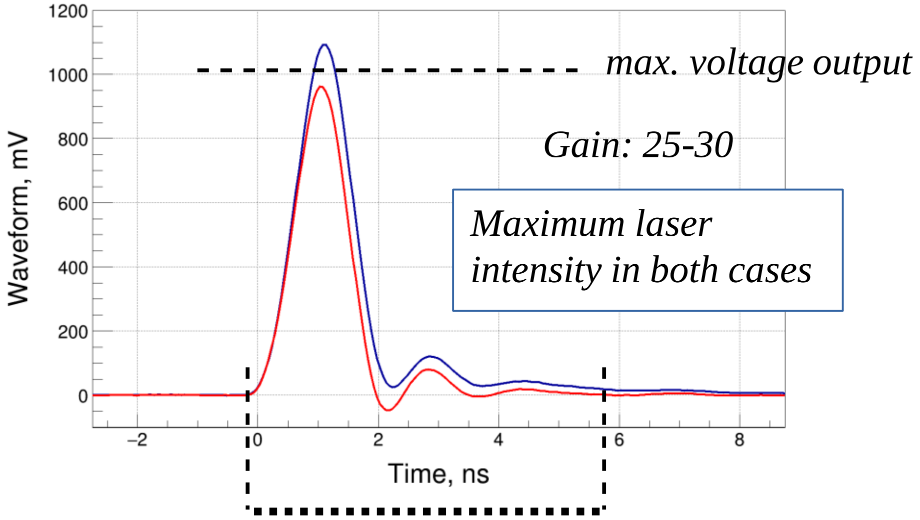


PIN diode W11 (50 um), Voltage: 100 V



Same amplitude signal

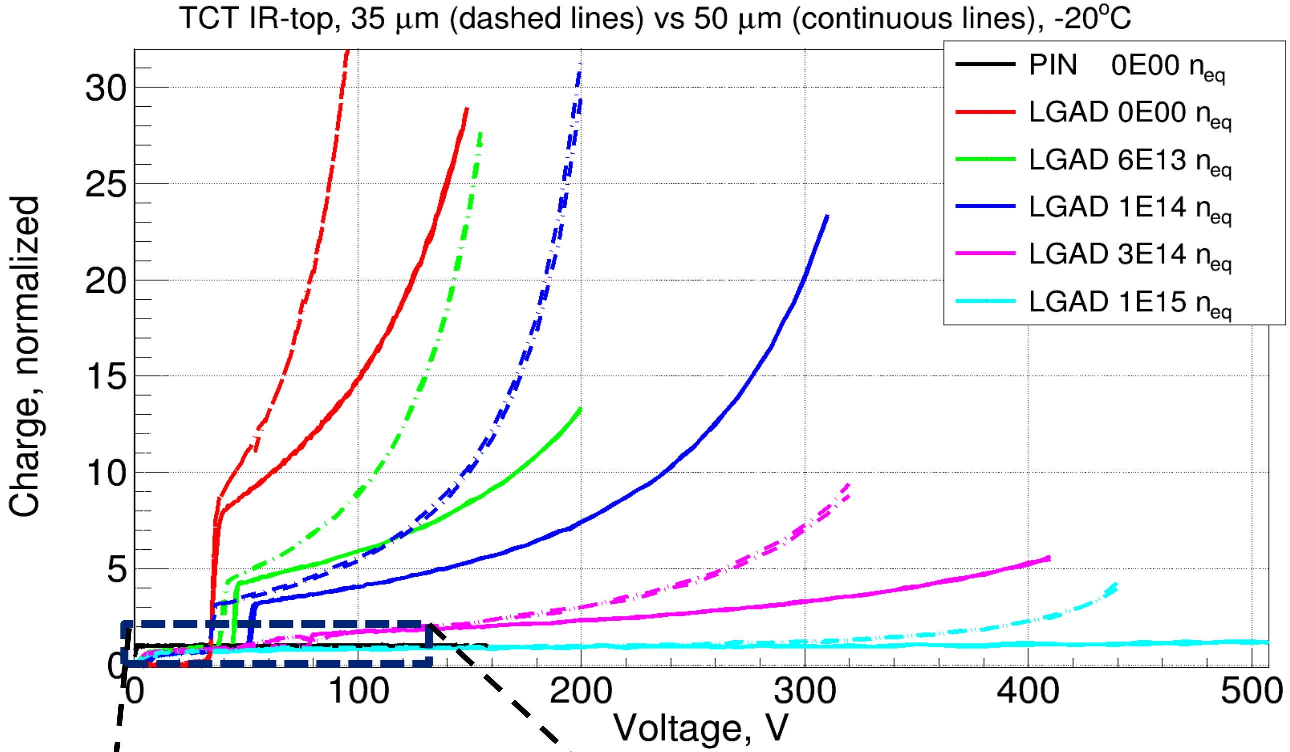
Unirradiated LGAD W11 (50 um), Voltage: 150 V

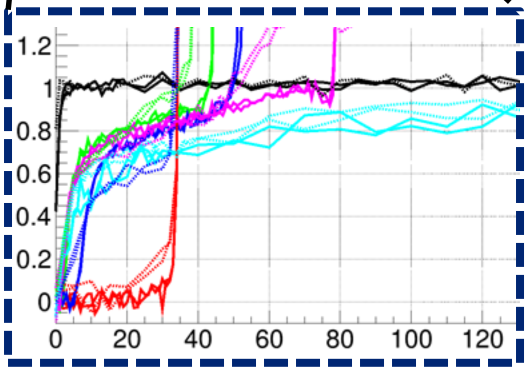


Gain: 25-30

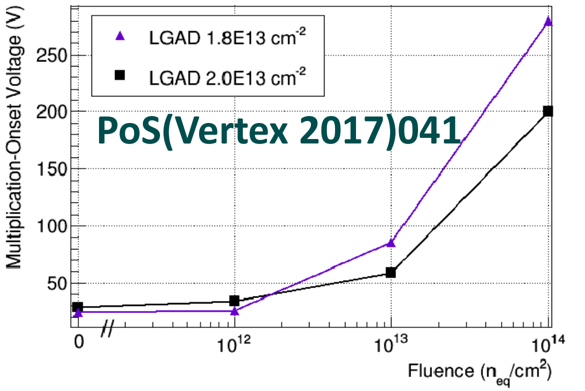
Maximum laser intensity in both cases

TCT Characterization: Charge vs. Bias Voltage





Positive shift of gain offset observed in [S. Otero et al., PoS(Vertex 2017)041] on 300µm thick sensors.

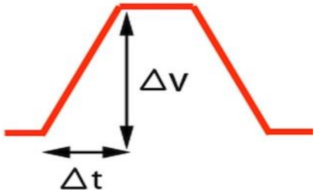


PoS(Vertex 2017)041

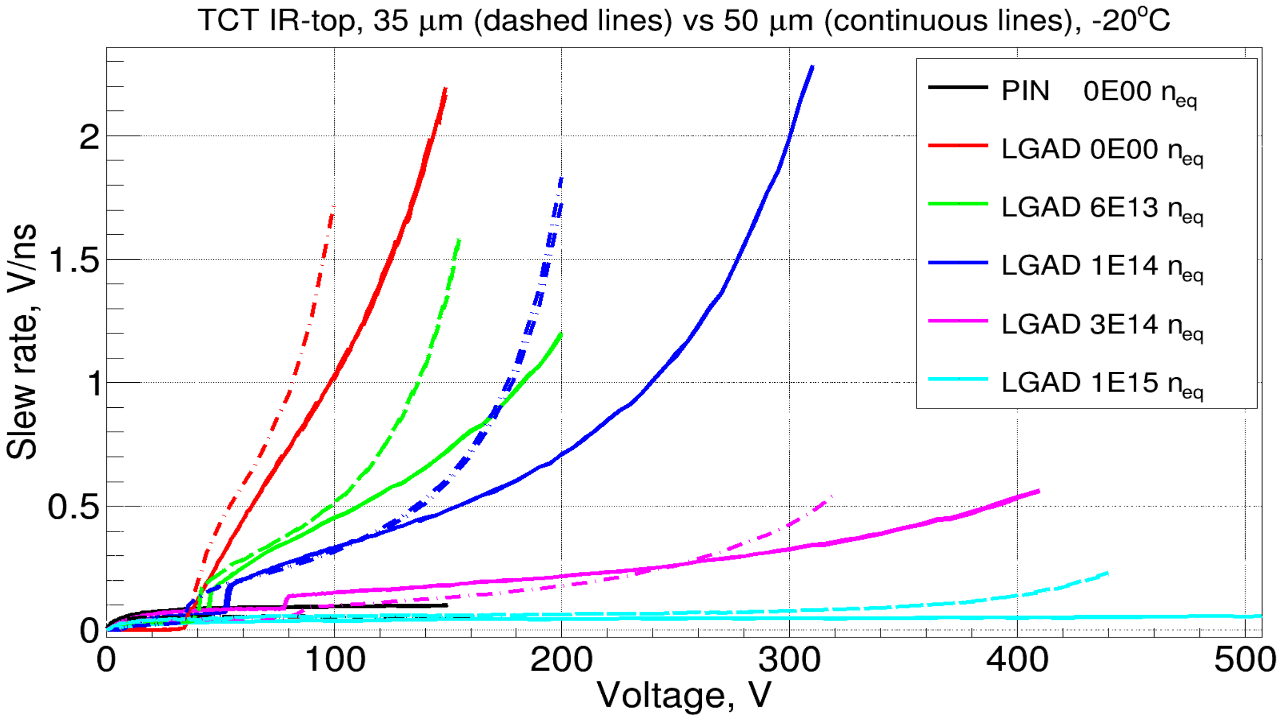
Fluence (n_{eq}/cm^2)	On-set Voltage (Volts)	CV Voltage@maximum
0	30-35	35(CV foot)
6e13	40-45	35
1e14	45-50	40
3e14	75-80	70

First estimation of timing performance: slew rate.

$$\delta_{time} \propto \frac{\delta_{noise}}{\left|\frac{dV}{dt}\right|} \propto \frac{\Delta t}{\Delta V} * \delta_{noise} = \frac{\delta_{noise}}{SR}$$



$$SR = \frac{\Delta V}{\Delta t}$$

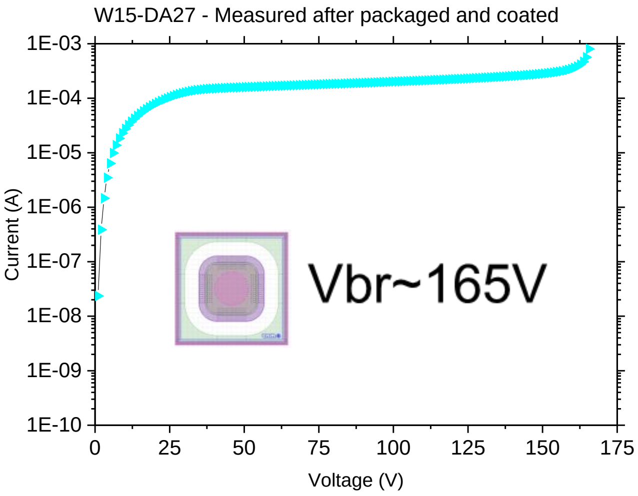


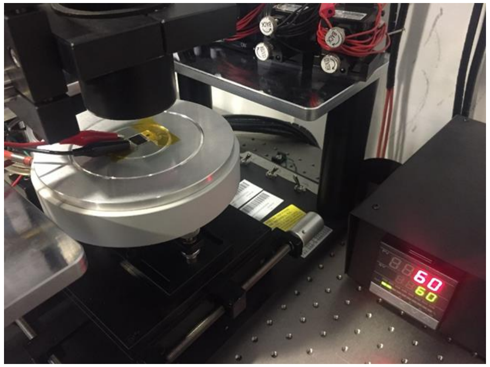
- Slew rate significantly better for the case of thiner LGADs.

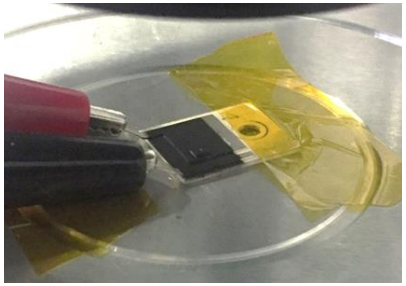
Infrared imaging of single diode LGAD

High leakage current

$I_{leak}>10^{-4}$A @ V>30V







SC5500 thermal camera

G3x Microscopic lens

t_i= 356 µs

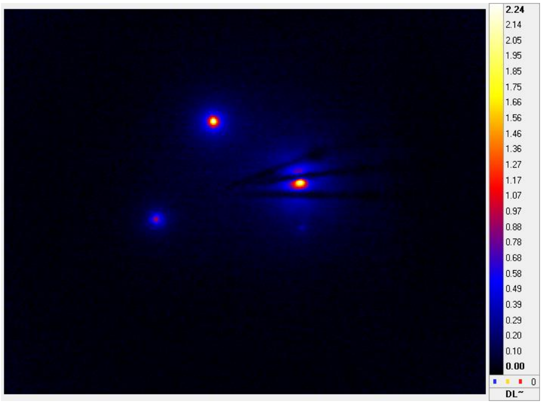
$n_{samples}$=10000

$f_{lock-in}$=101 Hz

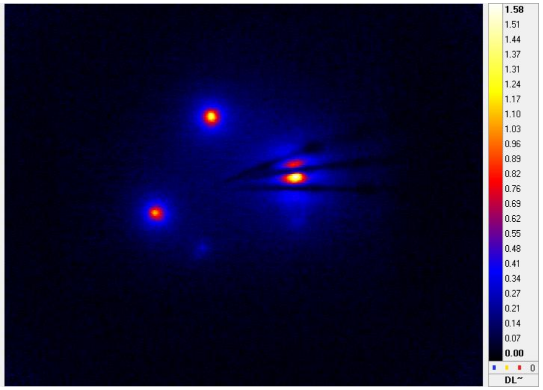
V_{pp}=10V

Leakage current origin: hot spot imaging

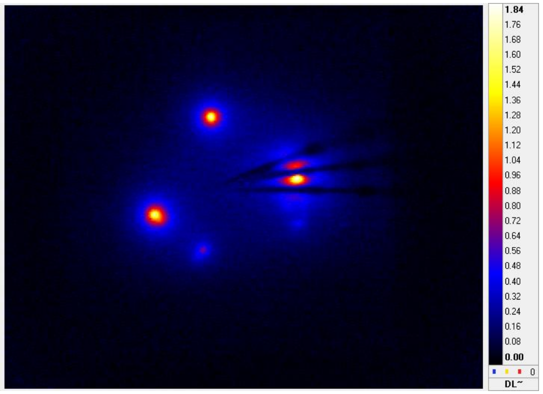
V = 20 V



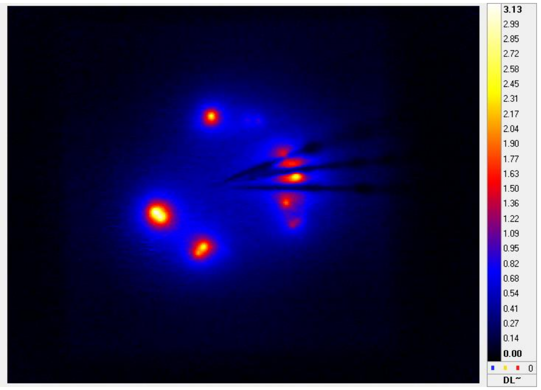
V = 50 V



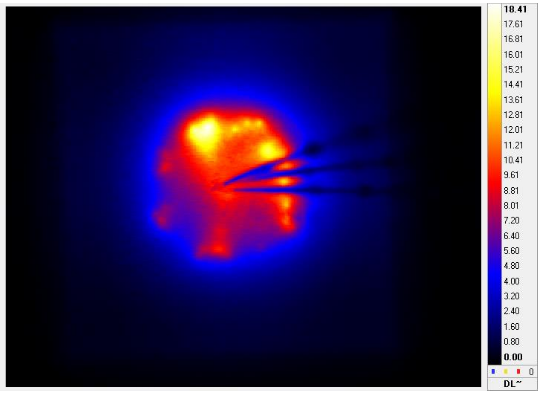
V = 100 V

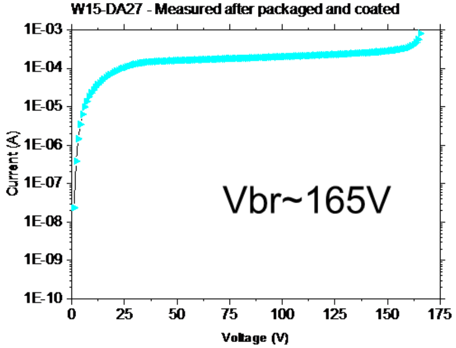


V = 150 V

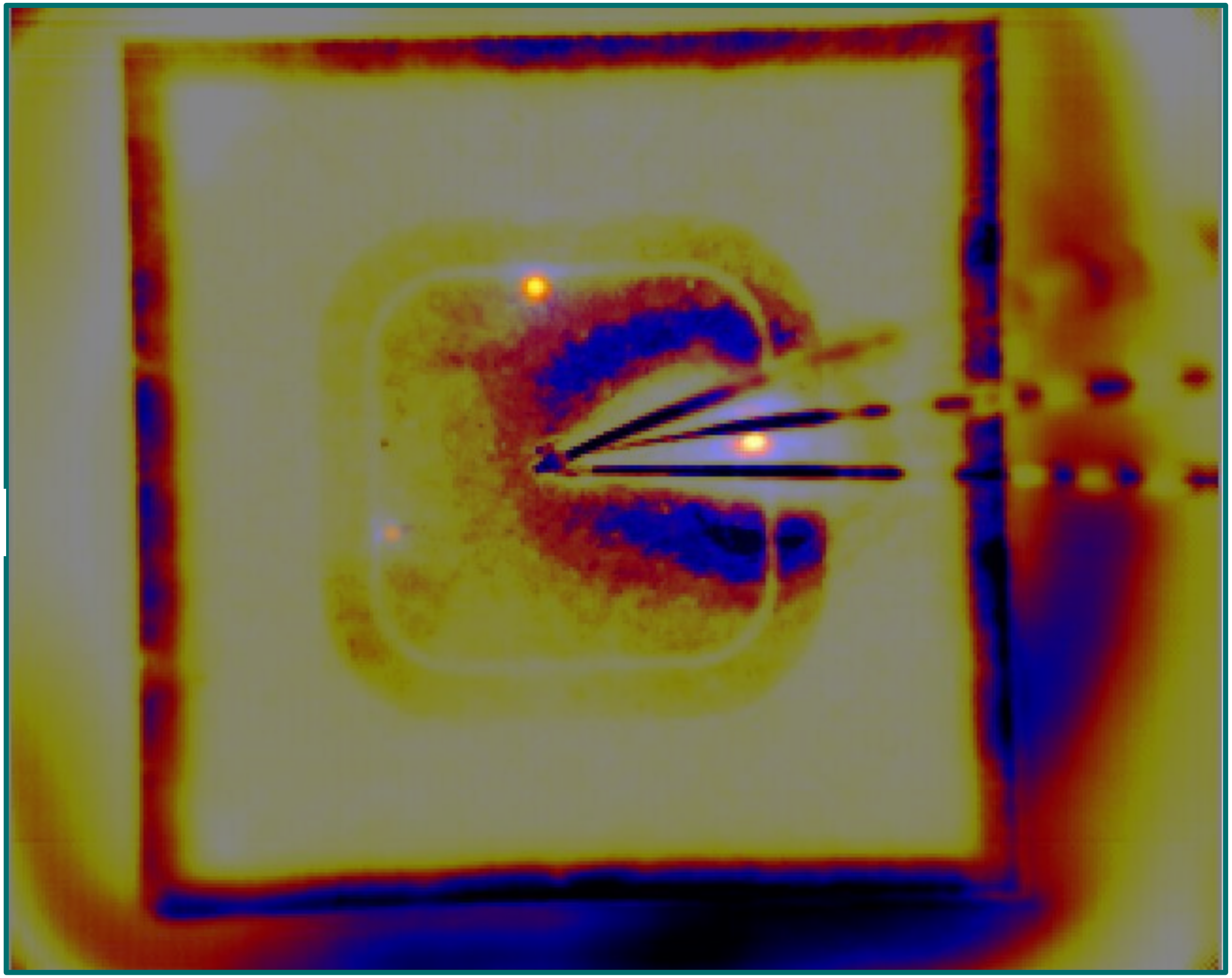


V = 170 V

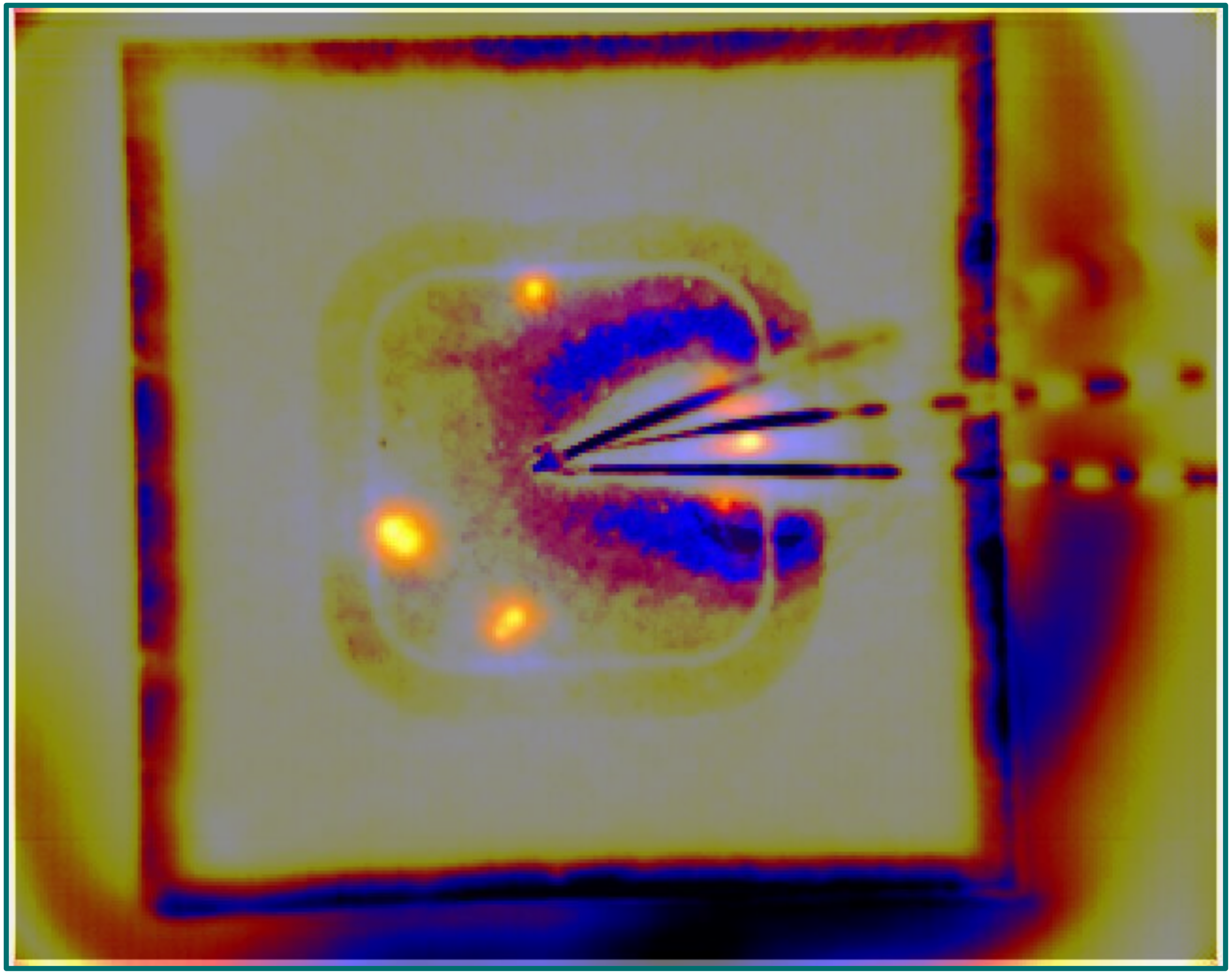




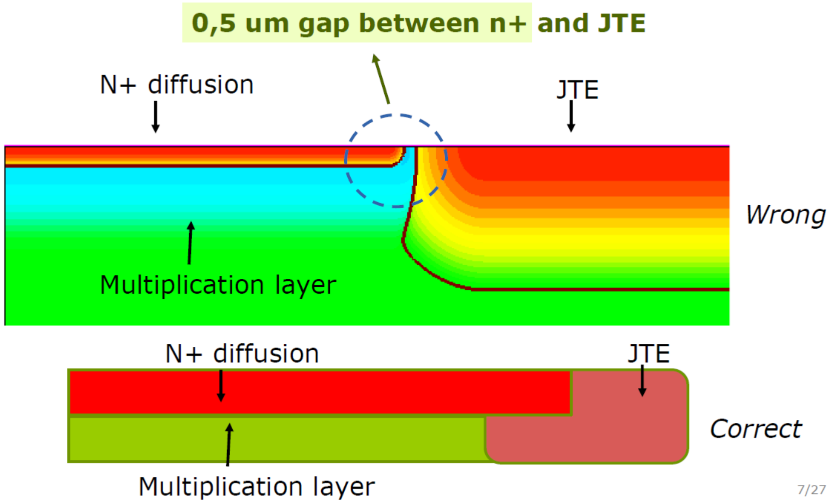
Location of hot spots @ V = 20 V

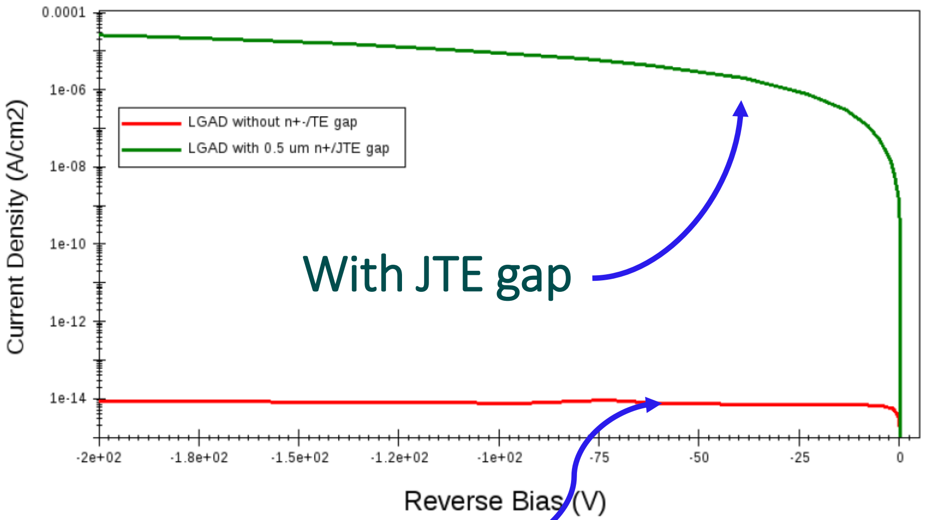


Location of hot spots @ V = 150 V



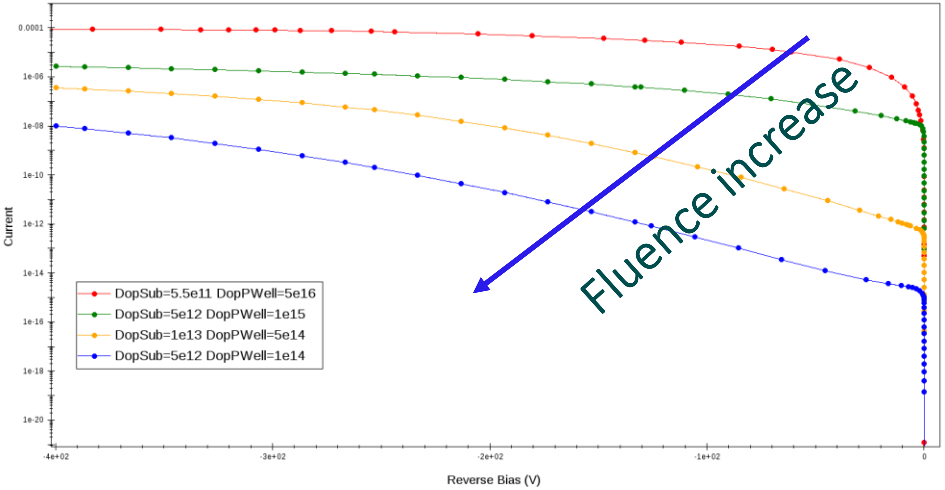
High-leakage current origin: TCAD simulations





With JTE gap

Without JTE gap



Fluence increase

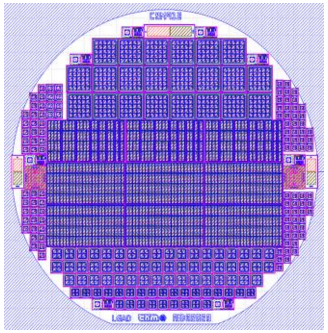
Reverse current suppression by irradiation

Origin of he high reverse current: new LGAD run

Run 12488. LGAD 4 AIDA2020. 2nd Run

New run with corrected periphery design

- ✓ **4” 50+300** µm thick **Si-Si** wafers
- ✓ **4** wafers (lack of wafers is starting to be important !)
- ✓ N^+-Layer **overhang** Multiplication Layer until the JTE end (**old design**)
- ✓ We will use **one implantation dose and energy value** for the multiplication area (Low Dose – Low Energy)
- ✓ We will **not use temporary metal** (to be faster but the option is possible).
- ✓ Run **On-going** (44/83 process steps)
- ✓ The run will end in **April 2019**



Outline - 2 / AIDA-2020 3D run from IMB-CNM

- **AIDA-2020 3D sensors from IMB-CNM.**
  - Technology recall
  - Devices description.
  - QA with temporary metal: manufacturing yield
- **Initial results from characterization of FBK 3D pixel sensors connected to Roc4Sens ROC(*).**
  - **Module assembly & radioactive source testing.**

(*) See **Marco Meschini's** talk results on FBK 3D pixel characterization with RD53A ROC.

AIDA-2020 production (run #11119): Technology

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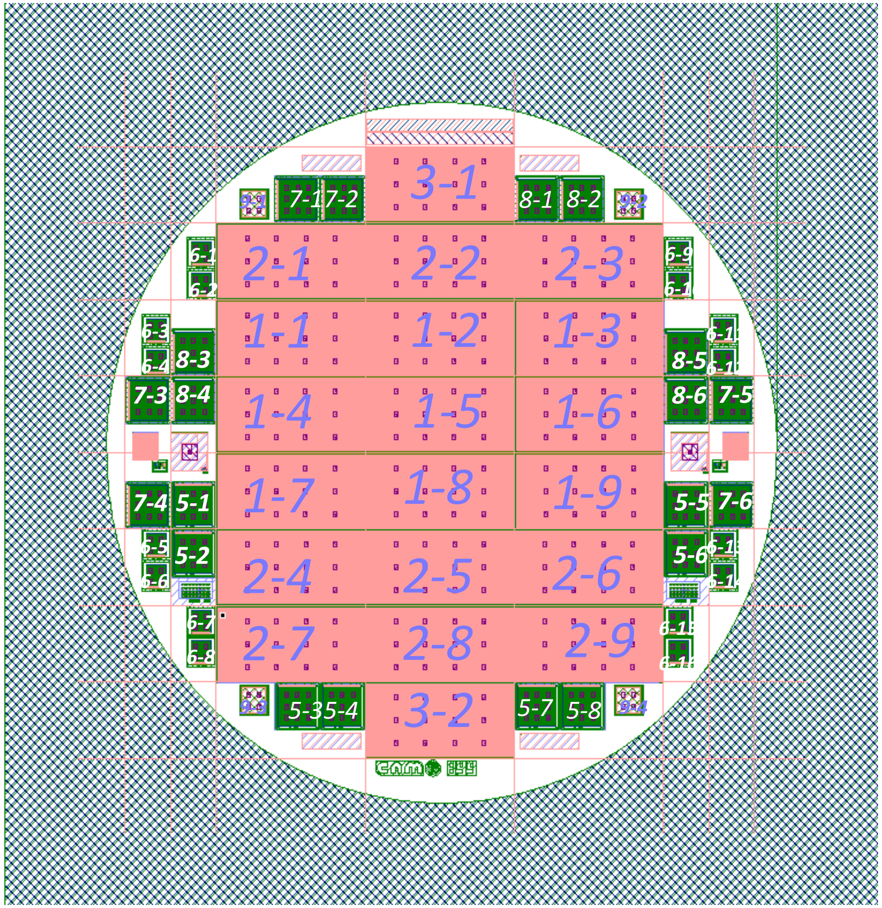
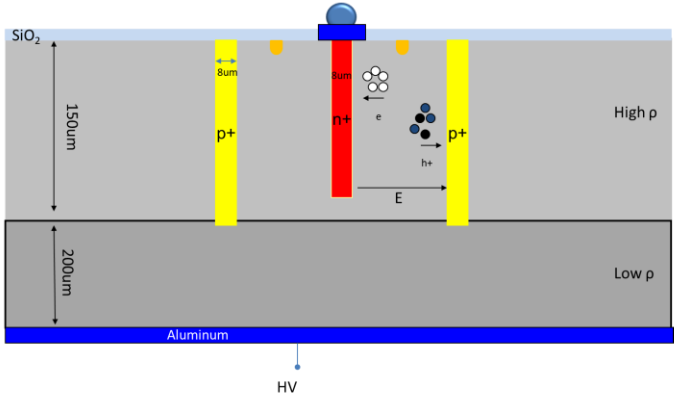
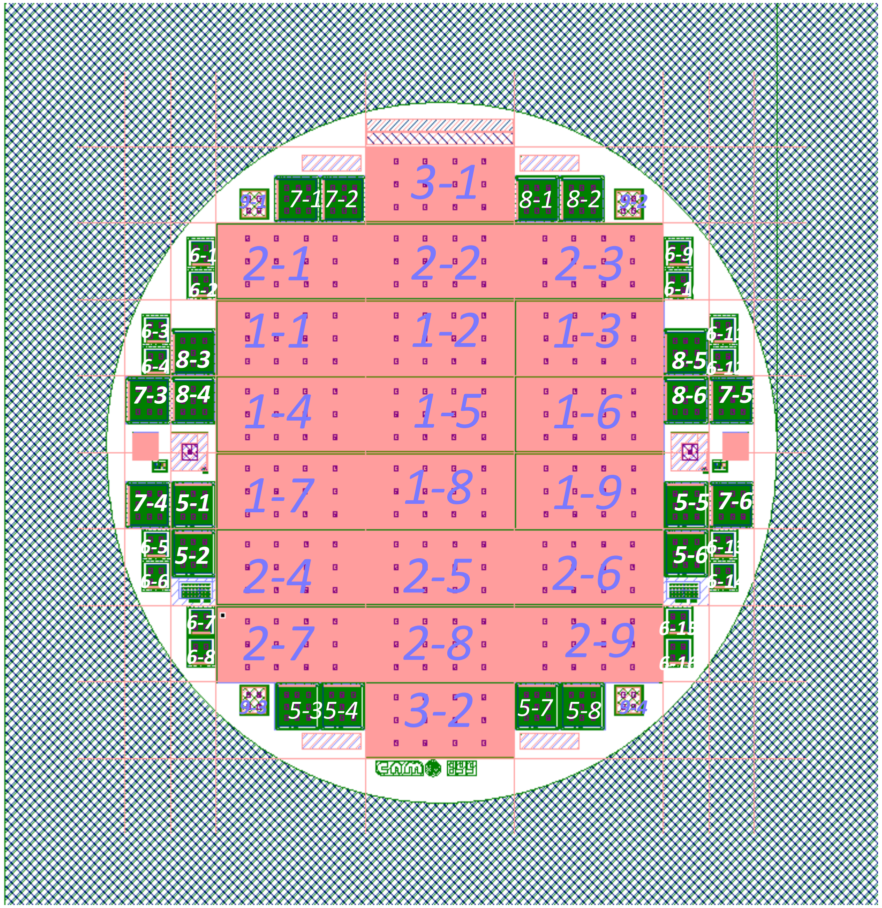




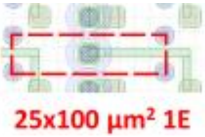
- Run completed in February 2019, seven wafers + one additional wafer for process control.
- Si-on-Si 4” wafers (150 μm + 200 μm)
- Single-sided 3D sensors pixels with RD53A layout.
- Etched columns: 8 um diameter, 120 um length.
- Different pixel cell form-factors and number of electrodes (see next slide)

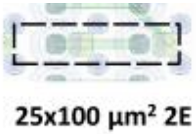
AIDA-2020 production (run #11119): Devices



- RD53A sensors
- 1-x 50x50 um^2 (nine units)
- 2-x 25x100um^2 2E (nine units)
- 3-x 25x100um^2 1E (two units)


50x50 µm²


25x100 µm² 1E


25x100 µm² 2E

– Diodes

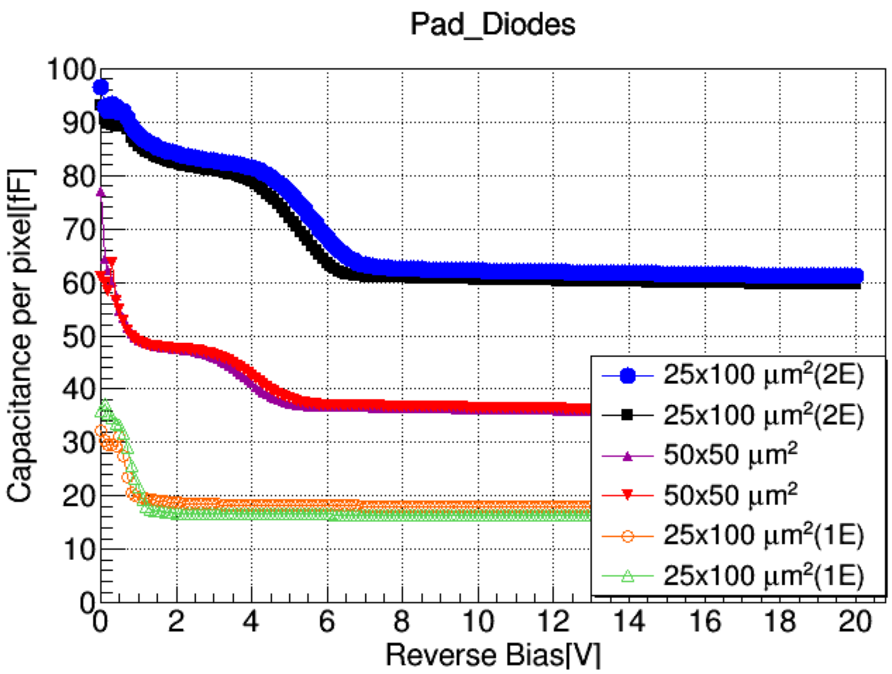
- 5-x 50x50um^2 100x100 electrodes
- 6-x 50x50um^2 50x50 electrodes
- 7-x 25x50um^2 50x50 electrodes
- 8-x 25x100um^2 50x50 electrodes
- 64 test structures 3x3 matrix

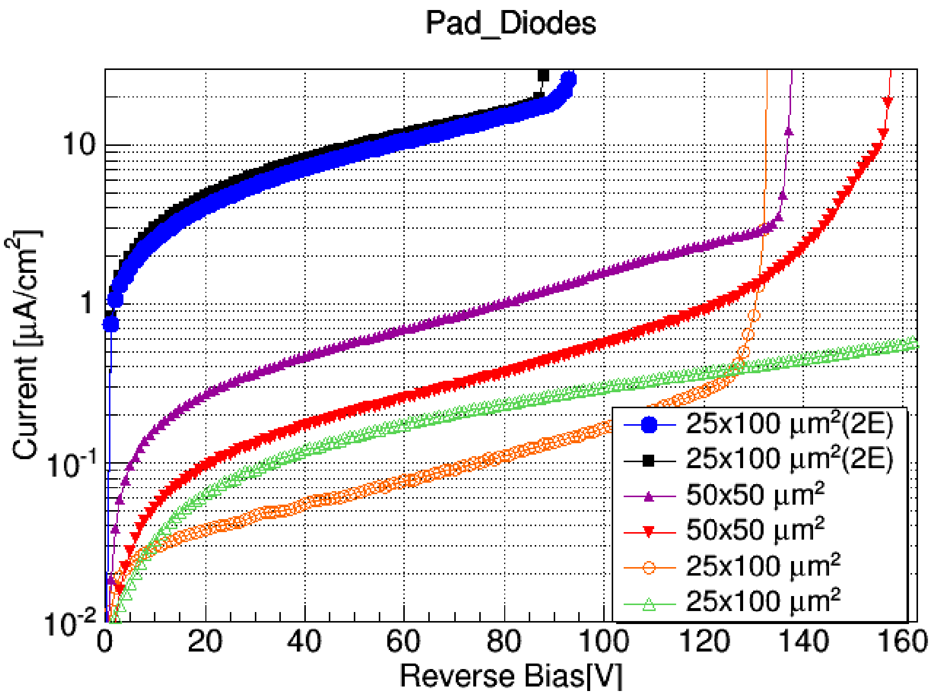
– MOS

- 9-x 3500x3500 um2
- Polysilicon test structures

QA using temporary metal: Diode CV characteristics

- In CV graphs two slopes: the first for the lateral depletion between columns and the second for full depletion.
- Very low capacitance for 25x100 (1E) geometry (below 20fF)
- The leakage current per pixel below 25pA/pixel for 50x50 μm^2 and 25x100 μm^2 (1E) geometries at 80 Volts (x10 for the 2E geometry)

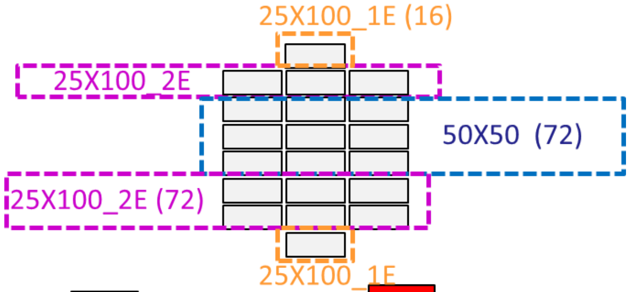




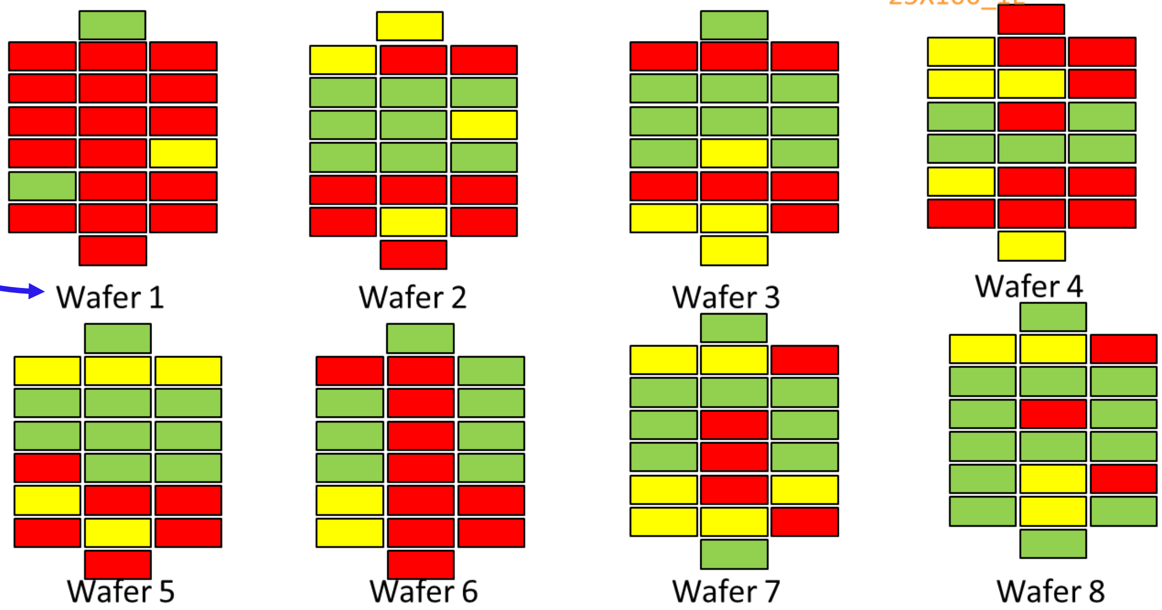
Yield summary

- Pixel cell 50x50: 79% (50/63)
- Pixel cell 25x110(1E): 50% (7/14)
- Pixel cell 25x110(2E): 6% (4/63)

- Green: Vbd > Vdepl + 20V → **50 50x50 μm²** → **8 25x100 μm²_1E**
- Yellow: "soft-BD" → **5 50x50 μm²** → **3 25x100 μm²_1E**
- Red: Vbd < Vdepl + 20V
- Vdepl = 5V from the CV measurements

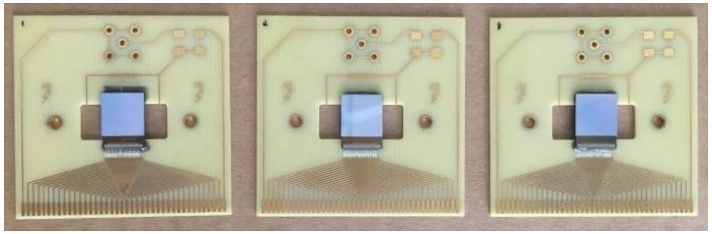


Control wafer (non consider for yield estimates)



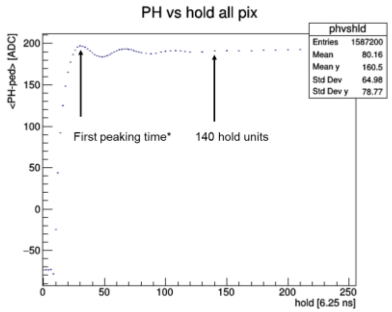
Characterization of 3D FBK pixels connected to R4S

Sensors from AIDA-2020 FBK 3D run, carrier boards from PSI, flip-chipped at IZM, wire bonded at AWGE.

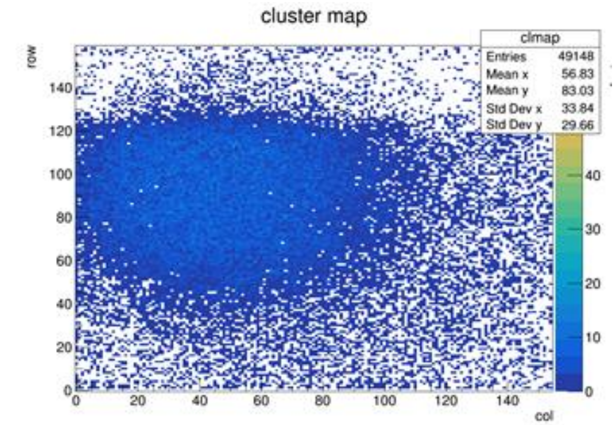


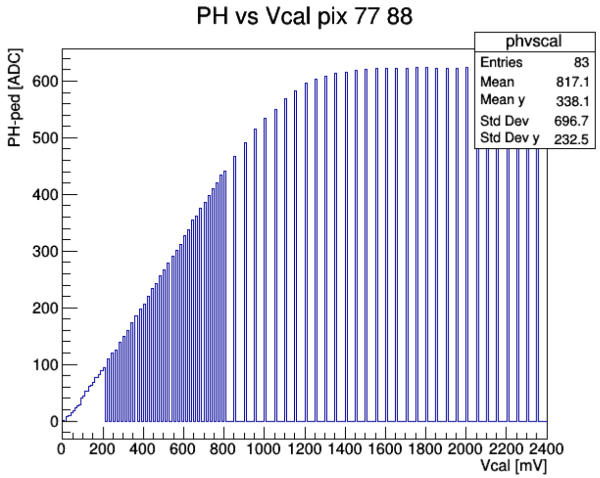
Carrier 1	Wafer 3, Sensor 3, 47	3347 - 50x50	-15V -> -97 uA
Carrier 2	Wafer 3, Sensor 1, 55	3155 - 25x100 1E	-15V -> -0.43 uA
Carrier 3	Wafer 3, Sensor 2, 62	3262 - 25x100 2E	-15V -> -0.31 uA

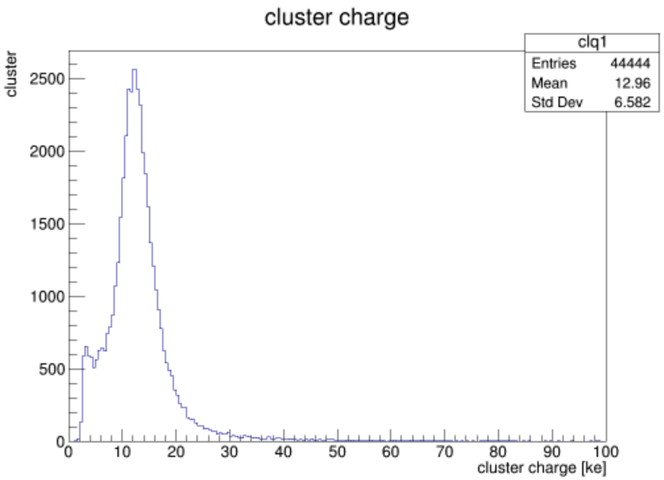
All three form-factor pixel cells working with low reverse current

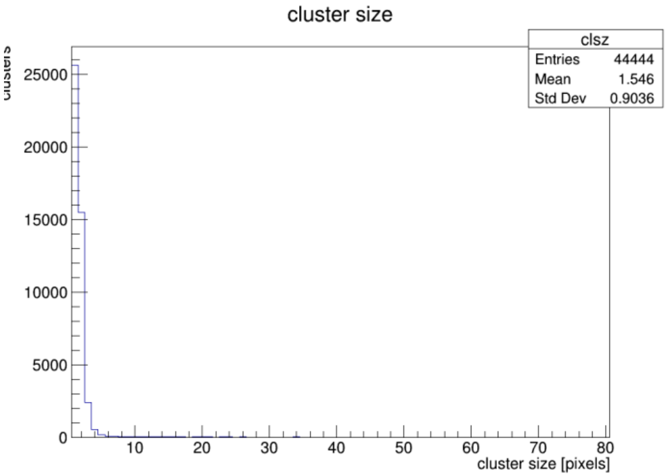


Characterization of 3D FBK pixels connected to R4S (2)









Summary and Outlook

- On CNM thin LGAD radiation-tolerance:
  - **Significantly better behavior of 35mm thick LGAD compared with 50 mm thick LGAD (gain and leading slew-rate wise)**
  - Timing resolution assessment still in progress.
  - High reverse current origin identified (new engineering run).
- On CNM 3D sensors:
  - **First IMB-CNM 3D sensors with almost final HL-LHC technology**
  - Excellent yield for 50x50 pixel cell form factor.
  - Good yield on 25x100 (1E) pixel cell form factor (low statistics).
  - Bad yield for 25x110(2E) pixel cell form factor.
  - Three wafers to be send asap to IZM for flip-chipping to RD53A ASIC.
- Dedicated study on FBK 3D sensors using R4S chip (high-resolution charge characterization without threshold).

Back-up

THANK YOU FOR YOUR ATTENTION

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BACK - UP

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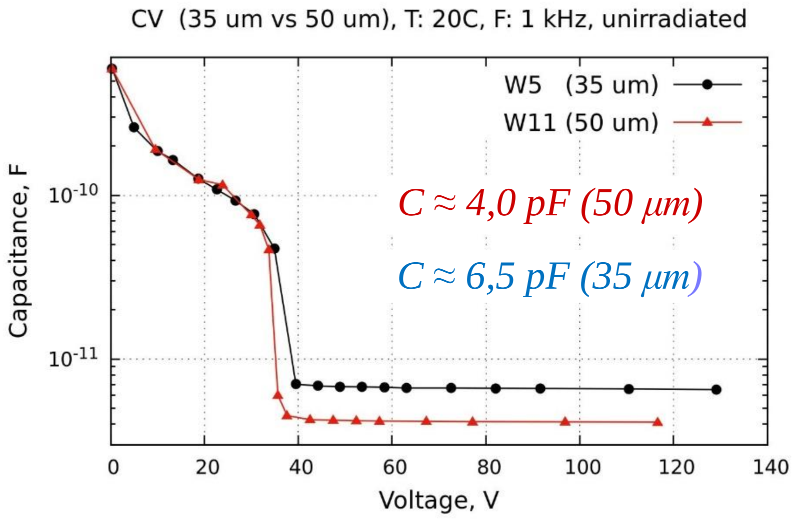
Electrical characterization: CV curves

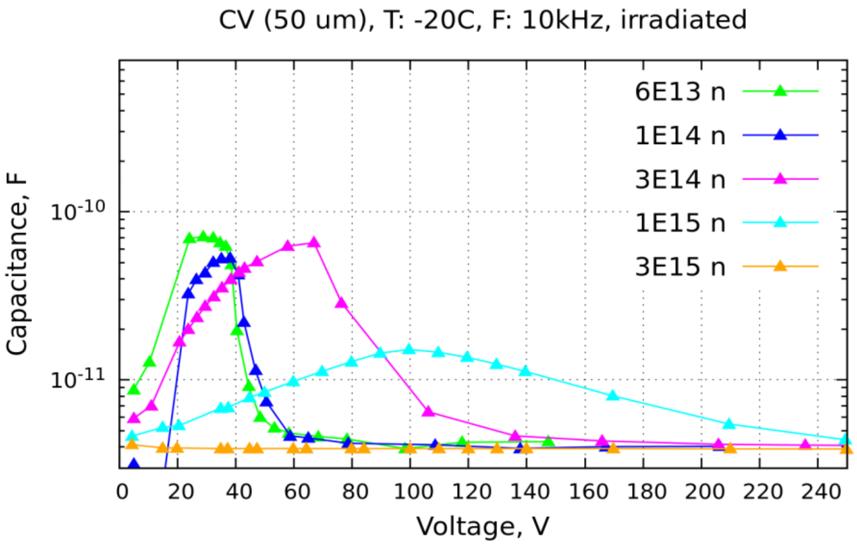
BEFORE IRRADIATION

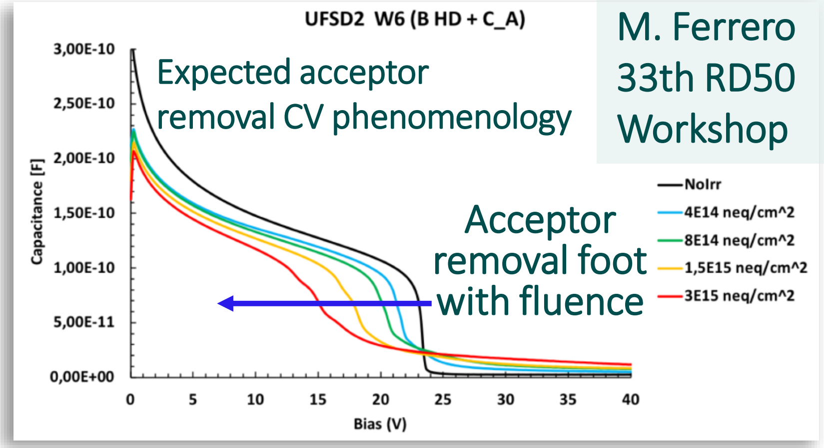


$C \approx 4{,}0$ pF (50 µm)

$C \approx 6{,}5$ pF (35 µm)

AFTER IRRADIATION





Expected acceptor removal CV phenomenology

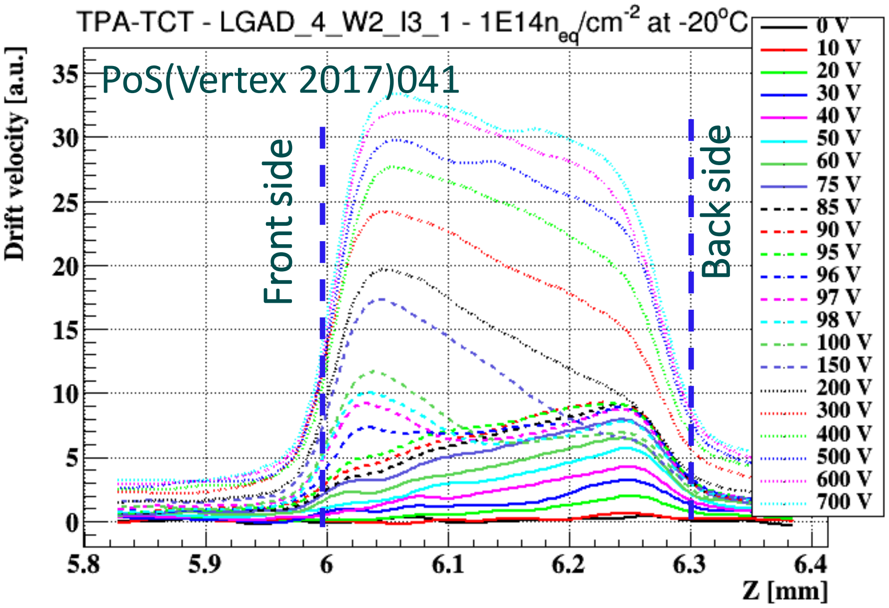
M. Ferrero 33th RD50 Workshop

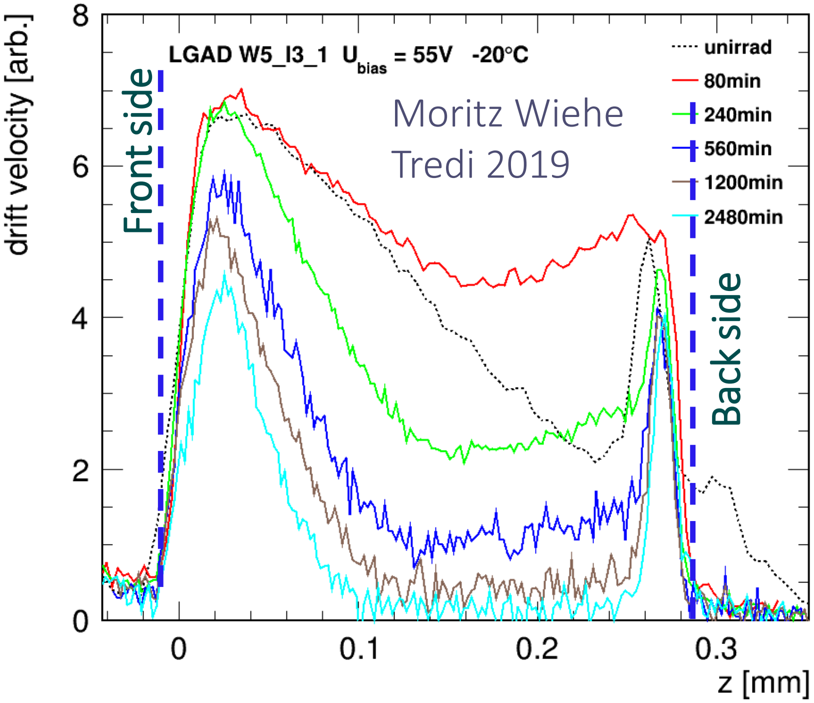
Acceptor removal foot with fluence

CV characteristics does not follow simple acceptor removal model after irradiation (to be discussed)

TCT Characterization: Charge vs. Bias Voltage (2)

- Positive shift of charge collection on-set observed previously in 300mm thick pad diodes with low reverse currents (few hundrend of nA on irrad).
- Caused by the Bulk Space Charge Inversion (BSCI) (trapped carriers)
- Double peaked E-field (velocity) with TPA-TCT and E-TCT profiles demostrated BSCI.



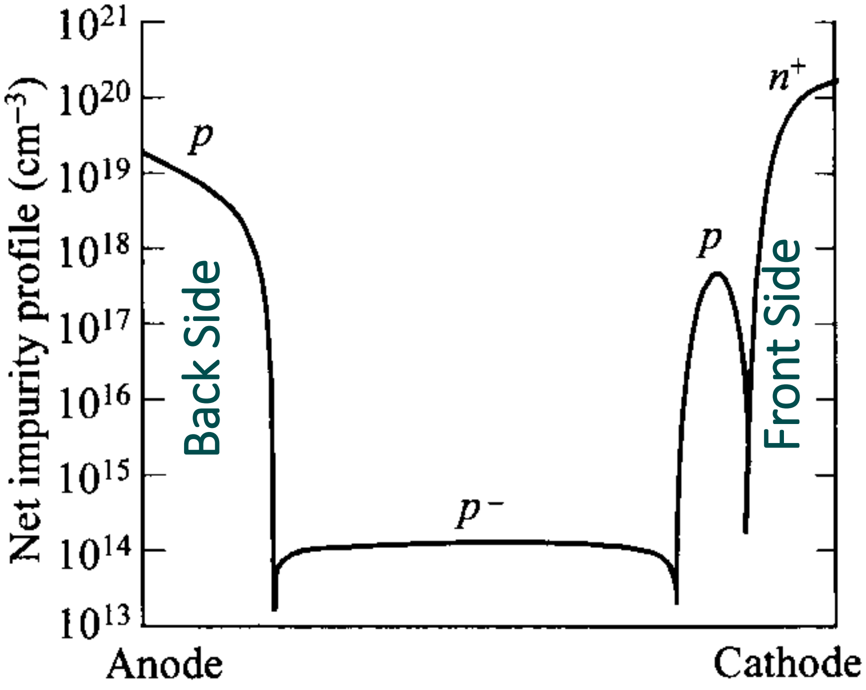


Does the BSCI induce the shift on the gain on-set?

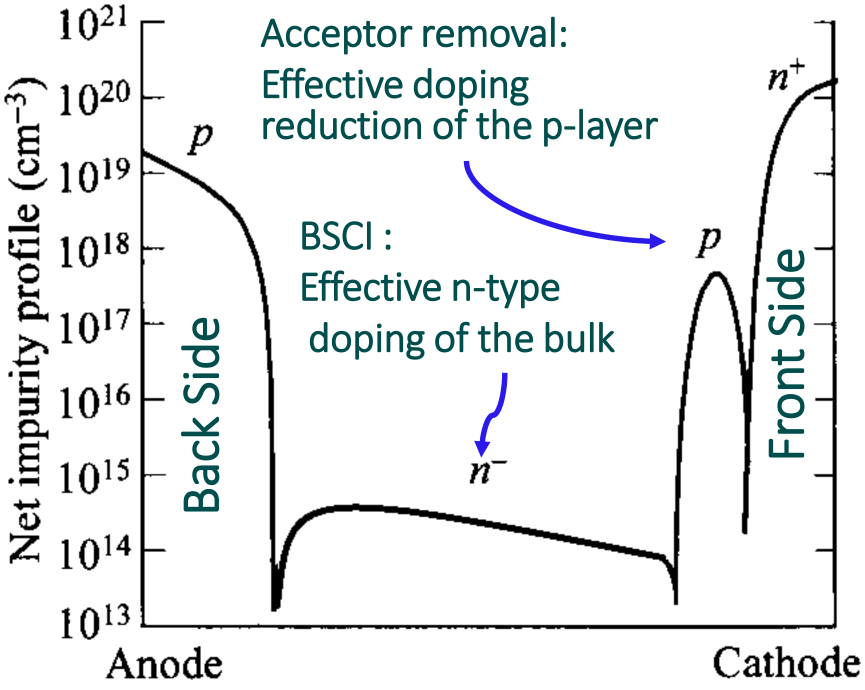
CV characteristic (revisited) - I

- Due to the BSCI of the p bulk, the LGAD becomes effectively a **Shockley four-layer diode** (aka Thyristor with floating gate).
- Can we explain the CV characteristic based on a Shockley four-layer diode?

Before irradiation,



After irradiation,

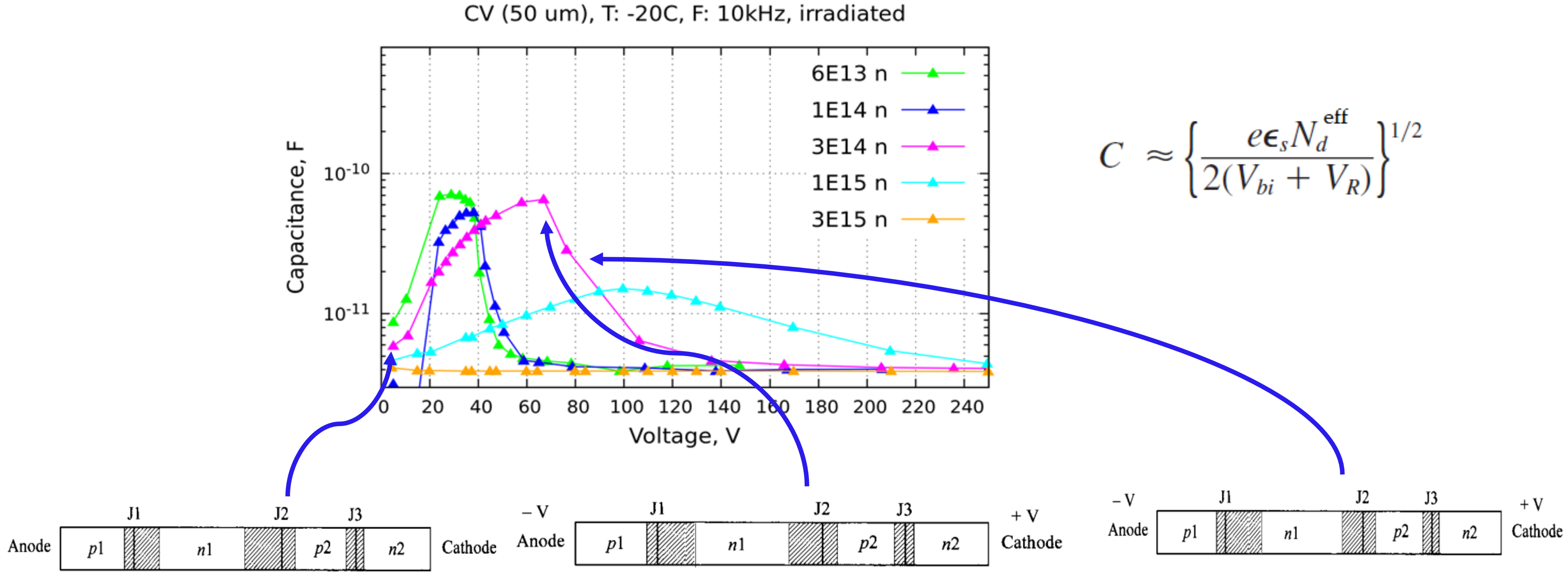


Acceptor removal:
Effective doping reduction of the p-layer

BSCI :
Effective n-type doping of the bulk

CV characteristic (revisited) - II

- The multijunction total capacitance is small than the smallest single junction capacitance.
- No biased:
  - J1 & J3 built-in field with same direction, J2 oposite
- Under bias(VR):
  - J1 & J3 reverse biased but **J2 is forward biased**.
  - J2 capacitance increases with VR while J1 & J3 decrease with VR.
  - Eventually J2 is not longer the smallest capacitance, J1 dominates (back side depletion and then J3 depletion)



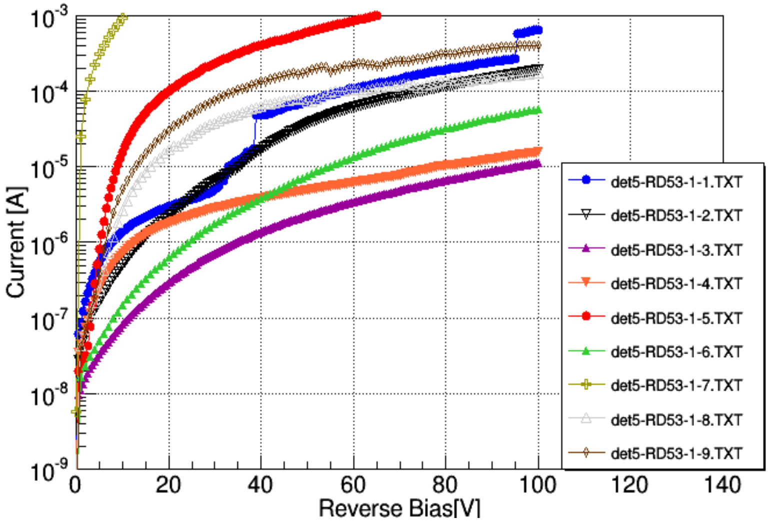
$$C \approx \left\{ \frac{e\epsilon_s N_d^{\mathrm{eff}}}{2(V_{bi} + V_R)} \right\}^{1/2}$$

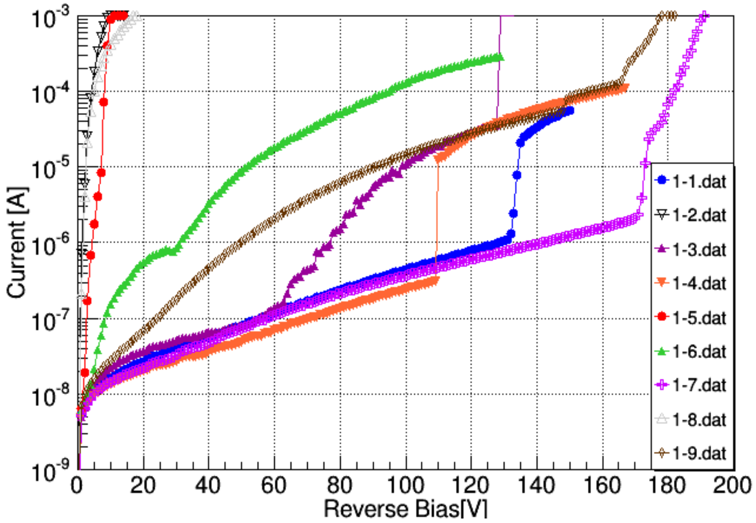
C3>C1 >C2

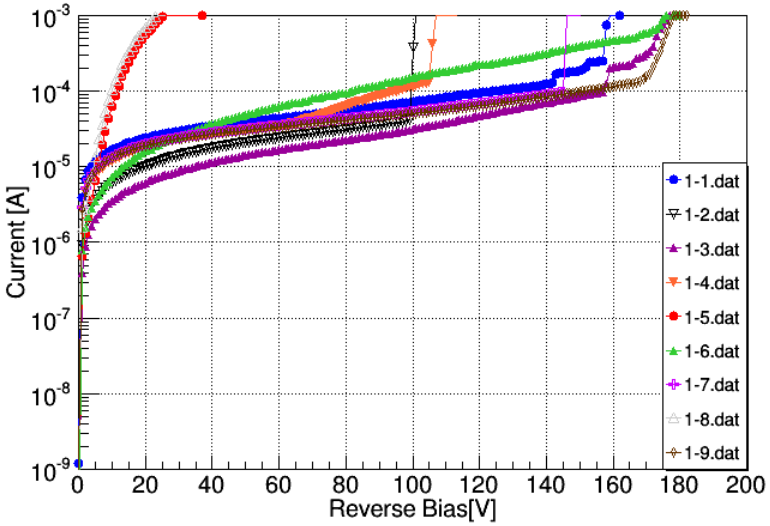
C3>C1=C2

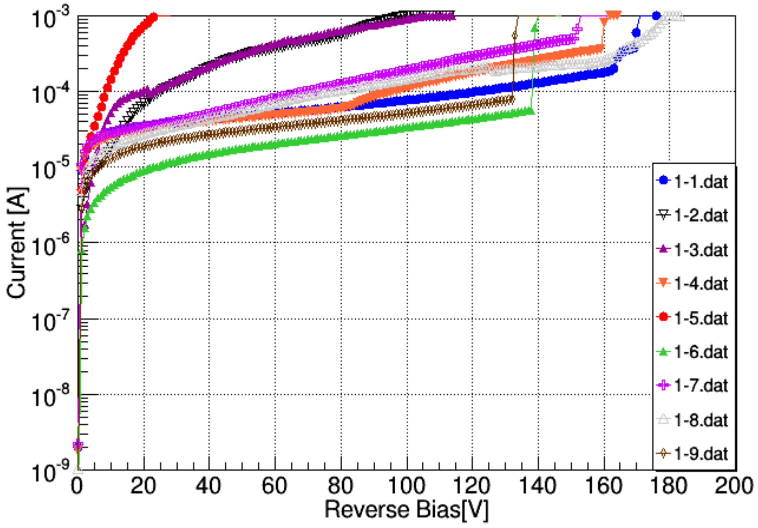
C1 < C2 < C3

QA using temporary metal: IV RD53A 50 x 50

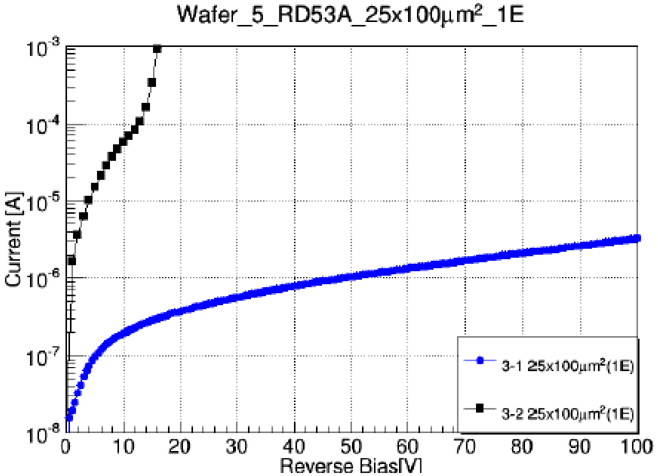

Wafer_5_RD53A_50x50μm²

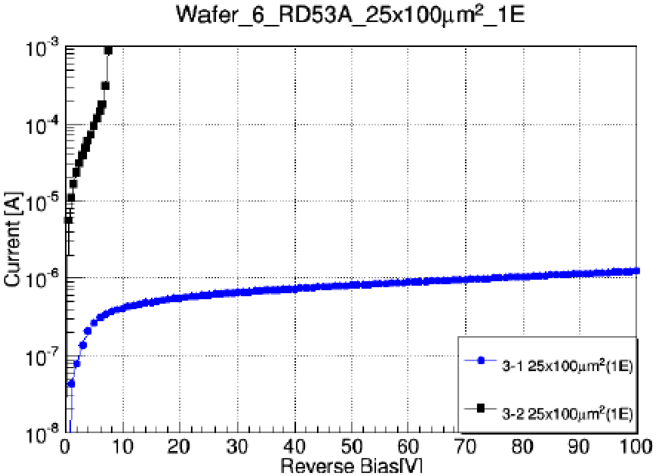

Wafer_6_RD53A_50x50μm²

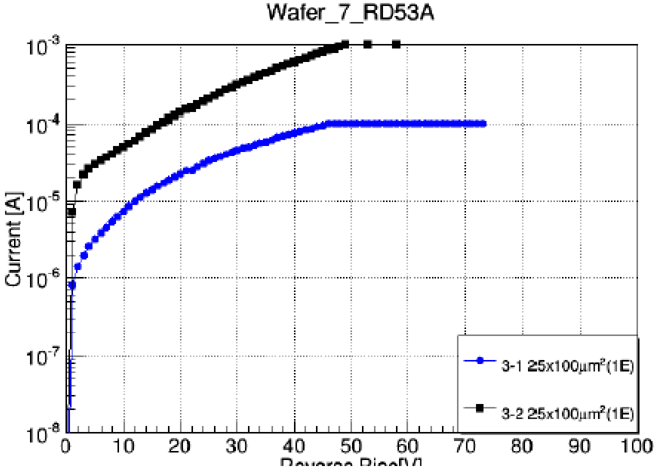

Wafer_7_RD53A_50x50μm²

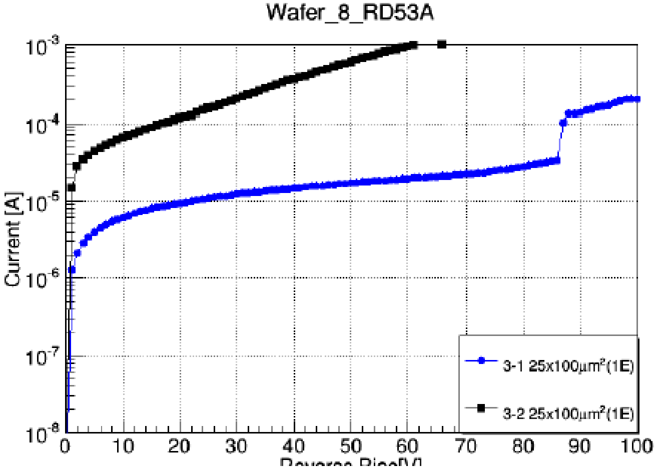

Wafer_8_RD53A_50x50μm²

QA using temporary metal: IV RD53A 25x100 (1E)


Wafer_5_RD53A_25x100µm²_1E


Wafer_6_RD53A_25x100µm²_1E


Wafer_7_RD53A


Wafer_8_RD53A

QA using temporary metal: IV RD53A 25x100 (2E)