

Thermal cycling tests on Indium bumped daisy chain modules

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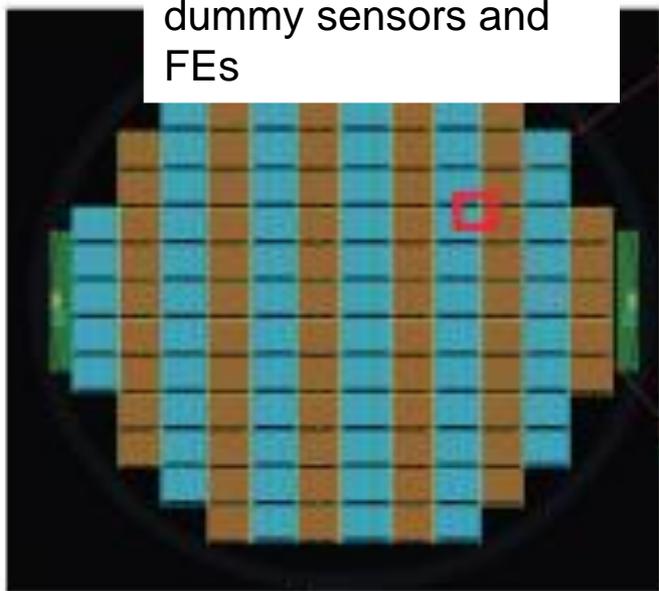
AIDA2020 Annual Meeting, Oxford, 03/04/2019

1: INFN Milano
2: INFN Genova

Thinned daisy chains from 300 mm wafers

- 300 mm wafers with daisy chains have been produced by IZM and three have been delivered to Leonardo with only metal pads (no UBM and/or bumps).
- Each dummy module has 336 columns with 400 bumps for a total of 134400 bumps tested per module and a density of 40000 bumps/cm²

300 mm wafer with dummy sensors and FEs



Dummy sensor

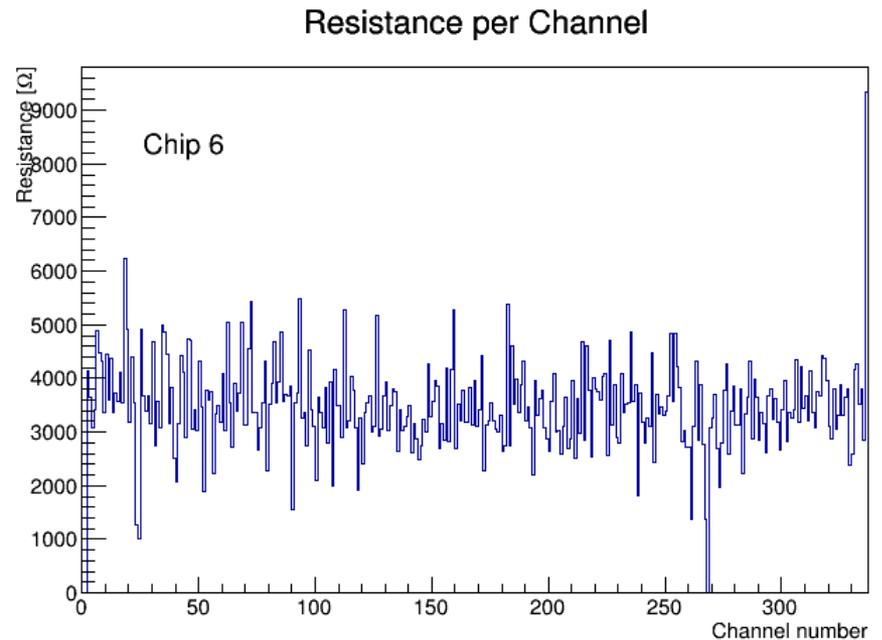
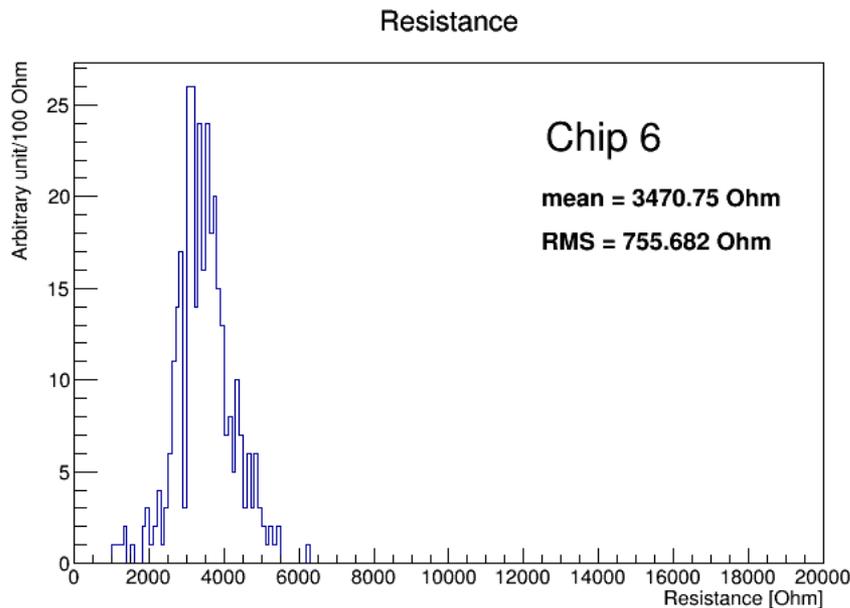
Dummy FE



b)

Assembled dummy modules

- Two 300 mm wafers have been deposited with Indium by Leonardo, diced and thinned by DISCO: one wafer to 150 μm and the other to 250 μm .
- 9 dummy modules from the 150 μm wafer and 5 from the 250 μm wafer have been flip chipped by Leonardo: total number of open+short less than 100 (from 150 μm) and less than 20 (from 250 μm) **with a total defect rate of about 7×10^{-5}** (see last ITk week @ Oxford and last AUW @ CERN)

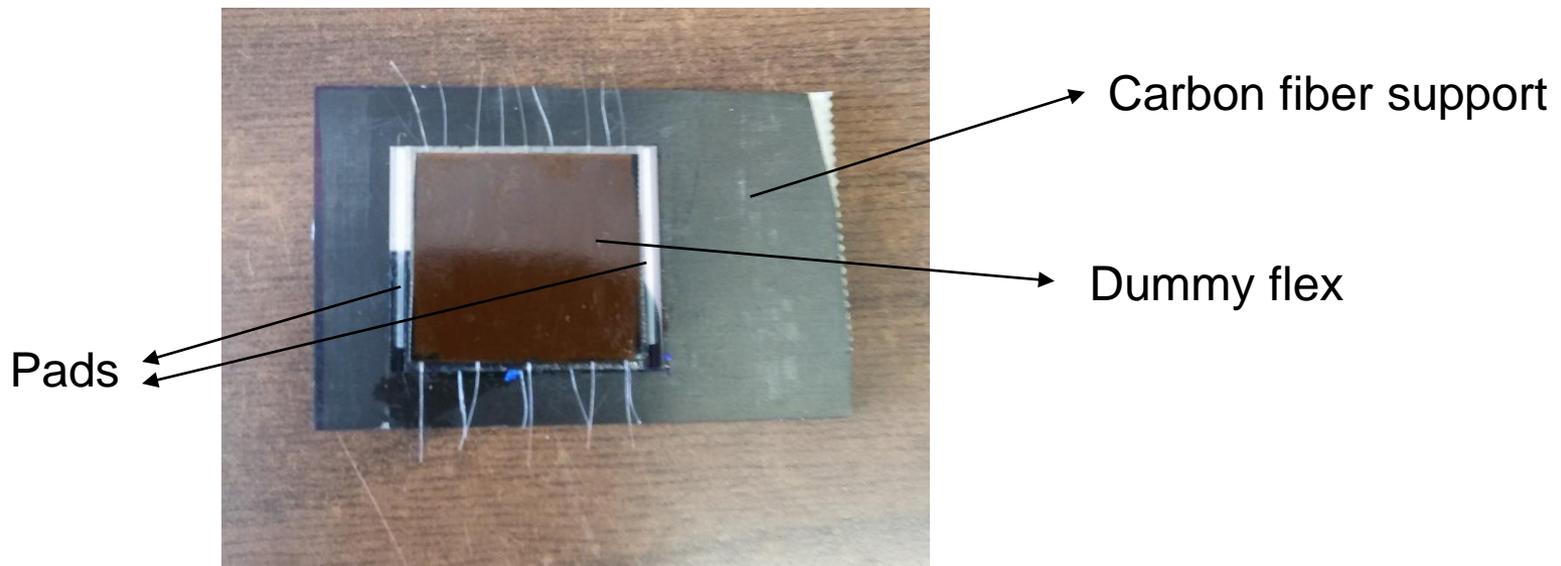


Samples

3 different modules under thermal cycles:

- 1) 150 μm thick, bonded at room temperature;
- 2) 250 μm thick, bonded at 90°C;
- 3) 250 μm thick, bonded at room temperature.

- Three dummy modules have been glued with araldite 2011 on carbon fiber (3x4 cm² of foam+90-0-90 prepreg) and cured at 45°C without any weight in Genova, thermal cycled and tested in Milano
- The second module have been also glued at Genova with araldite 2011 on a dummy flex module with 2 internal layers of dielectric and copper
- New results on thermal cycles are relative to the second module

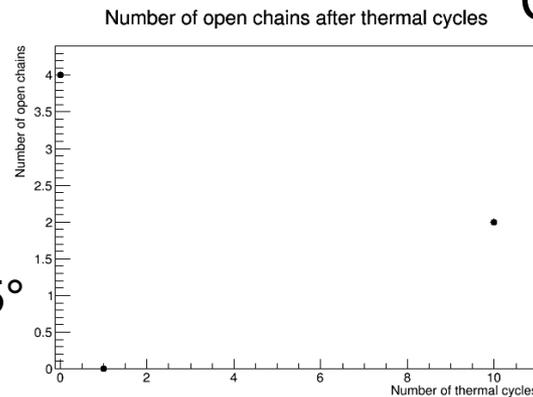


Preliminary thermal test

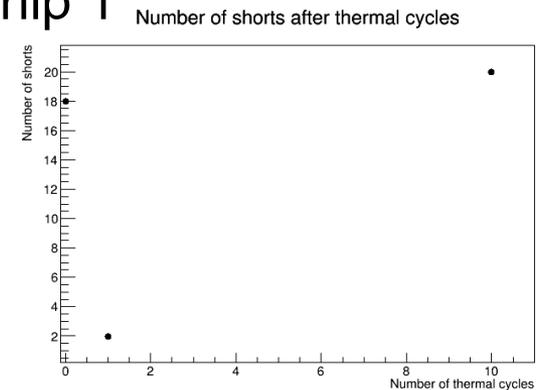
Simulation performed by Liam Cunningham (thanks!):

- Single chip FE_I4 size module
 - Thicknesses: FE=150 μm ; Sensor 150 μm
 - With and without Flex
 - Indium bumps: 50x50 μm pitch (336x400 bumps)
 - 100 μm epoxy layer vs constraints to ground
-
- At -55°C with flex the max shear stress is 4.9 Mpa
 - The Indium UTM is about 4.5 MPa: we should see the bumps failing after few cycles (basing on the Coffin-Menson model)
 - Without flex modules should withstand 1000-2000 cycles

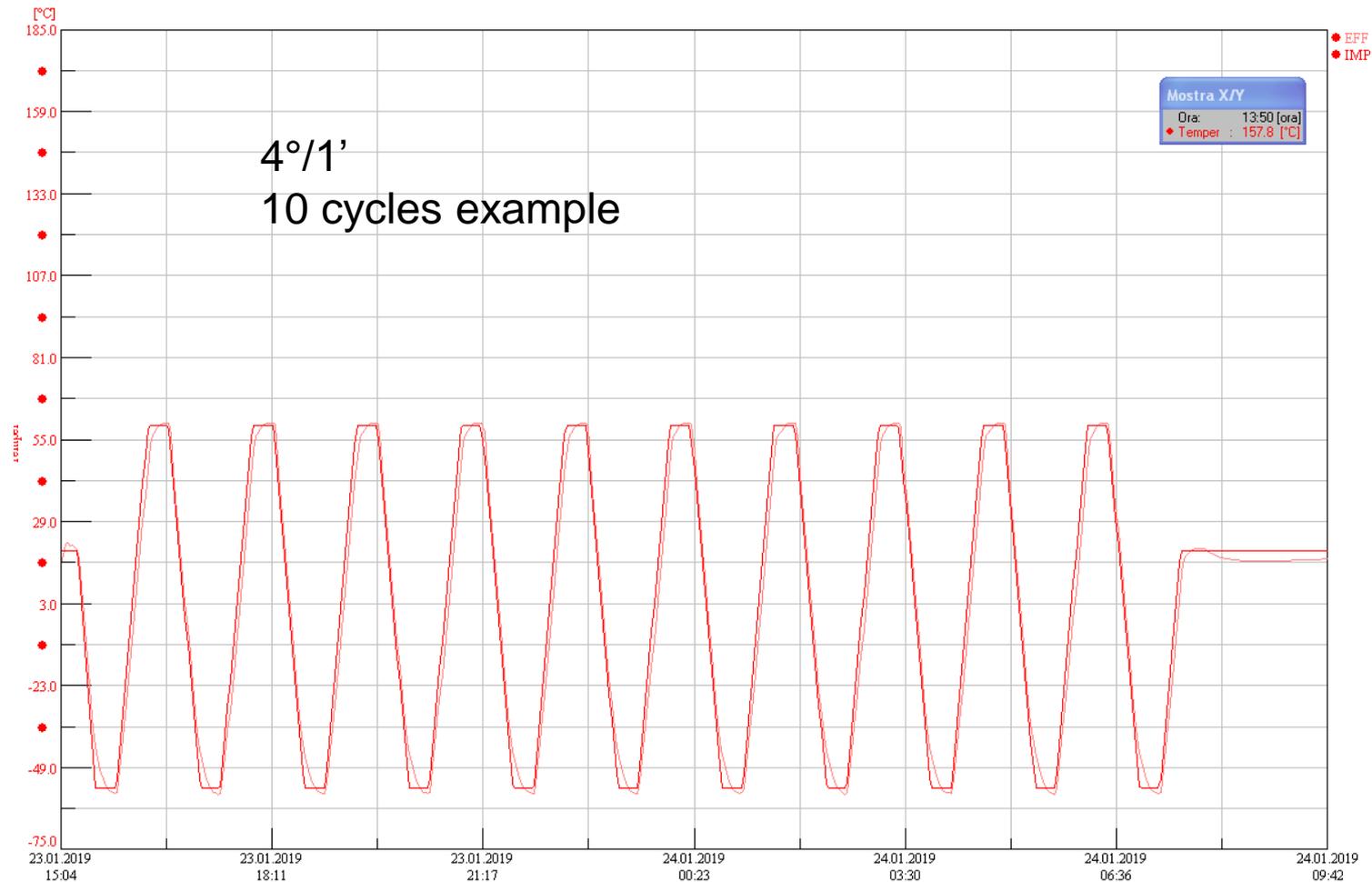
Previous results on the 3 chips with the only carbon fiber attached show no damages up to 10 thermal cycles between 60° and -55°



Chip 1



Thermal cycles steps

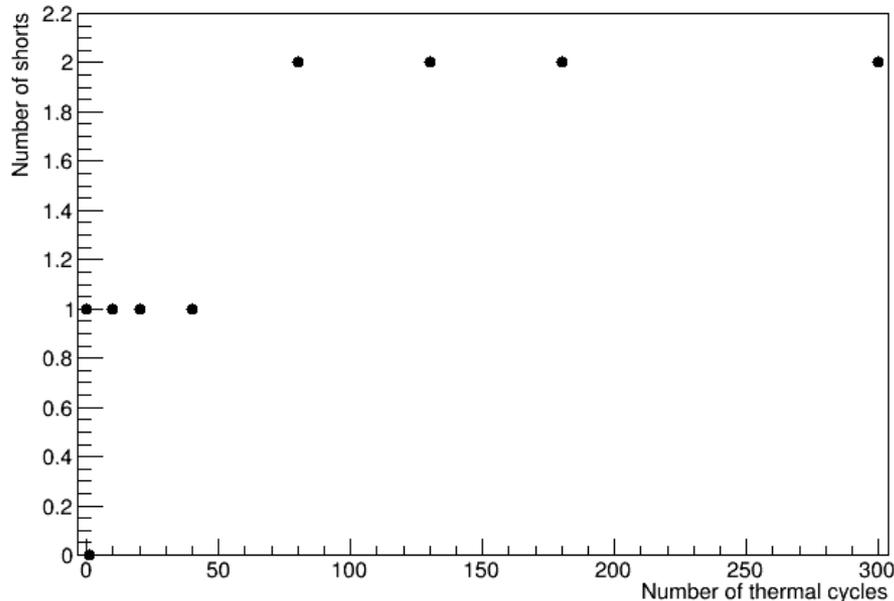


Repeated cycles between 60°C and -55°C, in steps of 10, 20, 40, 80, 130, 180, 220 and 300 cycles

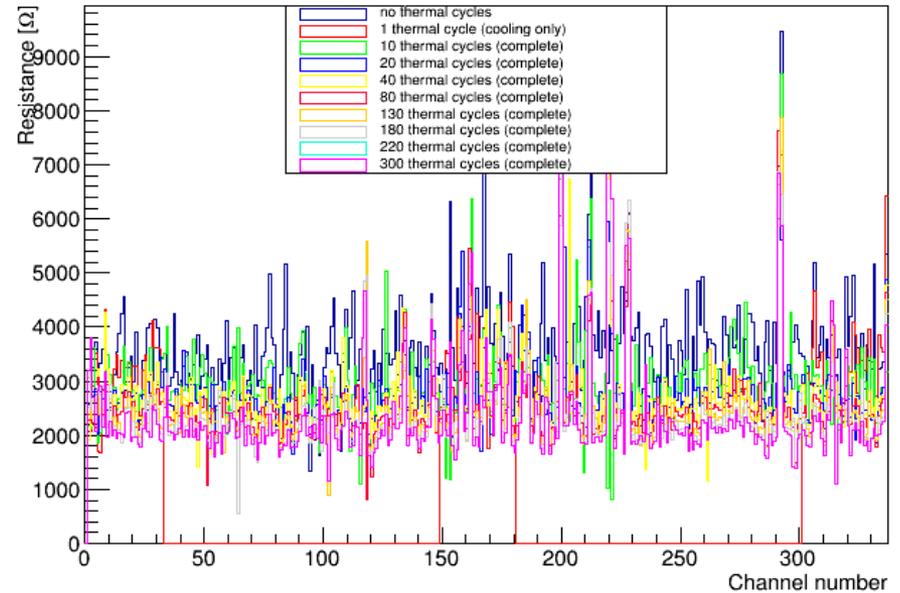
Results: open and shorts

- Without flex no chain is open after 300 cycles
- With flex, already after 1 cycle the second module show almost the whole number of chains open, the rest shows a resistance average 4-5 times increased (preliminary result)

Number of shorts after thermal cycles



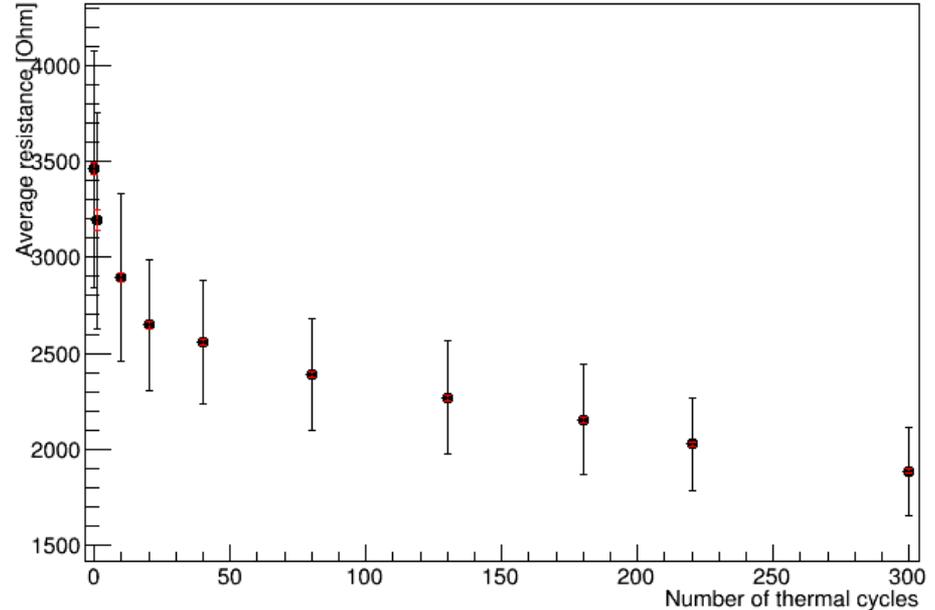
Resistances after different thermal cycles



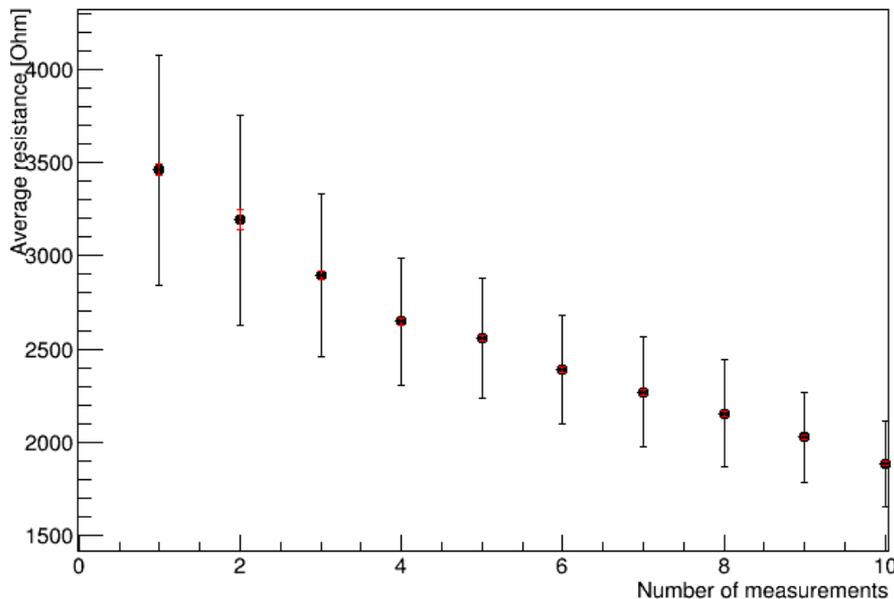
Results: resistances

Resistance after thermal cycles

Averages of resistances show an exponential behavior as a function of the number of cycles. This may be anyway a casual effect, as it depends by the number of cycles relative to each bin.



Resistance after measurements



This is confirmed by the more likely linear behavior of the averages of resistance as a function of the number of measurements on the same module.

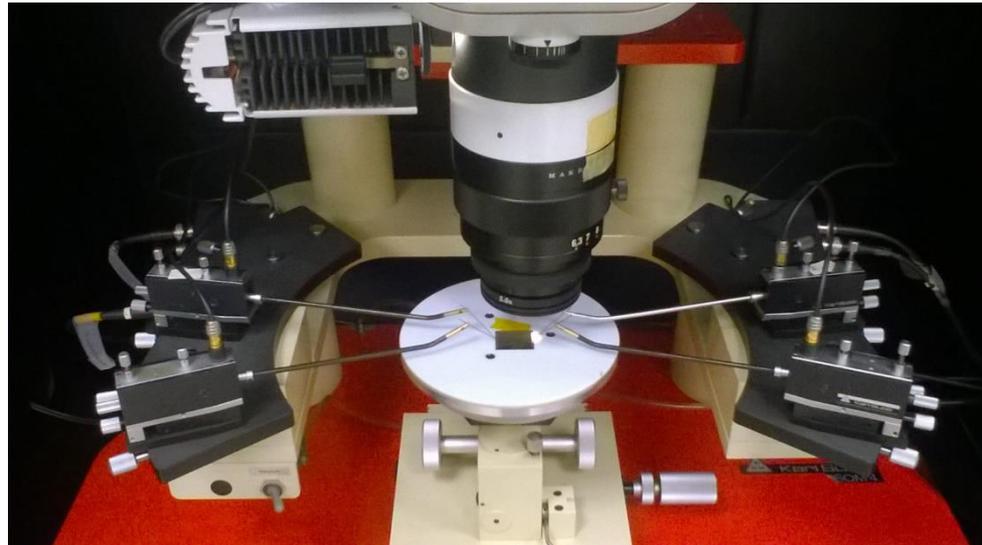
Conclusions

- Modules attached to carbon fiber without flex show no open chains after 300 thermal cycles with temperature ranging between 60° and -55° (1000-2000 foreseen by theory);
- Modules attached to carbon fiber and to a dummy flex show almost the 100% of chains open and the rest with averaged resistance values increased 4-5 times with respect to the nominal one (preliminary test);
- Further tests are on- going: thermal cycles on modules bump-bonded with a different procedure or attached to flex only, subdivide the thermal cycles into steps with lower temperatures.

Back-up

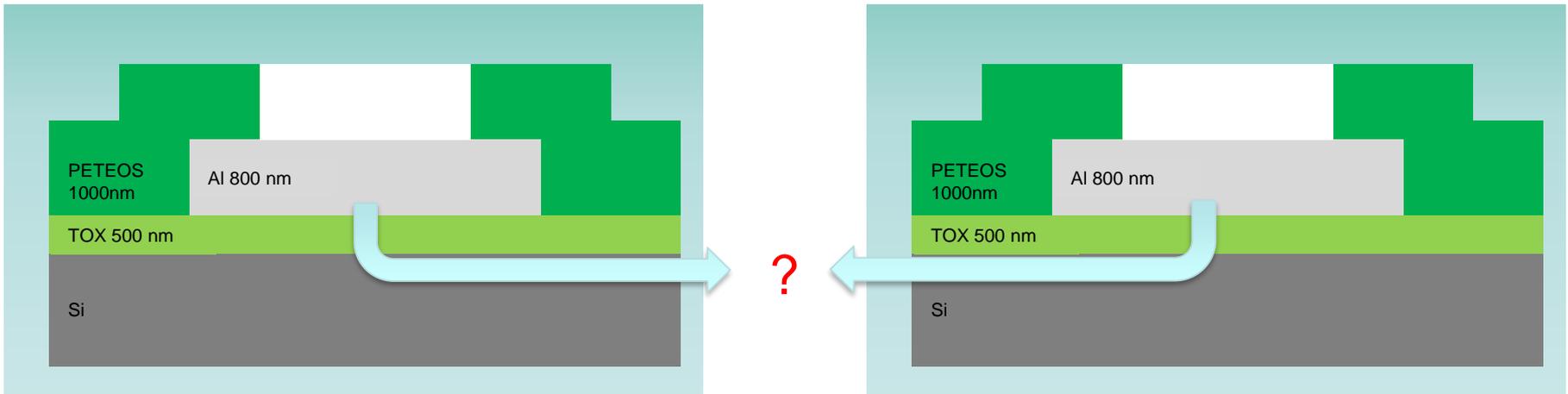
Assembled modules

- Two 12" wafers have been deposited with Indium by Leonardo, diced and thinned by DISCO: one wafer to 150 micron and the other to 250 micron.
- 9 dummy modules have been flip chipped by Leonardo, assembling devices from the 250 micron wafer: modules 1 to 3 at 90C, 4 to 6 at room T and the last 3 modules, 7 to 9, flipped at room T and then T increased to 90C
- Preliminary measurements performed in Milano



Not only Indium oxide...

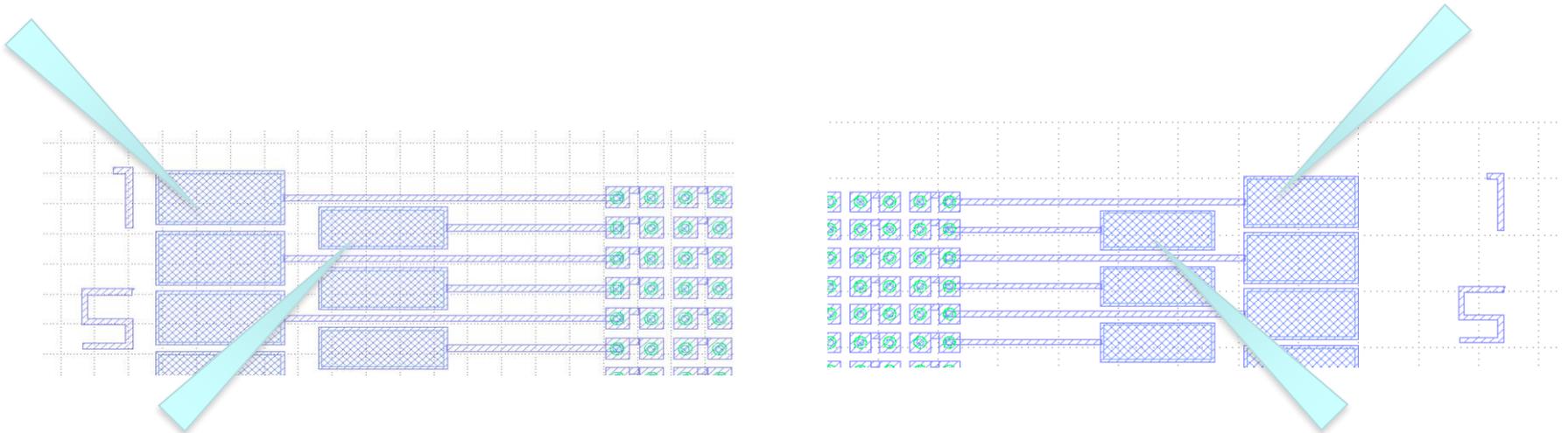
- Other than the “sparks” problems, we think there is another limitation: given the high voltage, sometimes a path, different from the daisy chain, can be opened, faking a short between adjacent chains...



- After several trials and completely changing the measurements setup, we found that using an AC between 150 V and 240 V, most of the times the indium is opened and the daisy chain resistance can be measured.

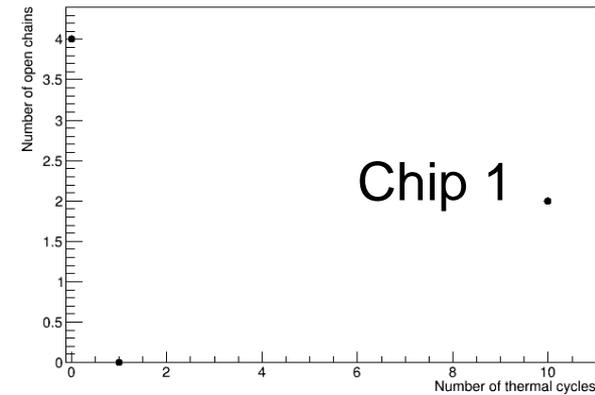
4 probes setup

- Given the 4 probes test setup, all the columns are tested for missing bumps, but only half of column pairs are tested for possible shorts
- Oxide opening 150-240 V AC. Resistive measurements: 0.1-4.5 V DC. Always with 1mA current limit

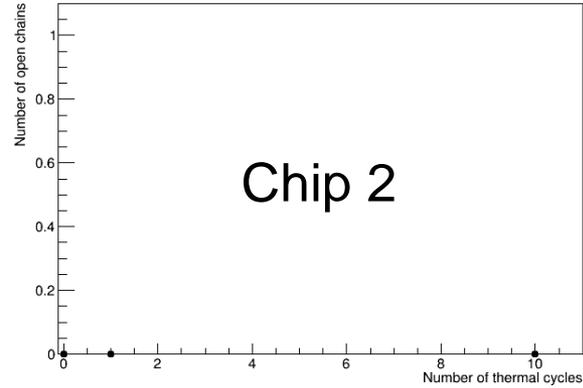


Results: open and shorts

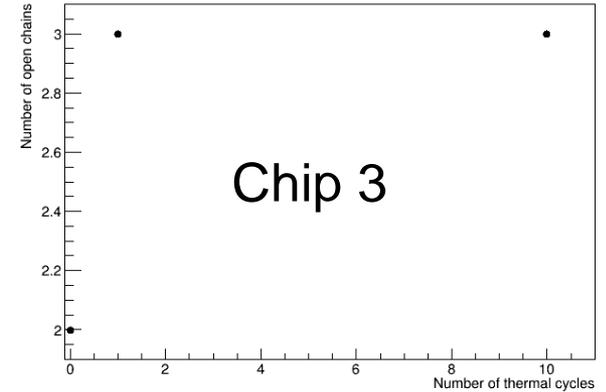
Number of open chains after thermal cycles



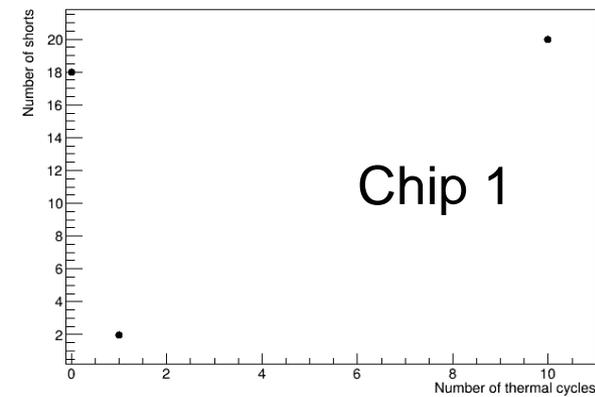
Number of open chains after thermal cycles



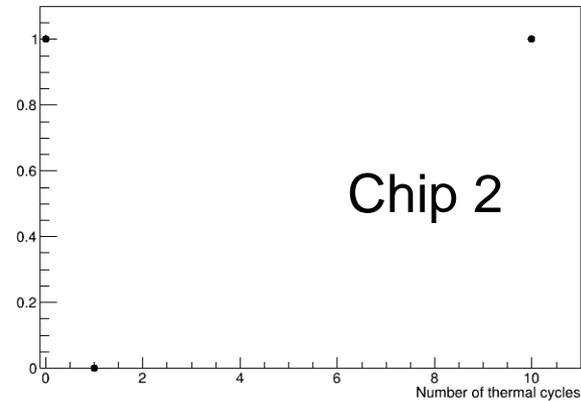
Number of open chains after thermal cycles



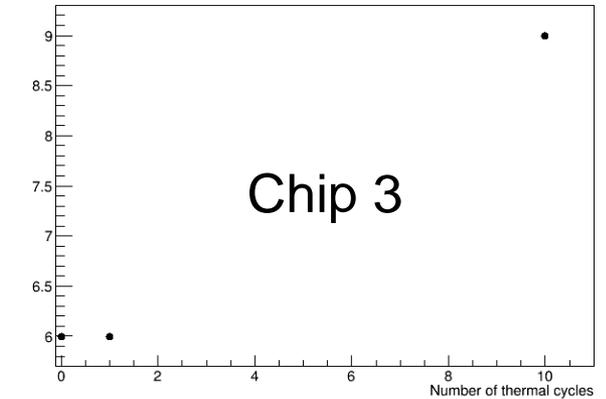
Number of shorts after thermal cycles



Number of shorts after thermal cycles



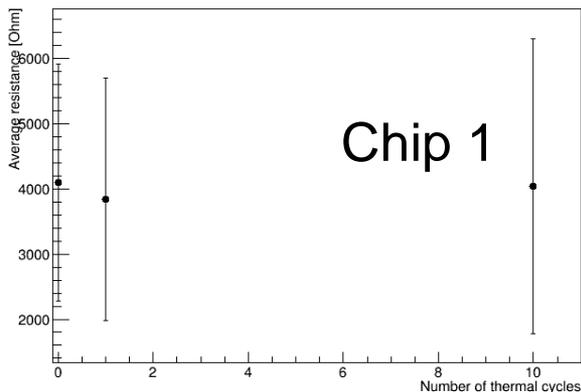
Number of shorts after thermal cycles



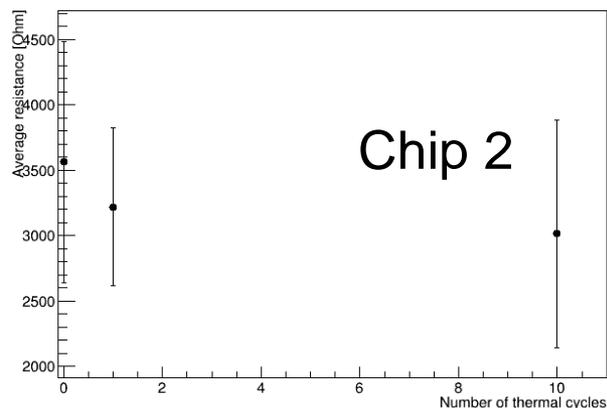
Step 1 (1 cycle only) has measurements relative to only a part of all channels

Results: resistances

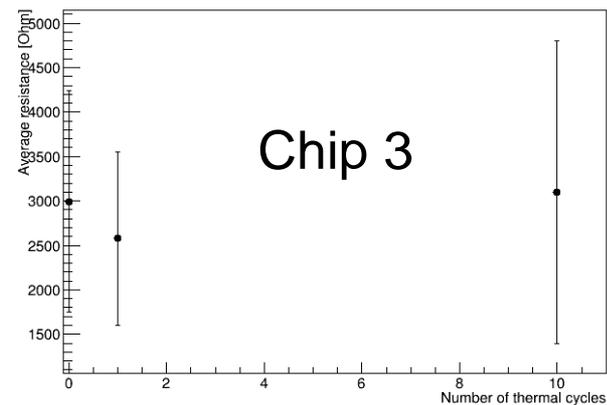
Resistance after thermal cycles



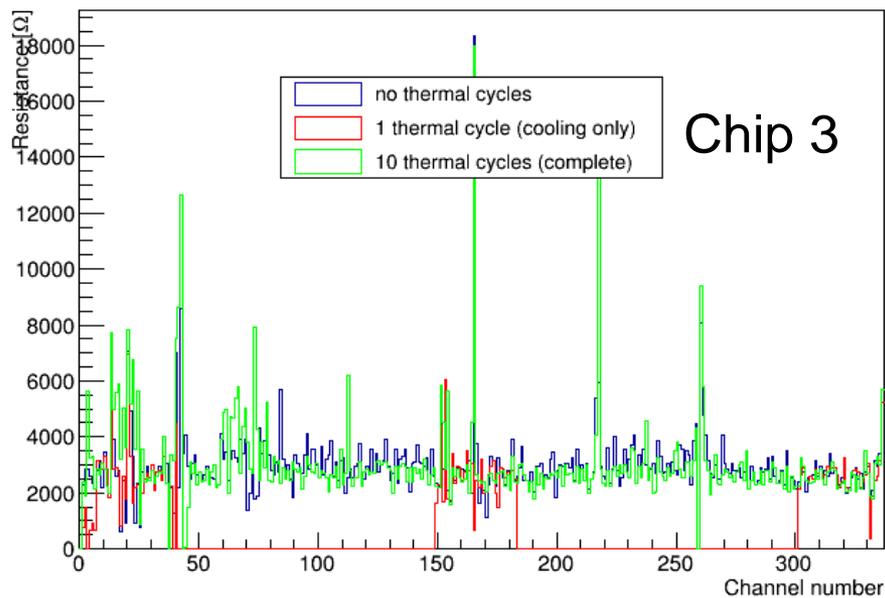
Resistance after thermal cycles



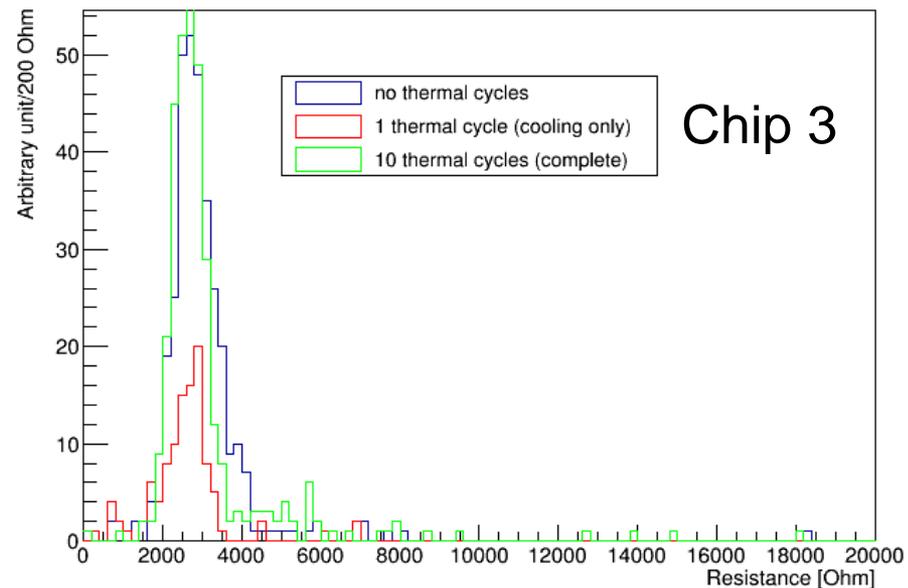
Resistance after thermal cycles



Resistances after different thermal cycles



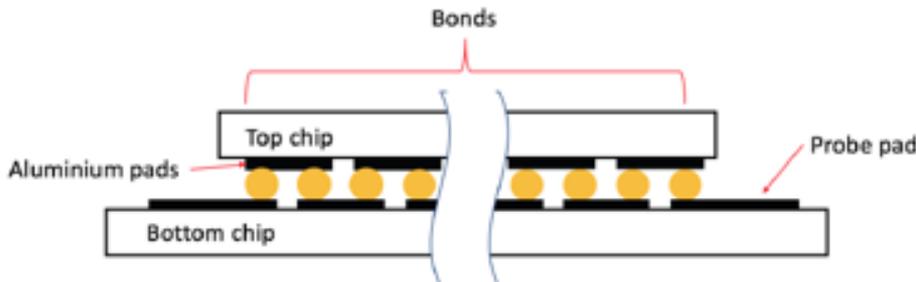
Resistance distribution



Step 1 (1 cycle only) has measurements relative to only a part of all channels

Dummy daisy chains

- Daisy chain test structures have been produced within the ITk community to prove the hybridization process on devices closer to the proposed ATLAS ITk Pixel chip before the real chip were available.
- The die has the same size as an FE-I4 chip, but a uniform bump pitch of $50 \times 50 \mu\text{m}^2$ (40000 bumps/cm²). Indium bumps of 12 μm and 16 μm diameter with an average height of 10 μm were deposited by Leonardo.



Measurements demonstrated the ability to bond high bump density large chips (FE-I4 size dies), albeit with thick chips from a 150 mm wafer.

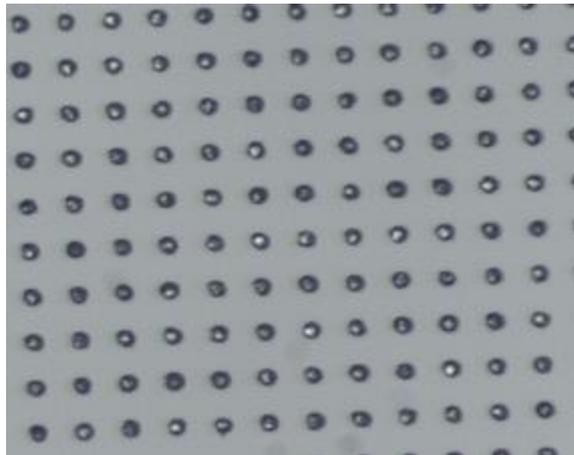
3 different modules under thermal cycles:

- 1) 150 μm thick, bonded at room temperature;
- 2) 250 μm thick, bonded at room temperature;
- 3) 150 μm thick, bonded at 90°C.

Indium bonding process

The bump-bonding process consists of two steps:

- bumps are deposited on both dies to be connected. This operation is performed at wafer level, together with other wafer processes, as the deposition of a metal layer in the bump area (UBM, under bump metallization);
- wafers are cut, and the individual dies are connected using a technique called “flip-chip”. This thermo-compression step is particularly labor intensive, as accurate alignment is needed and prone to errors.



Indium bumps (diam 16 μ m , pitch 50 μ m)

