Status report

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Design of a Multi Chip Module for a general purpose readout system for MPGD:s

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(on behalf of the Lund group)

Reminder

The goal of the full project: Construct a general purpose readout electronics for MPGD:s, with high position resolution.

This requires: Small readout pads (<= 1x6 mm2).
The channel density of the readout electronics has to match the small pad size.

- The aim of the project is thus to produce front-end electronics comparable in size to the readout pads.
- This readout electronics can be used in smaller MPGD-detectors for applications in various fields like particle physics detectors, medical diagnostics , material science at XFEL, and for investigations at ESS.
- The readout electronics is based on the SALTRO16 ASIC, which integrates the analogue and digital processing in the same chip.
- The size of the die itself is about 8.7x6.2 mm^2, which corresponds to a channel occupancy of 3.37 mm^2/channel.

Eight SALTRO16-chips are mounted on a Multi-Chip-Module (MCM) board, which also contains a CPLD, connectors and passive components. In our design the channel occupancy is 6.4 mm^2/channel

A new test board

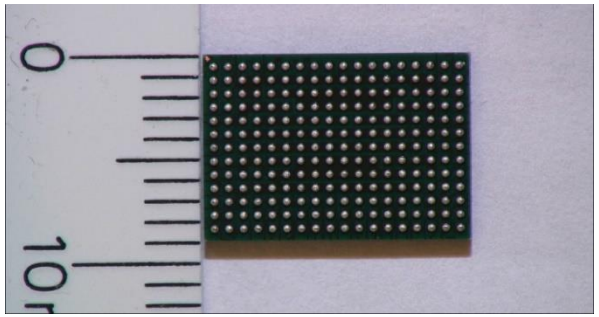
The original idea was to mount the dies on a carrier board, but the company failed to bond the dies succesfully.
Instead we had the dies packaged. Since the BGA footprint is different for the packaged chips compared to the originally intended carrier board,the test board had to be modified and a new test socket had to be purchased.

The test board is read out via an SRU (Scalable Readout Unit).

The FPGA firmware on the SRU is using the ALICE and TOTEM systems.
However, this firmware has to be modified for full functionality in our application.

The firmware for the CPLD is adopted from the ALICE exp.

End of July 2017 we received the first pre-sample of 34 packaged chips, which had a perfect surface quality and very precise dimensions.



- From the subsequent tests in Lund only 20 chips passed the requirements, which corresponds to a success rate of less than 60%. This doesn't include chips that were used for setting up the system.

- It was carefully tested that there was no bug in the test board.

- A procedure for selecting and positioning the dies was agreed on with the company and a second pre-sample of 55 chips was ordered.

- At the end of May the second pre-sample was delivered and subsequent tests in Lund showed that 46 chips passed the requirements, corresponding to a yield of more than 80%.

- Packaging of the full sample was ordered and the delivery followed at the end of November 2018

Present status of the SALTRO16-chips

- We have 66 chips that have passed the test requirements.

- All dies have been packaged. Out of the remaining dies 705 was selected after visual inspection. Out of these 682 were succesfully packaged.

- The 66 tested chips are more than enough to produce a prototype system.

- The remaining chips will be tested as soon as we have a fully functional readout system. For this we need help with the FPGA-progamming of the CPLD.

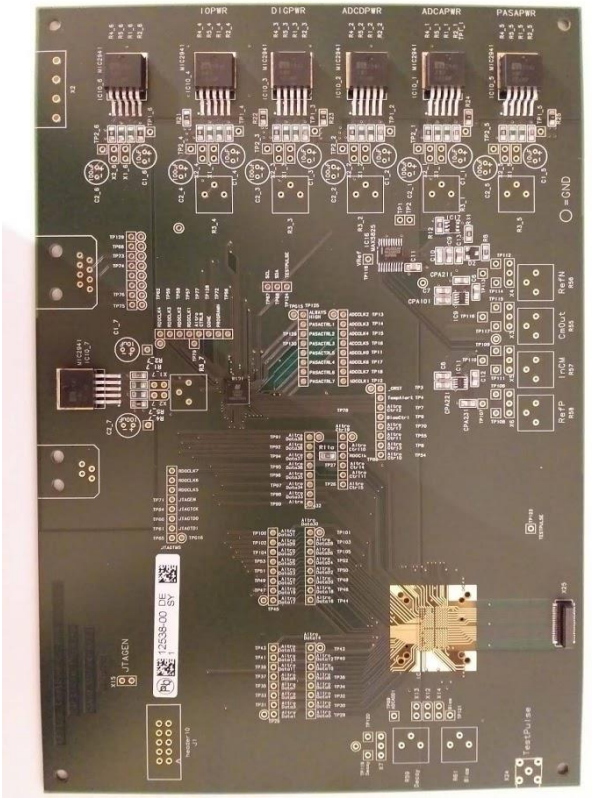
A further modification of the test board

A new and somewhat smaller CPLD has been found, which helps in the deployment of the components on the MCM-board. The new CPLD has a slightly different pin layout and therefore a new test board had to be developed.

The PCB has been delivered and the components have been mounted. The new test board is functional.

The aim is to test all the packaged chips with this test board but this can only happen when the firmware for the CPLD and the SRU has been finalized.

Tests of a SALTRO16 chip with the new test board, has been performed with the present firmware, in order to make sure that the routing for the CPLD was correct and that the firmware of the previous CPLD was successfully installed.



The final MCM-board

- The MCM-board had to be re-desinged, due to the replacement of dies mounted on a carrier board with the packaged chips and due to the new CPLD, but is now in its final stage. The design of the low voltage distribution is still remaining.

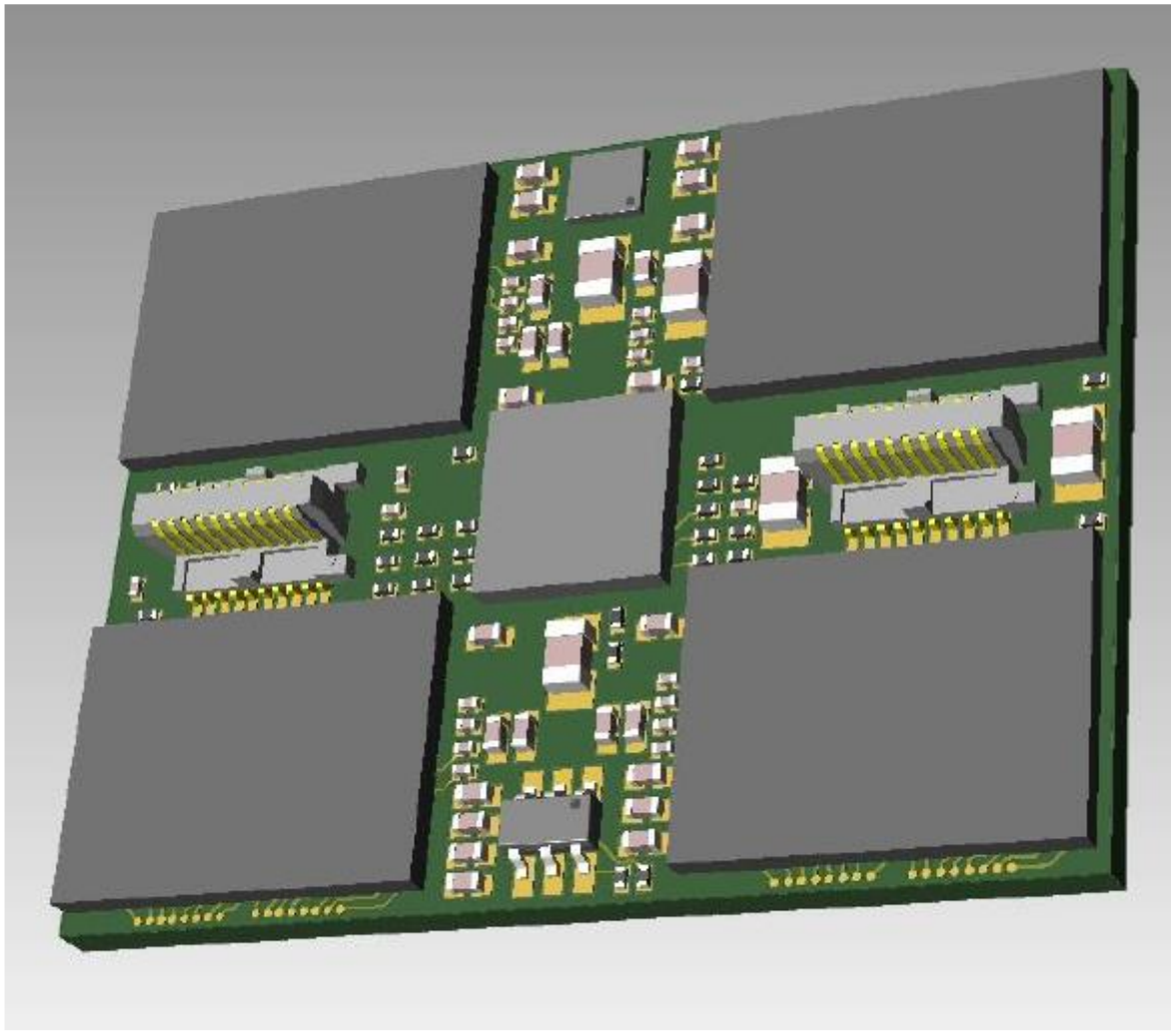
In the present ALTRO system there are 7 separated voltages and thus 7 voltage regulators are needed. We have investigated whether some of these can be combined so that the number of voltage regulators can be reduced. Tests have shown that the number of voltage regulators probably can be reduced to three with the option of a further reduction to two. This can only be verified through tests with the final MCM-board.

$\Rightarrow$ The Low Voltage Board has to be re-designed, which has implications for the voltage distribution on the MCM-board.

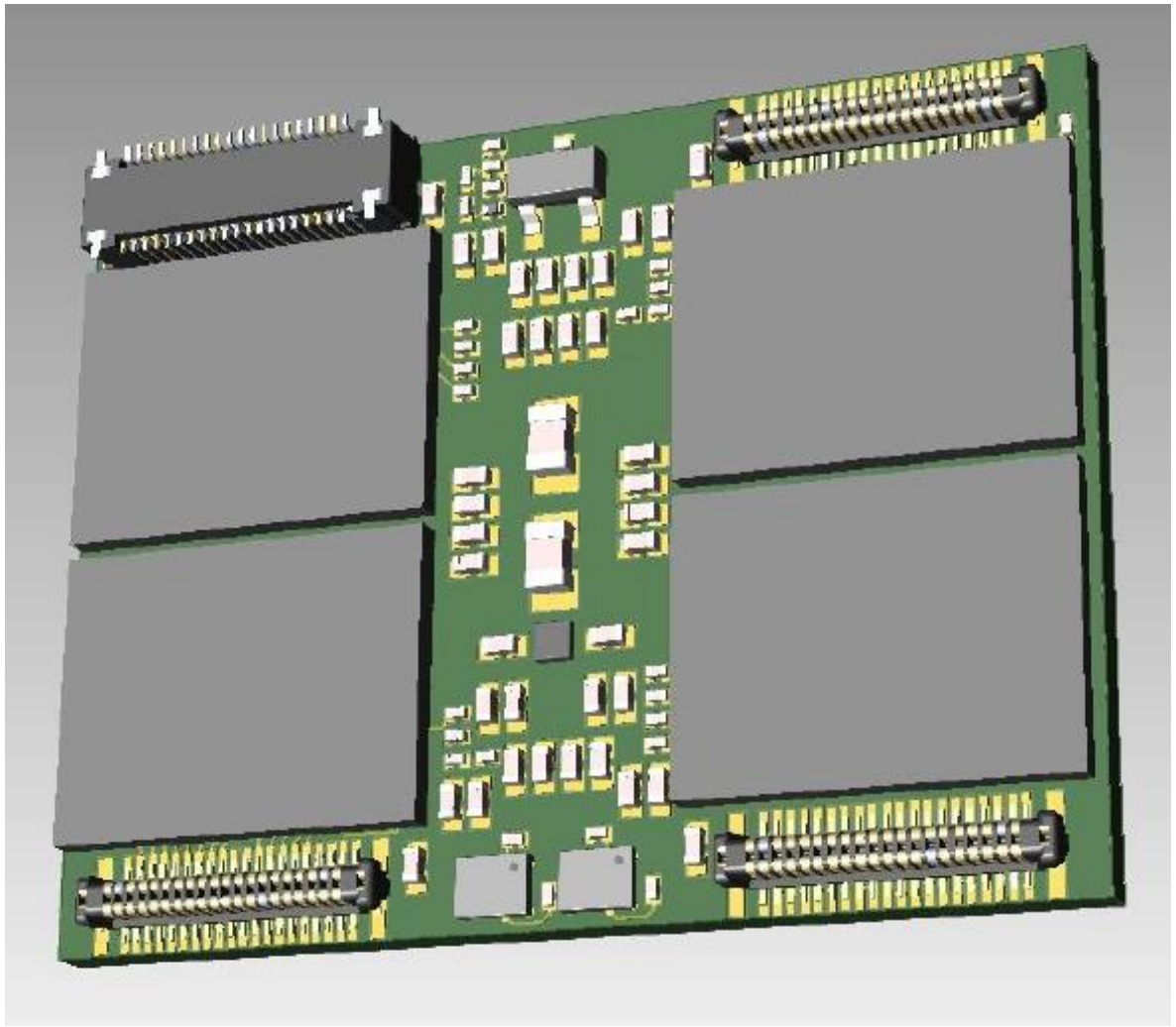
- The design of the final MCM-board can now be completed and a prototype MCM can be produced.
- Soldering tests with empty packages will be performed.
- After succesful test soldering, the MCM-boards will be mounted.

The MCM-board

The top side



The bottom side



Status of the DAQ system

- With the present DAQ-system we are limited to perform a full readout of 2 channels out of 16 alternatively to read out all channels but limited to 140 samples.

- The CPLD: the firmware, for the old testboard, has been modified and tested for the new test board.

- The SRU: re-arrangement of the memory management is necessary for full readout of al 16 channels. A bug which causes the system to hang has to be solved. This needs an FPGA programmer.

- The PC: the firmware exists but has probably to be further developed.

Cooling

Contact was established with Filippo Bosi, whose group in Pisa is working on micro channel cooling within the AIDA2020 project (WP 9). He offered himself to develop a cooling system for our puprose.

A mockup board was sent to us by Takahiro Fusayasu at KEK and was forwarded to Pisa. This board simulates one SALTRO chip ladder with 5 MCM-boards providing a realistic simulation of the power dissipation and could thus be used to test the performance of the micro channel cooling.

This has not yet been done since unfortunately Filippo got health problems.

The cooling is not part of the Lund commitment.

What has been acheived since the last AIDA Annual Meeting

- The full batch of SALTRO16-chips has been packaged.
- Two new test boards have been produced.
- A chip already successfully tested with the old test board, have been tested with the new test board to make sure that the routing of the new CPLD was correct and that the old firmware had been successfully implemented.
- Promising tests to combine some of the voltages have been performed.

Plans for the next future

- Re-design the Low Voltage Board.
- Test the Low Voltage Board
- Finalize the design of the MCM-board.
- Have a prototype MCM-board mounted.
- Tests of the prototype MCM-board