EMBEDDING MICROFLUIDICS INTO MICROELECTRONICS

WP9: NEW SUPPORT STRUCTURES AND MICRO-CHANNEL COOLING

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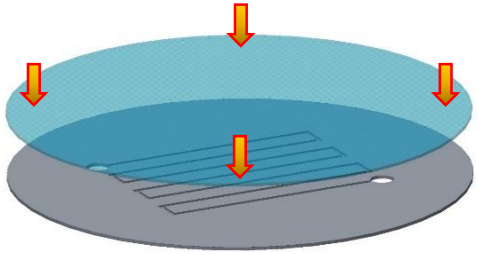
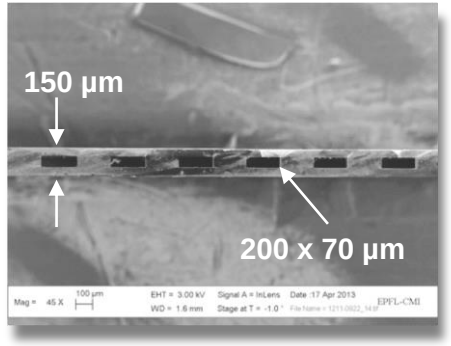
LAST YEAR

https://indico.cern.ch/event/677272/contributions/2976451/attachments/1638712/2615630/AIDA2020_status_update.pdf

Microchannels etched on a 4” silicon wafer and sealed with a glass wafer through anodic bonding process (350 °C) (close collaboration with Center of Micronanotechnology at EPFL)

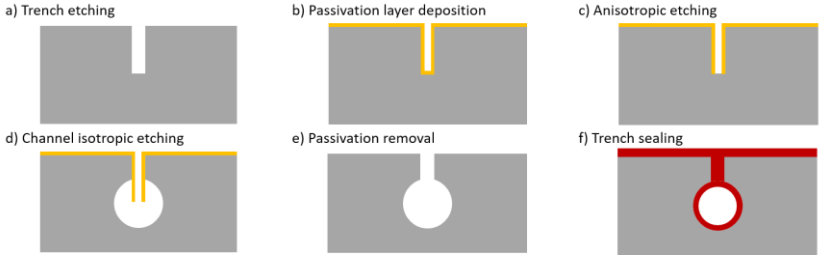


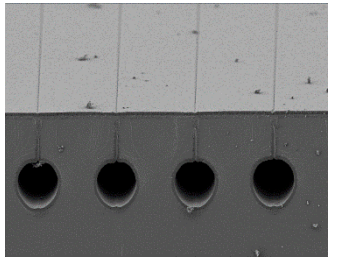
Microchannels etched on a 8” silicon wafer and sealed with another silicon wafer through direct bonding process (1050 °C) (external partners)



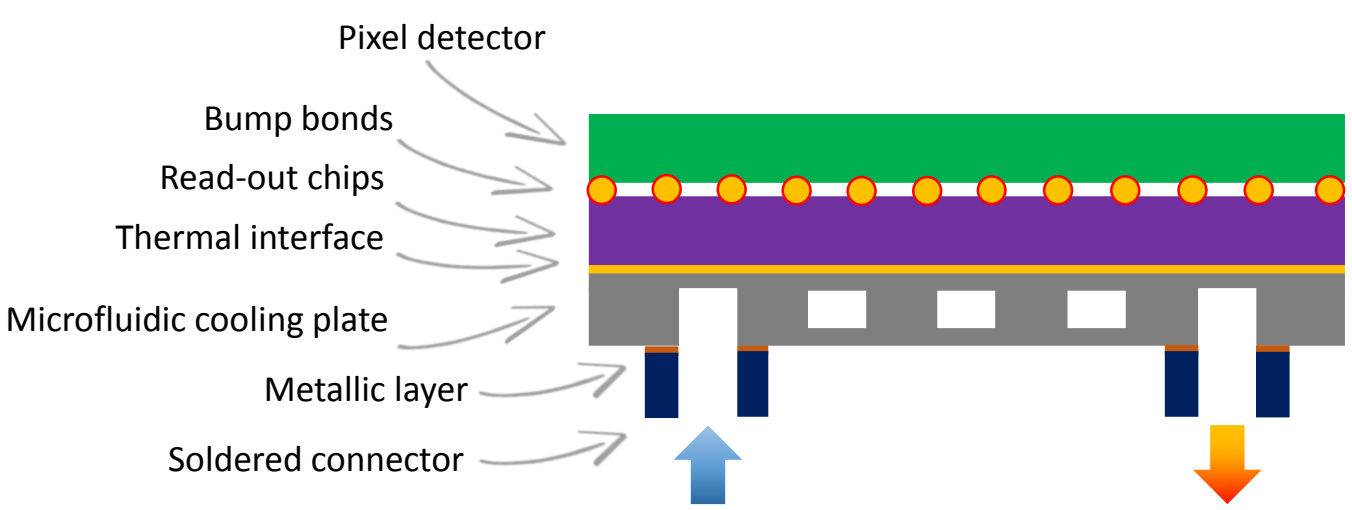
Microchannels without bonding process: buried channels (300 °C) (just mentioned last year)

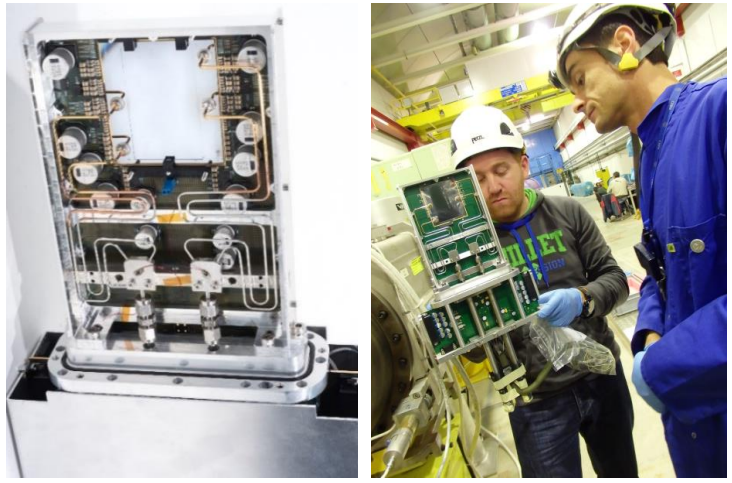
M. Boscardin et al., *Silicon buried channels for pixel detector cooling*, Nuclear Instruments and Methods in Physics Research, Section A, 2013
C. Lipp, *Approaches for the fabrication of silicon buried channels for the thermal management of monolithic pixel detectors*, MSc Thesis, EPFL, 2017





Microfluidic cooling plates for NA62 and LHCb (on hybrids)

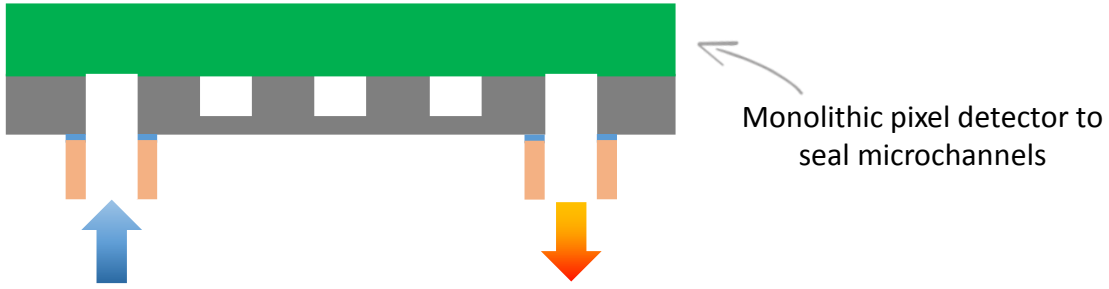




2010: start of the R&D campaign
2014: first detector with cooling plates (NA62)
2021: integration of cooling plates in LHCb

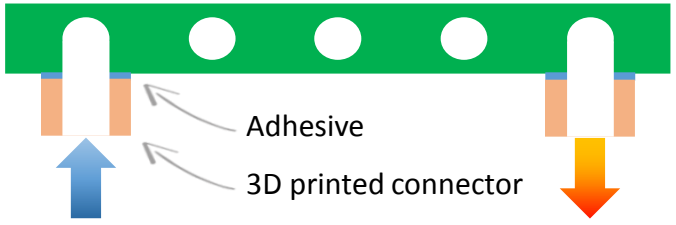
On going research at CERN (on monolithics)

Low temperature wafer bonding



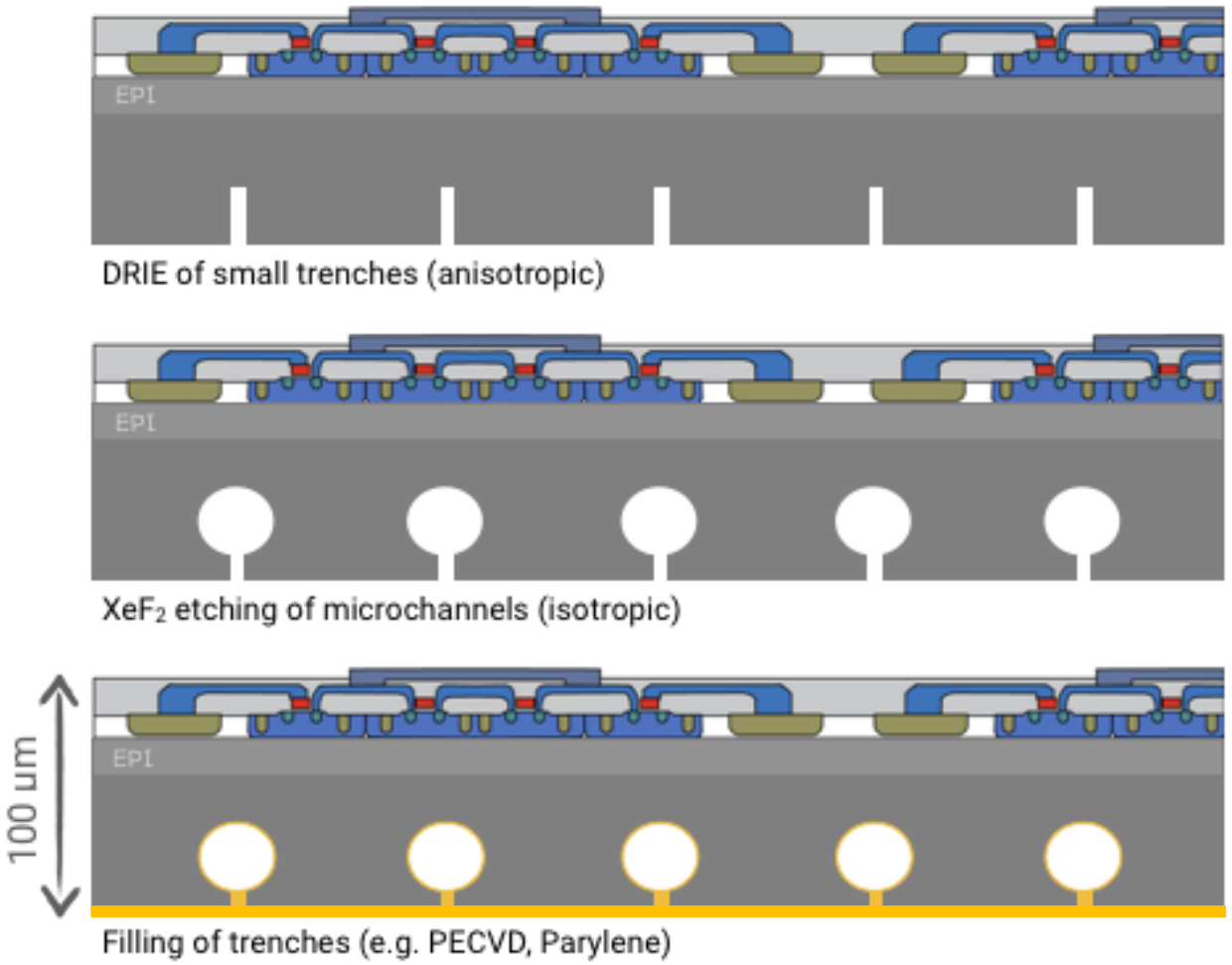
J. Bronuzzi, *Transient Current Technique characterisation of bonded interfaces for monolithic silicon detectors*, PhD Thesis, EPFL, 2018

Microchannels embedded in CMOS device



R. Callegari, *Integration of a microfluidic circuitry in a CMOS device operating in HEP experiments*, MSc Thesis, Università di Genova, 2018

MICROCHANNELS ETCHED DIRECTLY ON THE BACKSIDE OF A MONOLITHIC PIXEL DETECTOR (MALTA: MONOLITHIC FROM ALICE TO ATLAS)



A pattern of small trenches (3 x 10 µm) is etched on the backside of the pixel detector to a depth of 30 µm

Microchannels are etched isotropically with XeF2 from the bottom of the trenches.
Diameter of the microchannels = 40 µm
Overall depth of the microfluidic circuitry = 50 µm

A thin film of parylene (5 µm) seals the microchannels.
It is finally cured by a thermal cycle.

I. Berdalovic et al., *Monolithic pixel development in TowerJazz 180 nm CMOS for the outer pixel layers in the ATLAS experiment*, JINST 13 C01023, 2018

MICROFLUIDIC CONNECTION

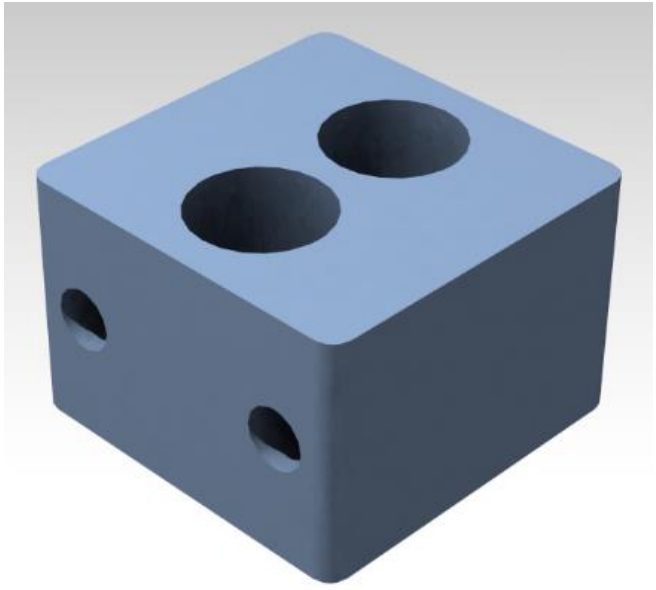
https://indico.cern.ch/event/677272/contributions/2976453/attachments/1638722/2615654/AIDA2020_connectors.pdf

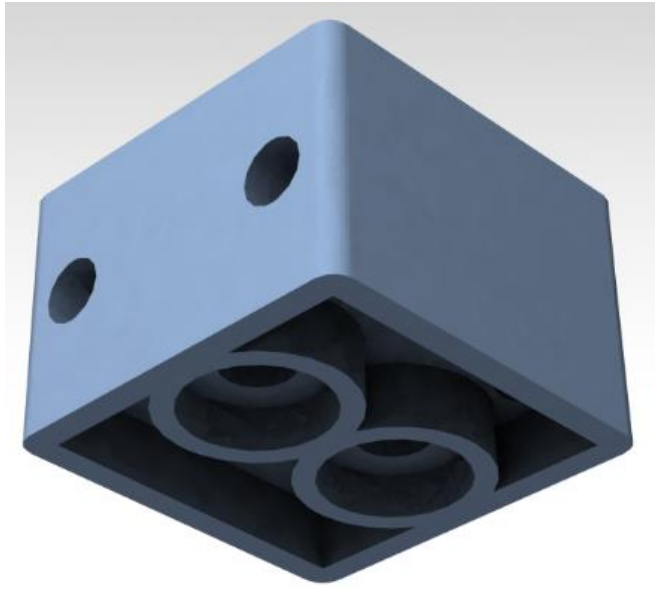
3D printed with Formlabs SLA:

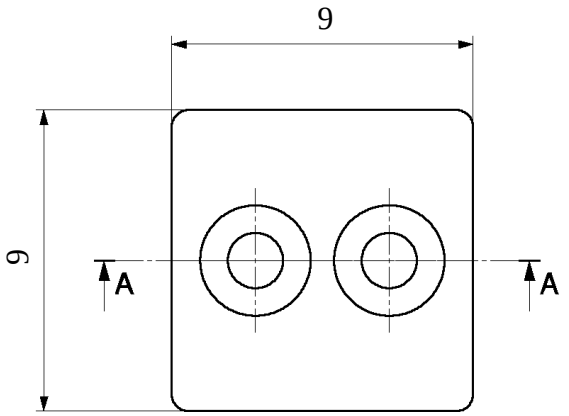
- Cheap
- Fast
- Easy
- Shapes difficult to achieve with conventional machining

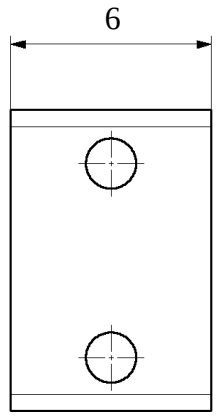
But…

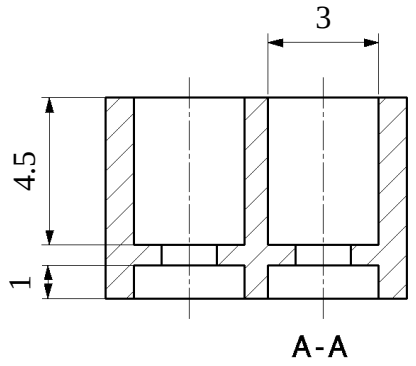
- Lack of dimensional repeatability





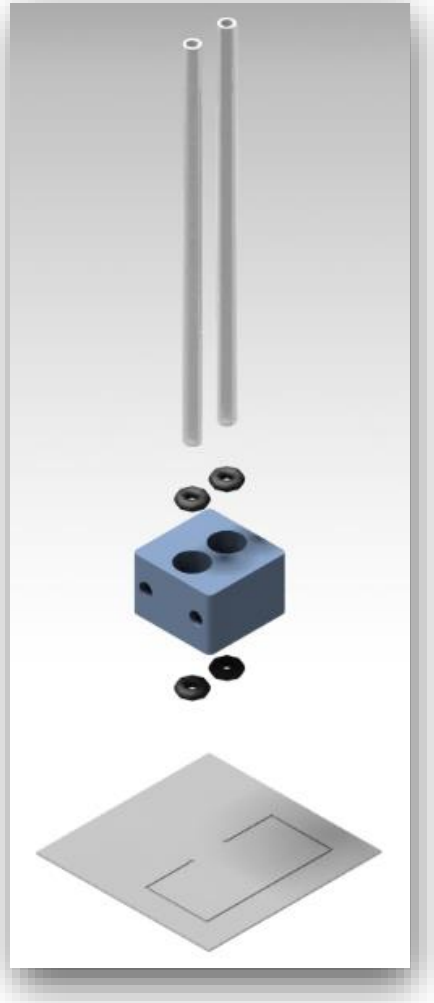


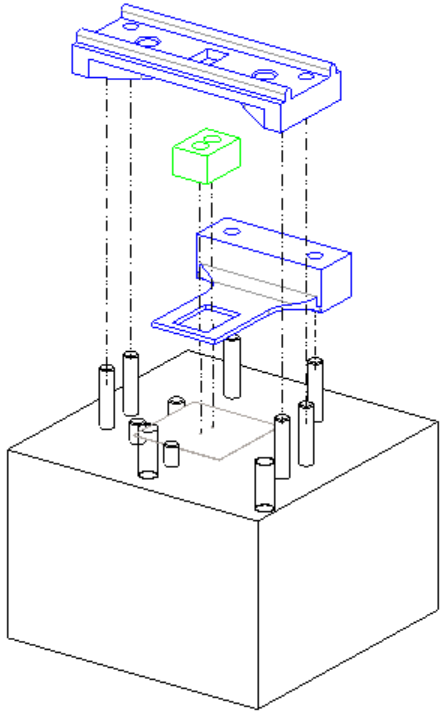




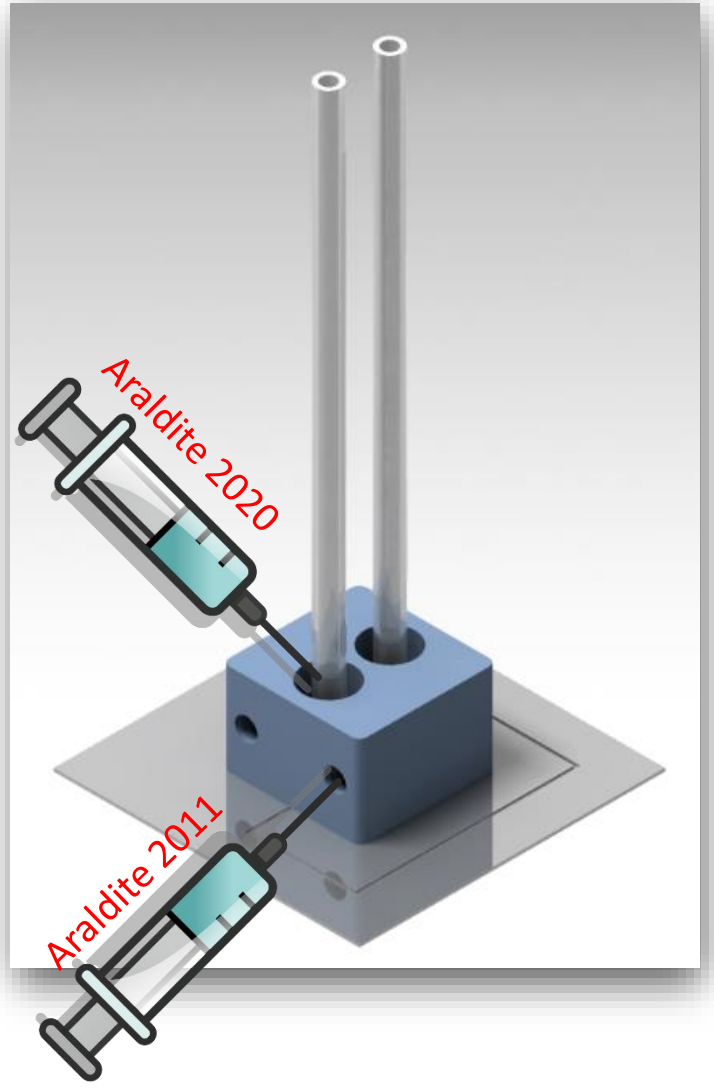
ASSEMBLY PROCEDURE

- The plastic capillaries are glued to the connector
- The connector is glued to the silicon chip
- Bottom o-rings prevent liquid leakages
- Top o-rings prevent glue infiltration





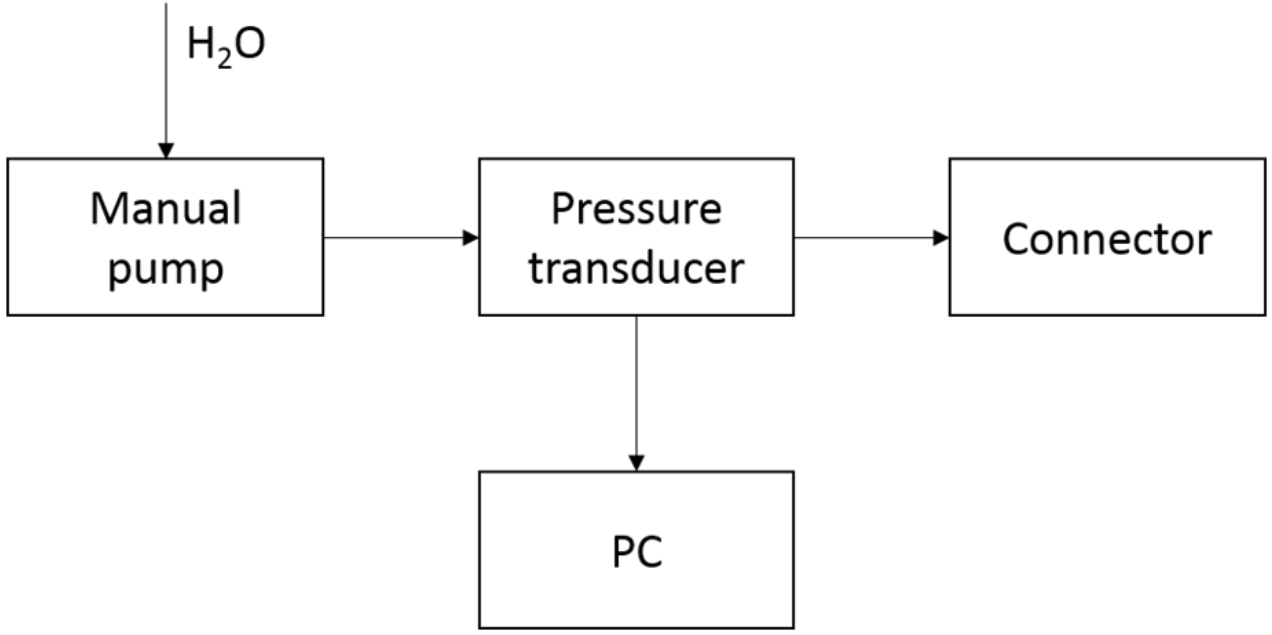
- Blue parts: 3D printed
- Black parts: machined
- Green part: connector (3D printed)



CONNECTOR CHARACTERIZATION

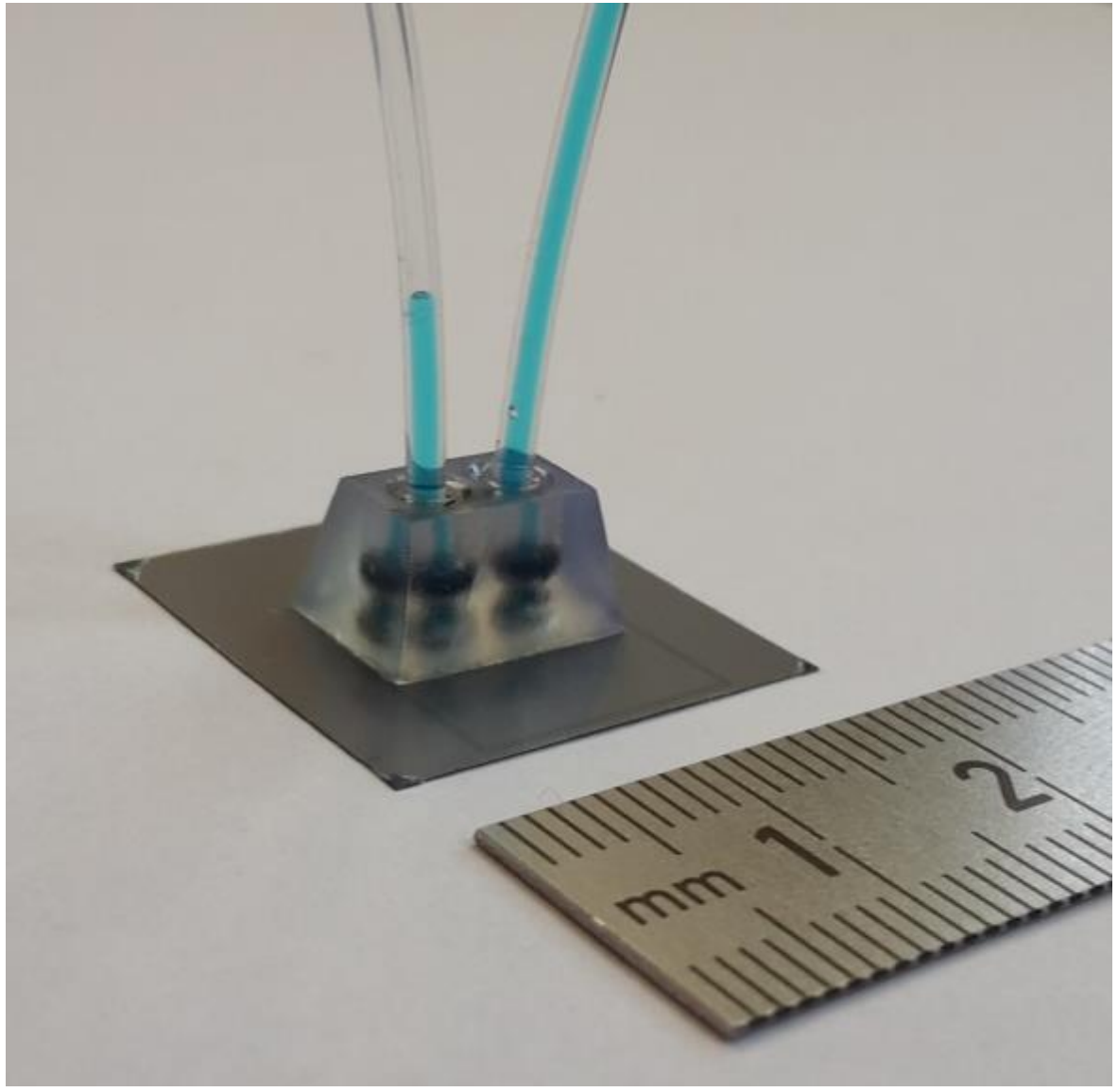
Connector glued on a blank piece of silicon:

- Helium leak rate: $L_{He} \approx 10^{-8}$ mbar · l / s
- Failure pressure: $p_{max} = 110$ bar



CIRCULATION DEMONSTRATED

Microchannels and connector integrated into a 100 µm thick CMOS device



A fully CMOS-compatible microfabrication process to embed microchannels has been validated

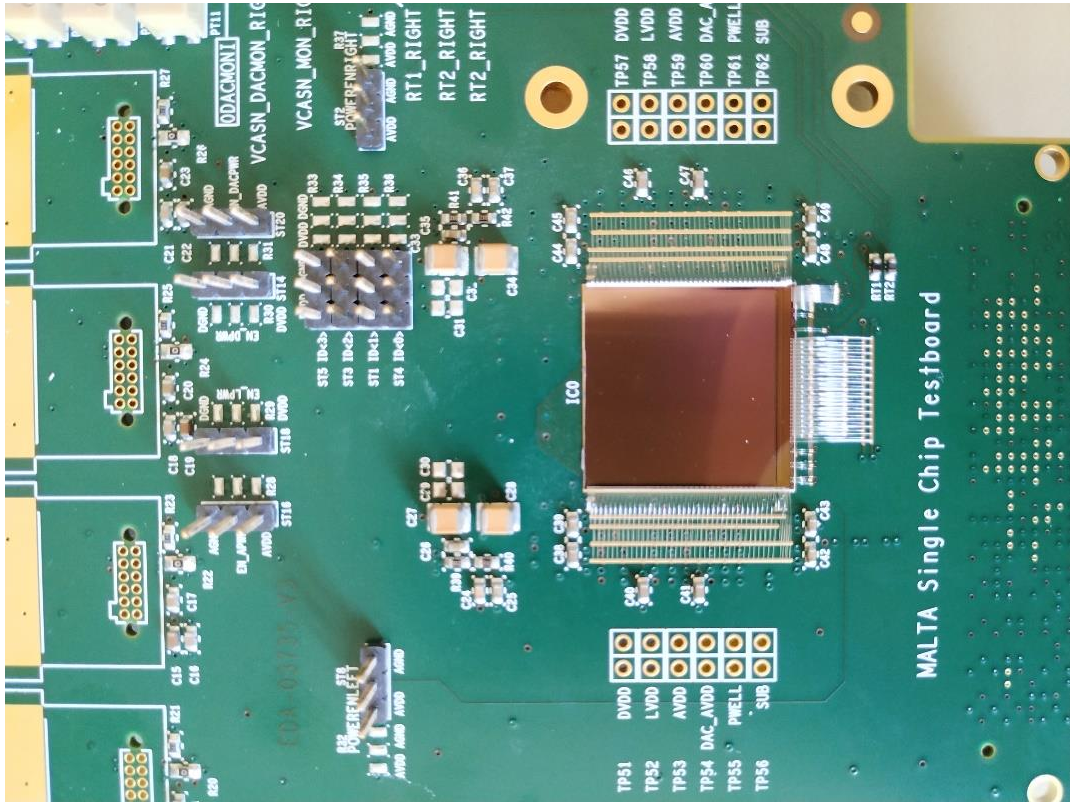
- As a post-process
- At a die level
- In an extremely thin substrate
- In an operating device

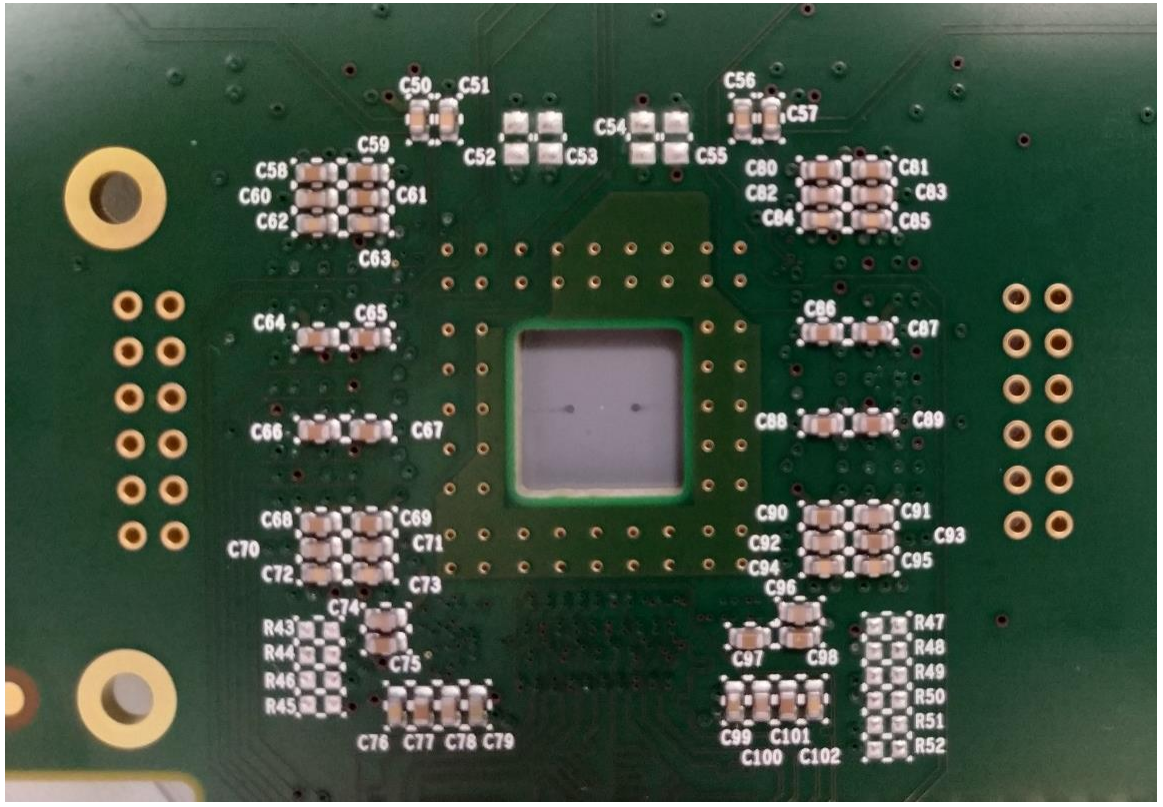
INTEGRATION WITH THE PCB (ONGOING)

First line of investigation:

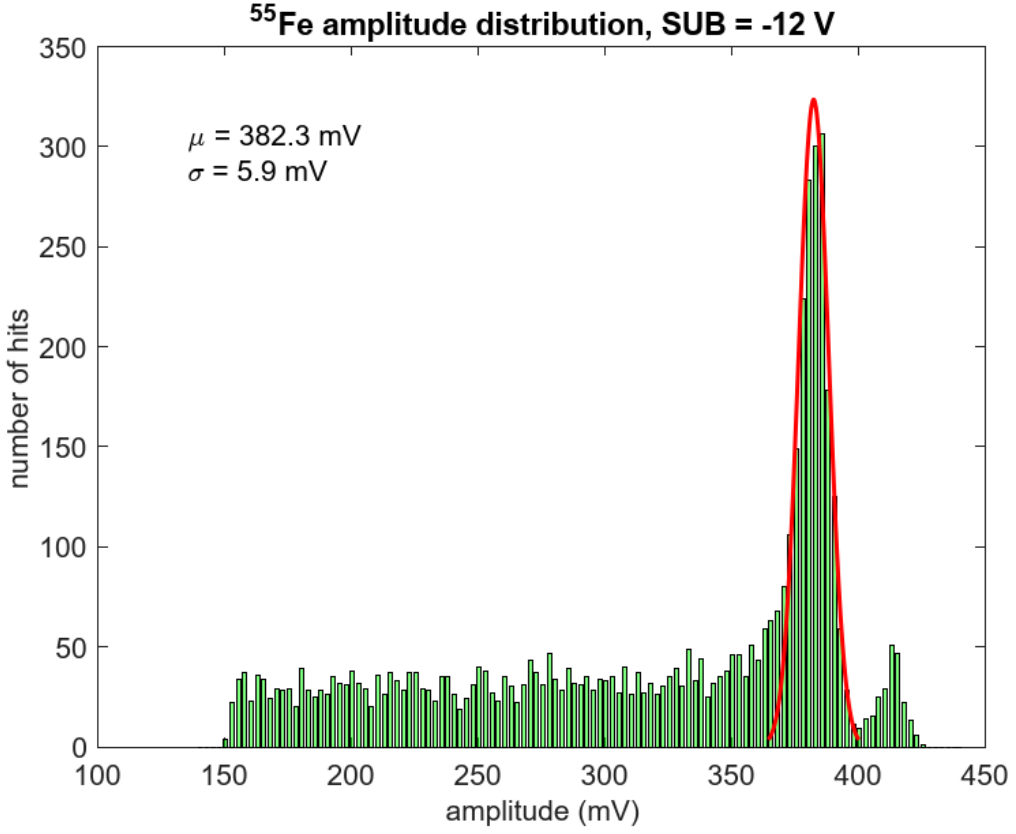
- Characterisation of a fully functional MALTA pixel chip with embedded micro channels to study possible effects of the post-processing

The first MALTA chip with embedded micro channels (without connectors) has been mounted on a PCB and wire bonded





IRON SOURCE SCAN (PRELIMINARY)



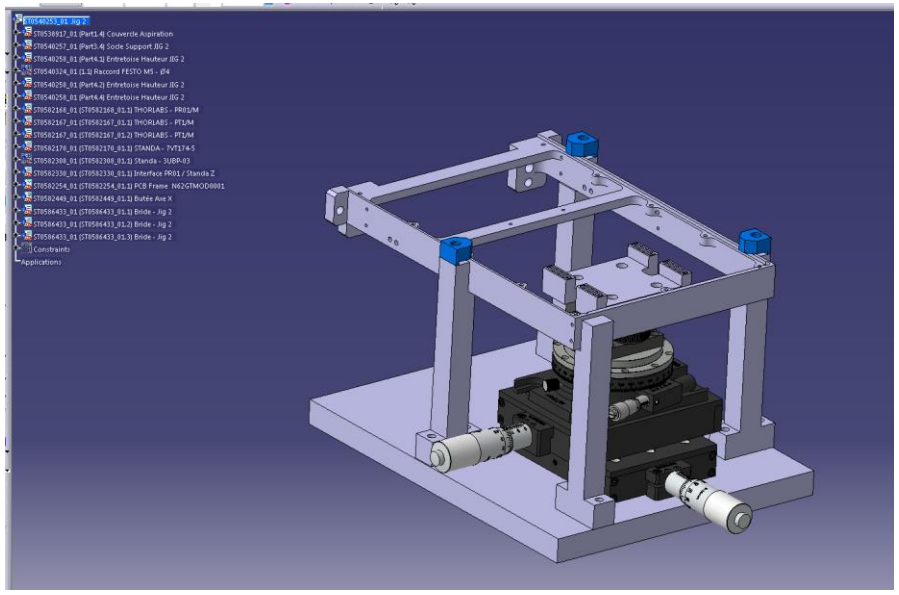
Preliminary electrical tests and source scans using a 55Fe source show a similar behaviour as in standard MALTA chips. Further tests are planned in the near future including measurements in a testbeam

INTEGRATION WITH THE PCB (ONGOING)

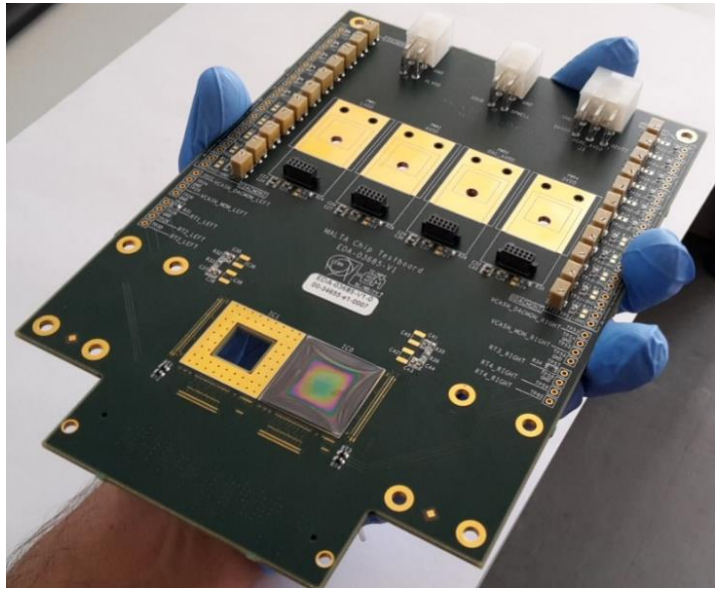
Next step:

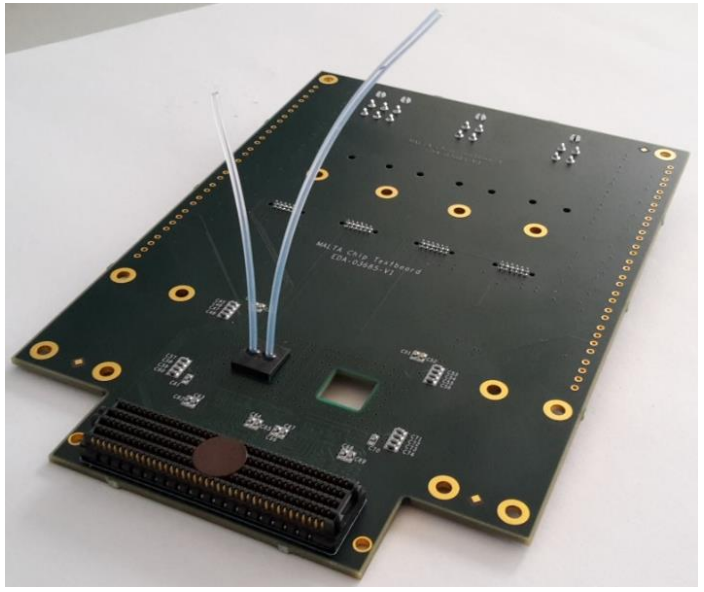
- Thermo-fluidic measurements for on-detector cooling

Helium leak rate: $L_{He} \approx 10^{-7}$ mbar · l / s



Alignment jig of the GTK for NA62





To be able to perform the wire bonding over an assembled chip a jig is required (under development).

Three axis translation stages + rotation

A tailor-made clamp for the connector has to be designed

CONCLUSIONS

A CMOS-compatible microfabrication process to embed microchannels into microelectronics has been developed. It allows to minimize more and more the overall thickness, getting rid of any thermal interface between the electronics and the cooling system.

A 3D printed microconnector, with the purpose of a test vehicle, has been validated. Optimization is required to reduce the amount of material.

Electrical, thermal and fluidic characterizations are ongoing.