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High data-rate readout logic design for 1024*512 CMOS pixel array dedicated for CEPC experiment

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CMOS Pixel Sensors (CPS) are attractive for CEPC vertex detector construction due to its high granularity, high speed, low material budgets, low power and potential high radiation tolerance. For the innermost layer of CEPC vertex detector, the expected resolution is 3 to 5 μm; the bunch spacing of CEPC vertex detector is 680 ns for Higgs, 210 ns for W and 25 ns for Z; the hit density is 2.5/bunch/cm2 for Higgs and W, and 0.2/bunch/cm2 for Z. As a result, the maximal hit rate is about 40 MHz in case of W for a pixel array of 1024×512 with 25 μm pitch. Suppose the average cluster size is 3 pixels, the data rate is near 120 MHz. In addition, in order to achieve a detection efficiency of 99%, the dead time for the pixel readout is about 500 ns assuming the pixel occupancy of 0.05%. The existing CMOS sensors such as ALPIDE, ATLAS-MAPS, MIMOSA and so on can not fully satisfied the requirements. Therefore, the CEPC MOST2 vertex detector design group propose a new readout architecture for CPS chip [1]. In the new architecture, the hit pixel addresses in a double column are read out based on the data-driven scheme such as FEI3 [2] and ALPIDE [3], and all the double columns of pixel array are read out parallel. In order to reduce the output data rate of the chip, the timestamp is recorded at the end of the double column, and the data with matched timestamp are buffered for output in case of trigger mode. Considering the chip test, the triggerless mode is also supported. This paper will focus on the peripheral readout logic design of the CPS chip with such high data rate for CEPC.

The overall architecture of the peripheral readout includes two level FIFOs. The first level FIFO is used to store the pixel addresses temporally for each double column and the FIFO depth is 12 to 16 considering the data rate and the deadtime. The second level FIFO is used to match the readout speed of chip interface and there are four FIFOs with depth of 256. In the periphery logic design, we adopt three strategies to fulfill the readout requirements. Firstly, 32 double columns are organized as a group for address priority readout and a special token readout method is proposed between these blocks for realizing the data-driven in the group and avoiding some groups are blocked for a long time. Secondly, both the trigger and the triggerless readout modes are supported in order to suppress the data with unmatched timestamps in trigger mode and to read out all the data in triggerless mode. Thirdly, advance data compression is realized before being written into FIFO1 in order to increase the design capability and reduce the power consumption.

The readout logic of 1024×512 pixel array has been realized in 0.18 μm Tower Jazz process. The area is 25.68 mm×1.13 mm. The simulation results indicate the readout logic work well with an input data rate of 120 MHz in case of disabling the advance data compression. When the data compression is enabled, higher data rate can be supported. A reduced scale chip with 192×64 pixel array is planned to be submitted on May 2019 for evaluation the chip architecture and block circuits.

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