FRIC - a 50 µm pixel-pitch single photon counting ROIC with Pattern Recognition algorithm in 40 nm CMOS technology

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Agenda

1. Motivation
2. ROIC architecture
3. Measurement results
    1. On-chip calibration
    2. X-ray exposure
4. Summary

Motivation

High granularity hybrid single photon counting pixel detector for operation with monochromatic radiation (e.g. synchrotron radiation).

Certain implications:

High granularity detector with 50 um pixels suffers from charge sharing effect

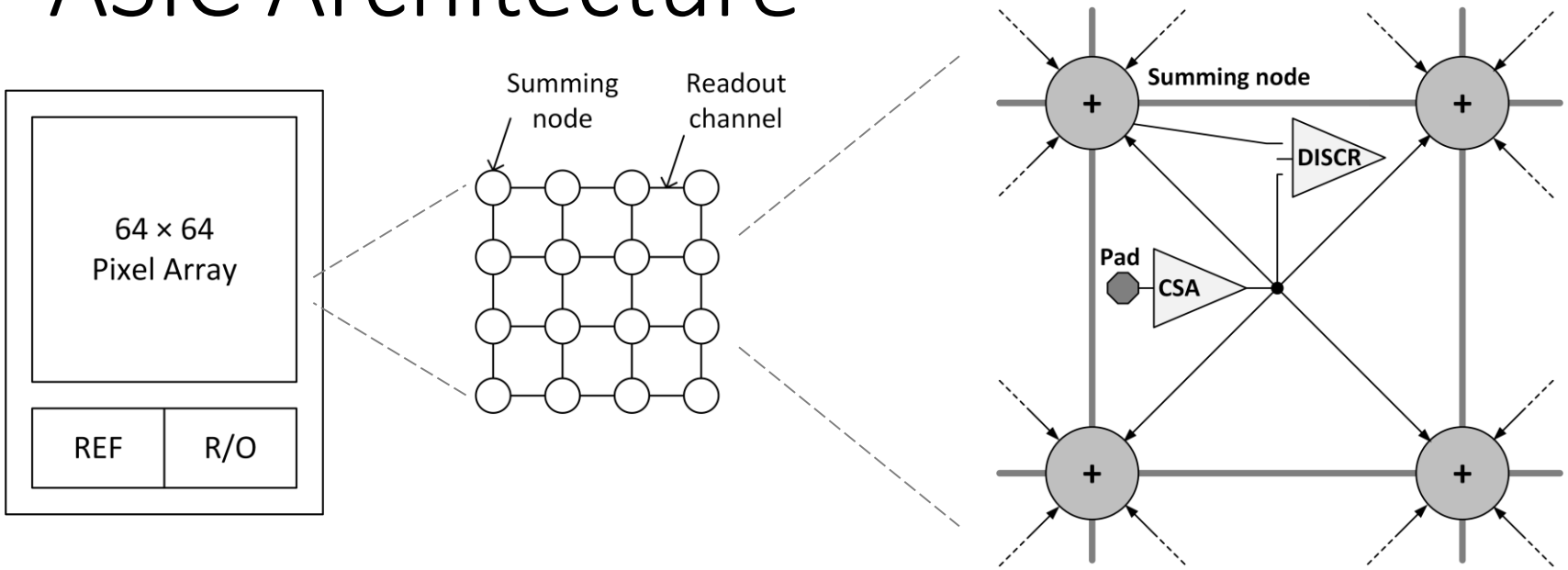
For time-resolved experiments with monochromatic radiation the uncertainty of threshold setting decreases the contrast

Implementation of a charge-sharing compensation algorithm

Compensation algorithm rises noise and decrease count rate due to charge summing

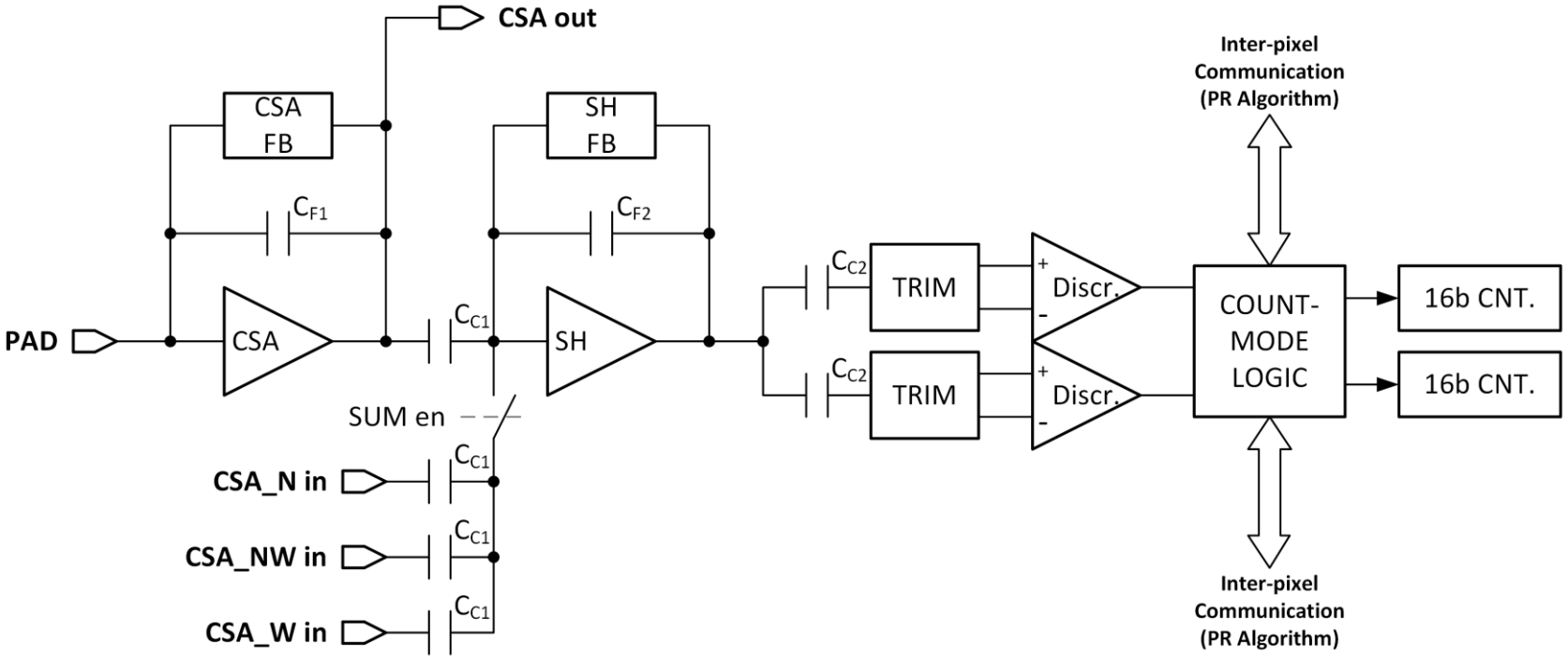
IC should be optimized for high count rate and low noise operation

ASIC Architecture

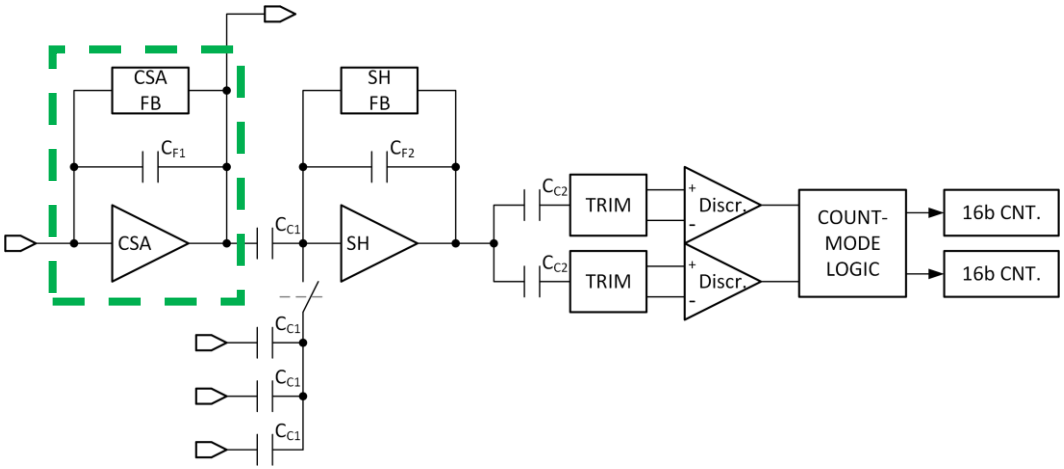


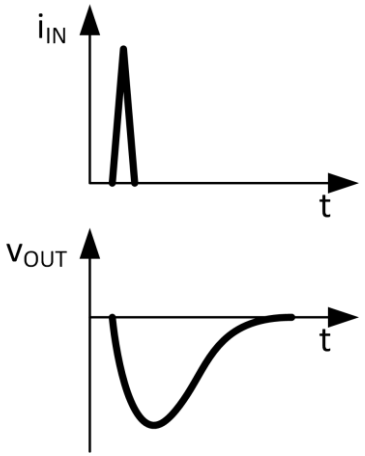
- Matrix size of 64 × 64 pixels with pixel pitch of 50 µm
- Signal summing with Pattern Recognition algorithm for charge sharing correction
- Two 8-bit threshold DACs
- External gate signal for short, precisely timed exposure window
- All control signals in LVDS standard
- 40 nm CMOS technology

Channel architecture



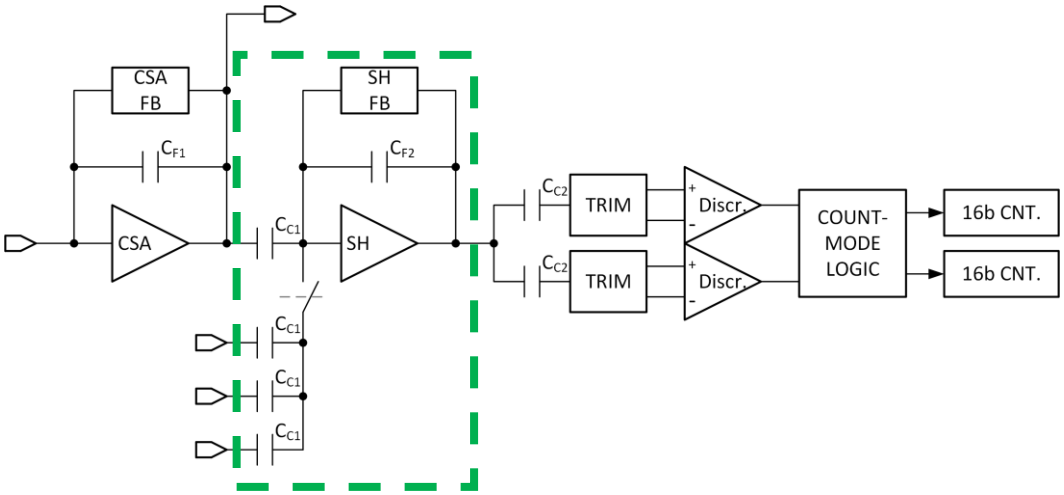
Channel architecture – 1st stage (CSA)

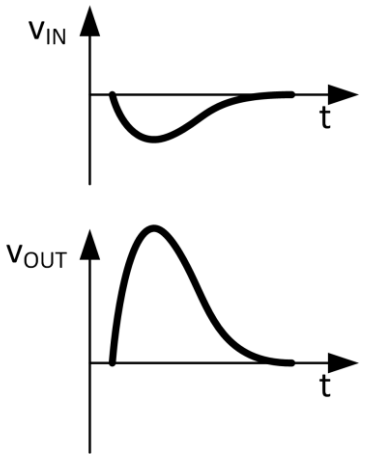




- Input stage operating in transimpedance mode, with short time constant
- Amplifier core based on inverter
- Fixed feedback capacitance C_{F1}
- Globally regulated feedback resistance, affecting gain and pulse time

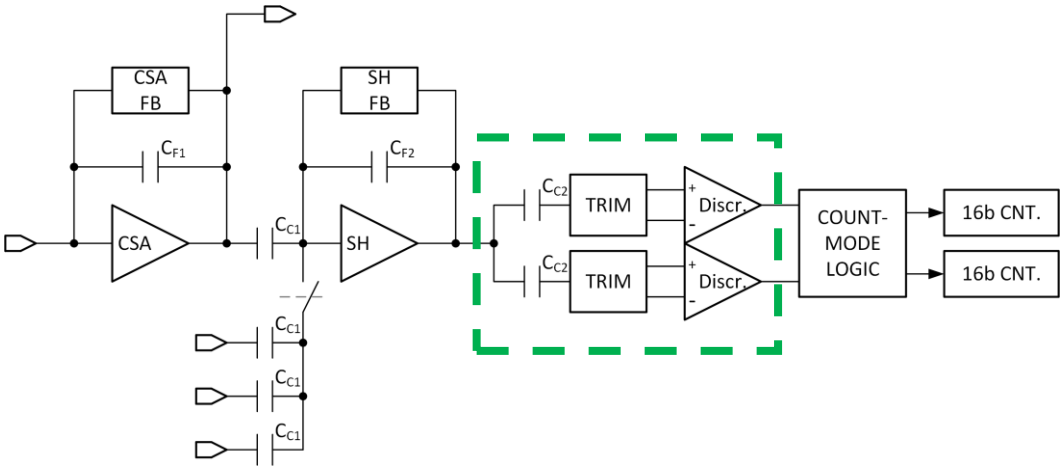
Channel architecture – 2nd stage (shaper)

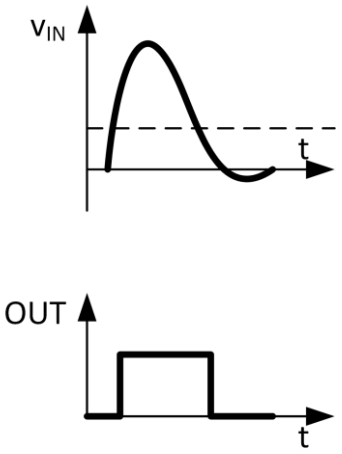




- Second stage operating as voltage amplifier, with very long time constant
- Amplifier core based on inverter
- Fixed gain of $\frac{C_{C1}}{C_{F2}}$
- Realizes summing of signal from four adjacent pixels

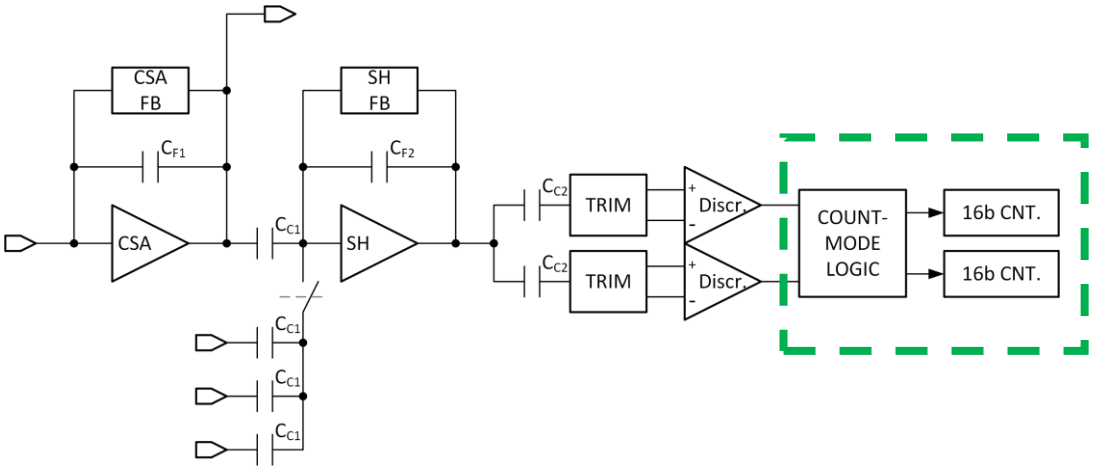
Channel architecture – discriminator

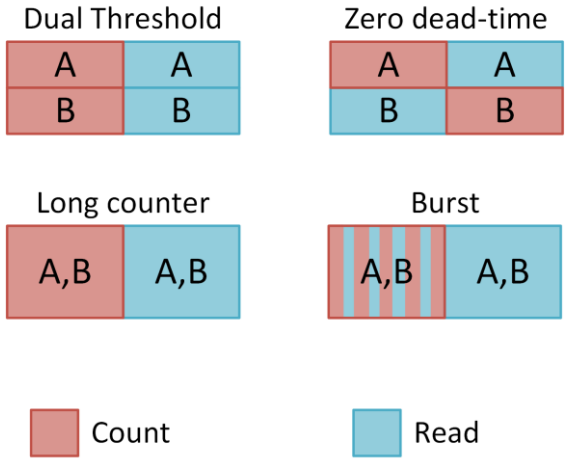




- Two high-speed discriminators with independent thresholds
- 5-bit trimming DACs

Channel architecture – digital back-end



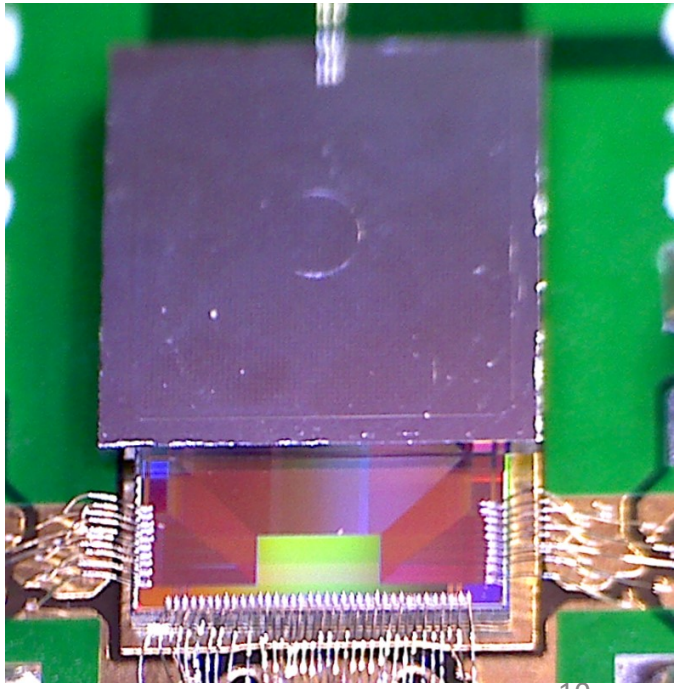


- Conventional Single Photon Counting or Pattern Recognition algorithm
- Two independent 16-bit counters
- Supported modes: dual threshold, long counter, zero-dead time readout, burst

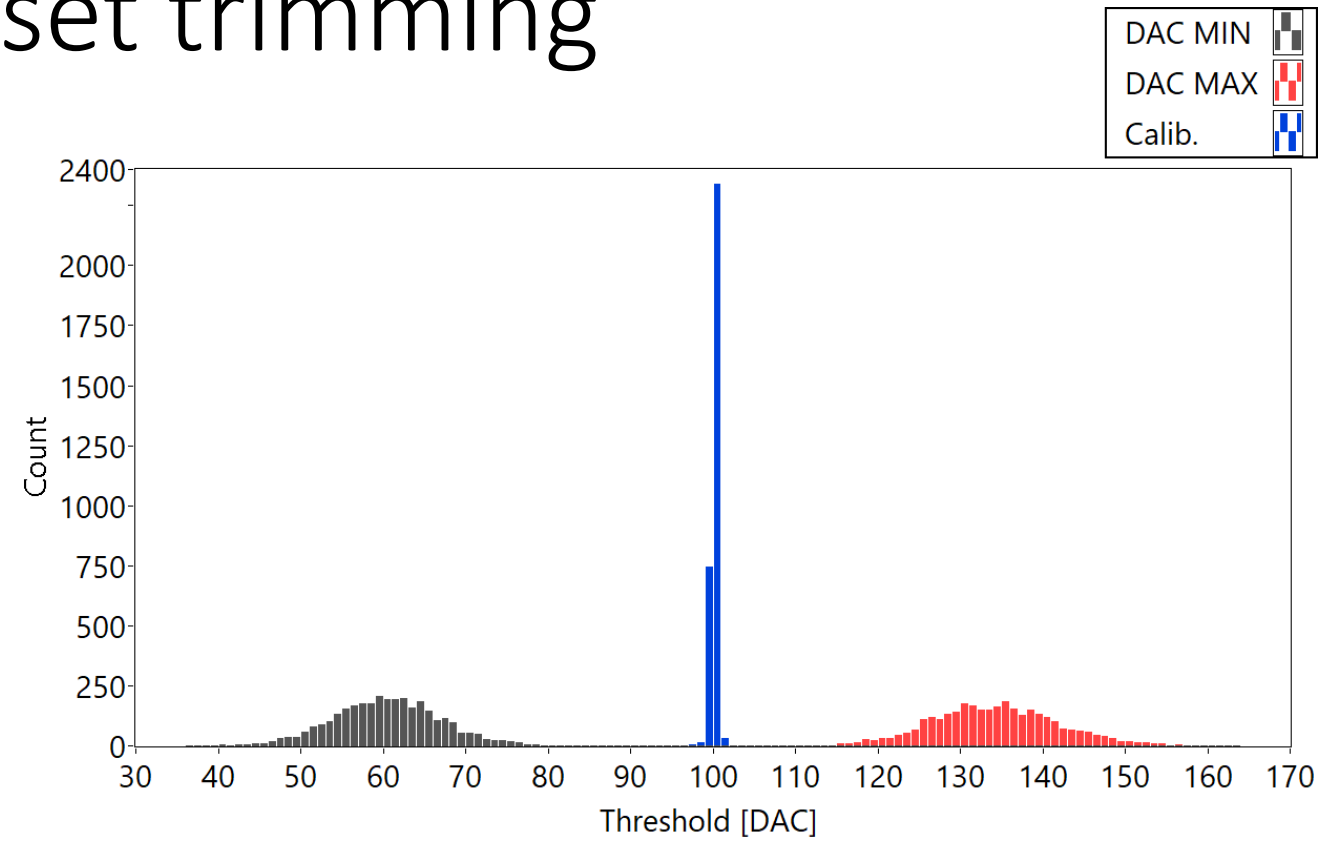
On-chip calibration – measurement setup

- Supply voltage – 1.05 V
- Two analog FE bias settings – High Gain and High Speed

- Chip bonded to 0.32 mm Si detector
- Detector bias ~ 180 V



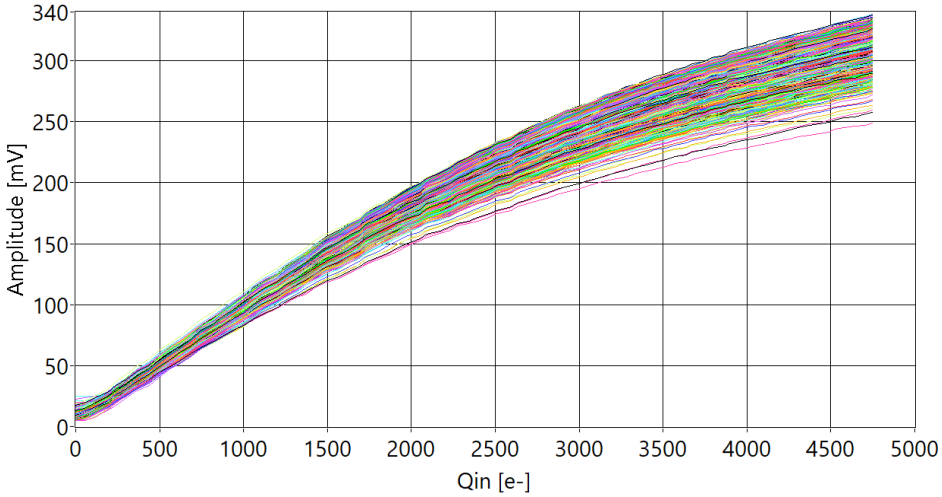
Offset trimming

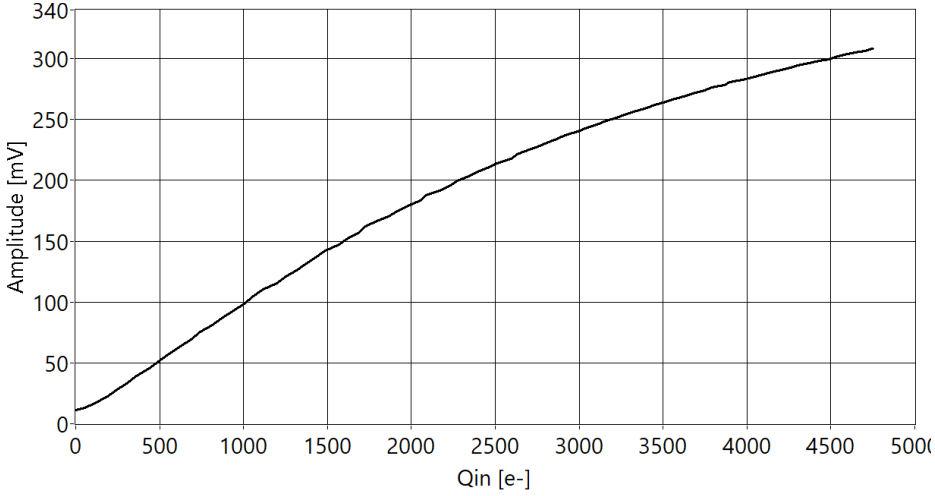


	DAC MIN	Calibrated	DAC MAX
Mean	60,4	100,1	134,2
Standard dev.	6,4	0,34	7,5

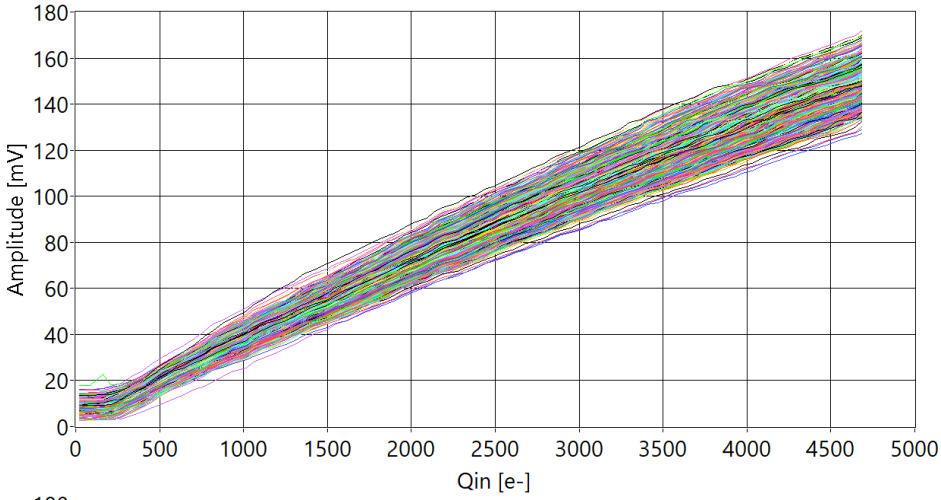
Linearity

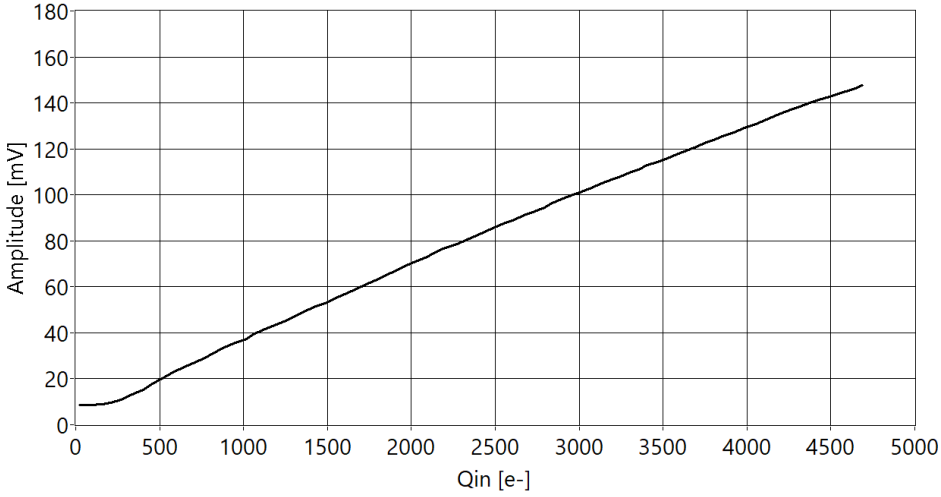
High Gain



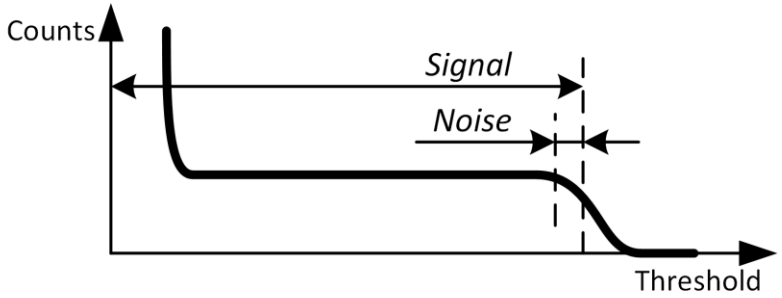


High Speed

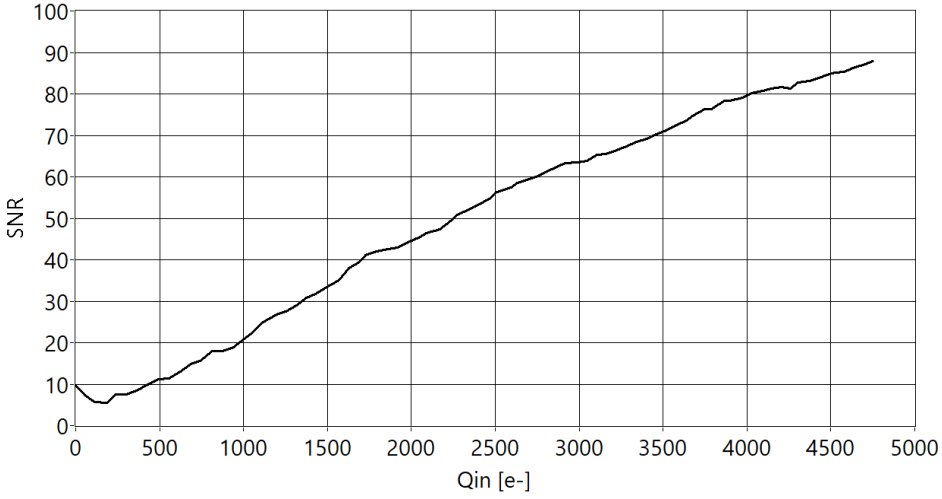




Signal-to-noise ratio

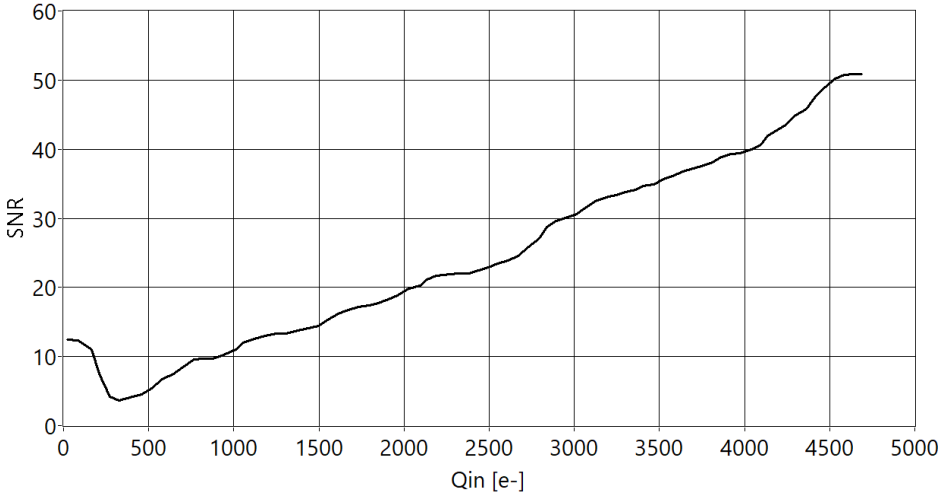


High Gain



rms noise @ 8 keV ≈ 50 e$^-$

High Speed

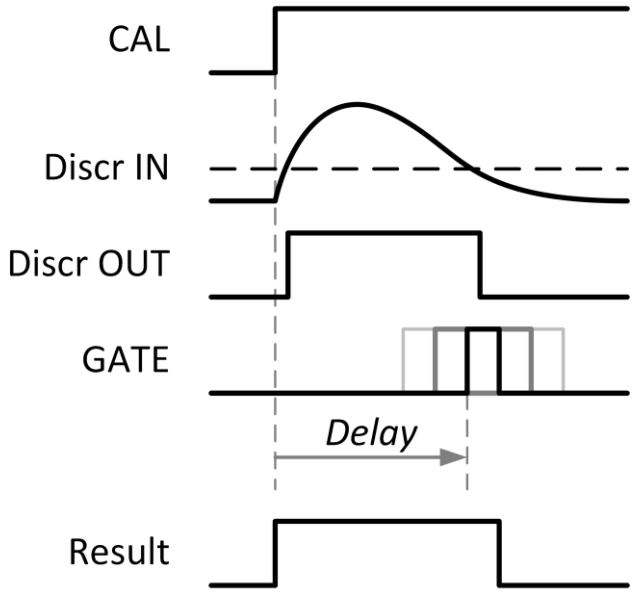


rms noise @ 8 keV ≈ 100 e$^-$

FE dead-time – method description

Pulse length measurement :

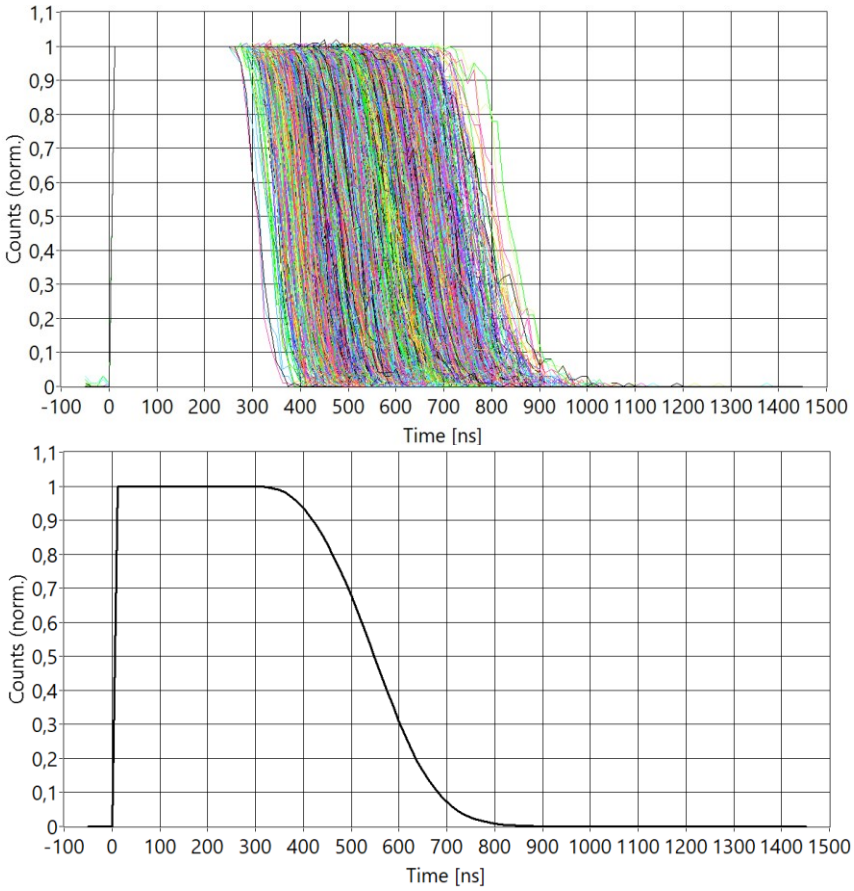
1. Send a calibration pulse.
2. Wait a predetermined delay time.
3. Send a short gate strobe. Depending on discriminator output, the counter is incremented or not.
4. Repeat steps 1-3 and readout the counter data.
5. Increment the delay time and repeat steps 1-4.



- Discriminator's output is sampled by gate signal level, not its edge - the measured pulse length will always be longer than an actual one
- Gate strobe length – **12,5 ns** (f_{CLK} = 80 MHz)

FE dead-time

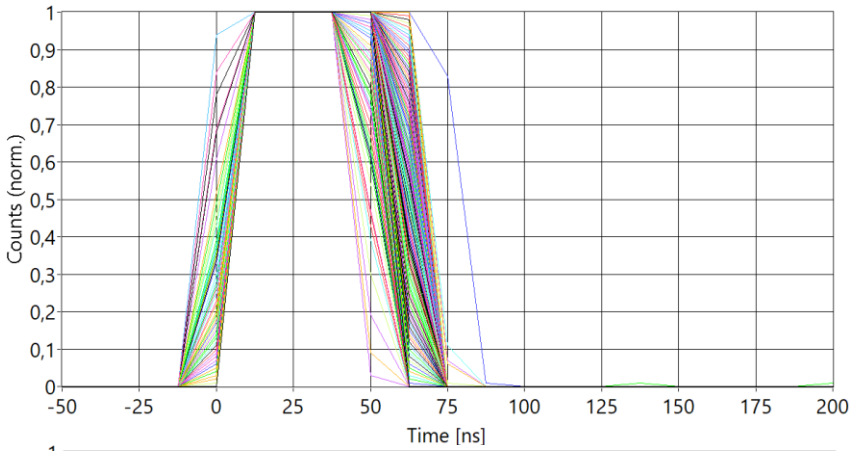
High Gain

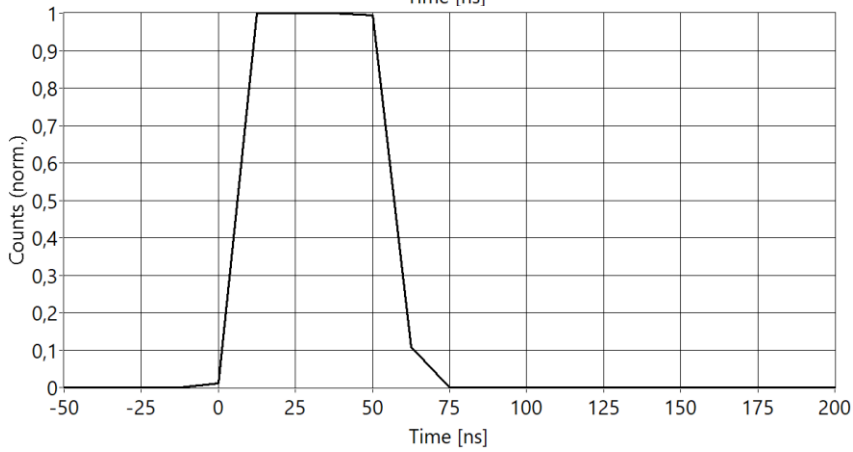


Average FWHM pulse length = 550 ns

@ TH = 10% pulse amplitude

High Speed

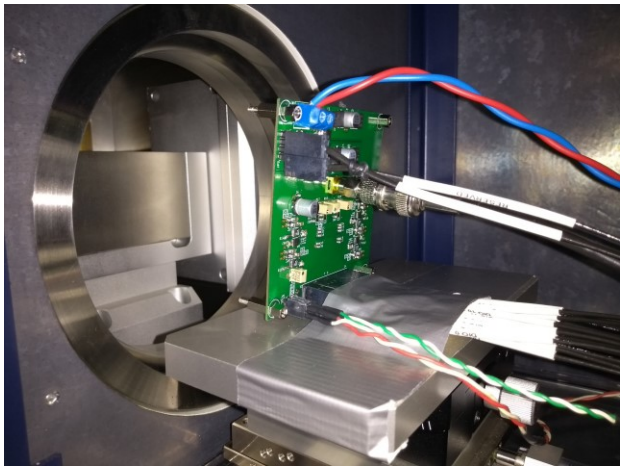




Average FWHM pulse length = 50 ns

@ TH = 24% pulse amplitude

X-ray measurements – experimental setup



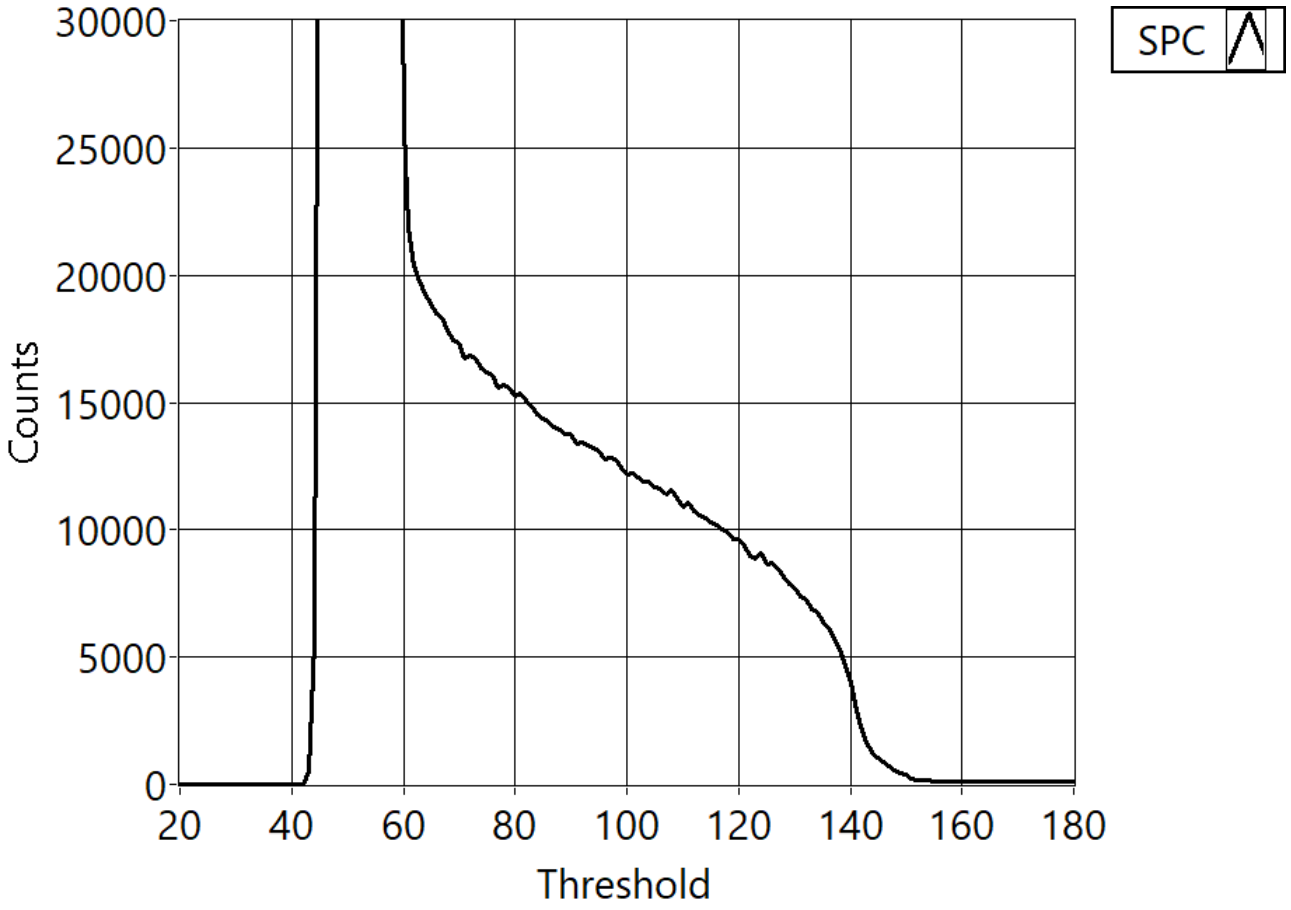
- Exposed to 8 keV X-rays (Cu target)
- Exposure time – 10 s / frame

- Only on-chip DACs used for bias setting
- No forced cooling

X-ray measurements – threshold scan

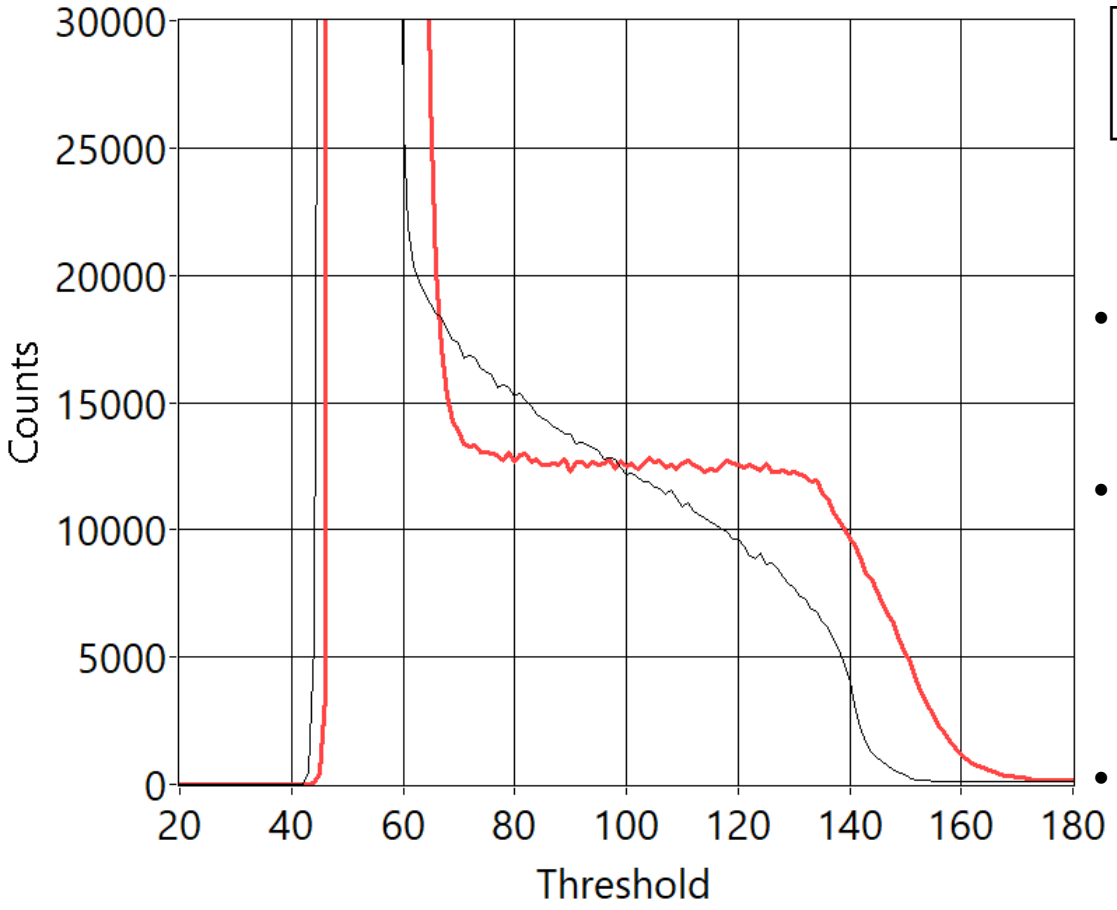
High Gain mode –

Conventional Single Photon Counting mode



X-ray measurements – threshold scan

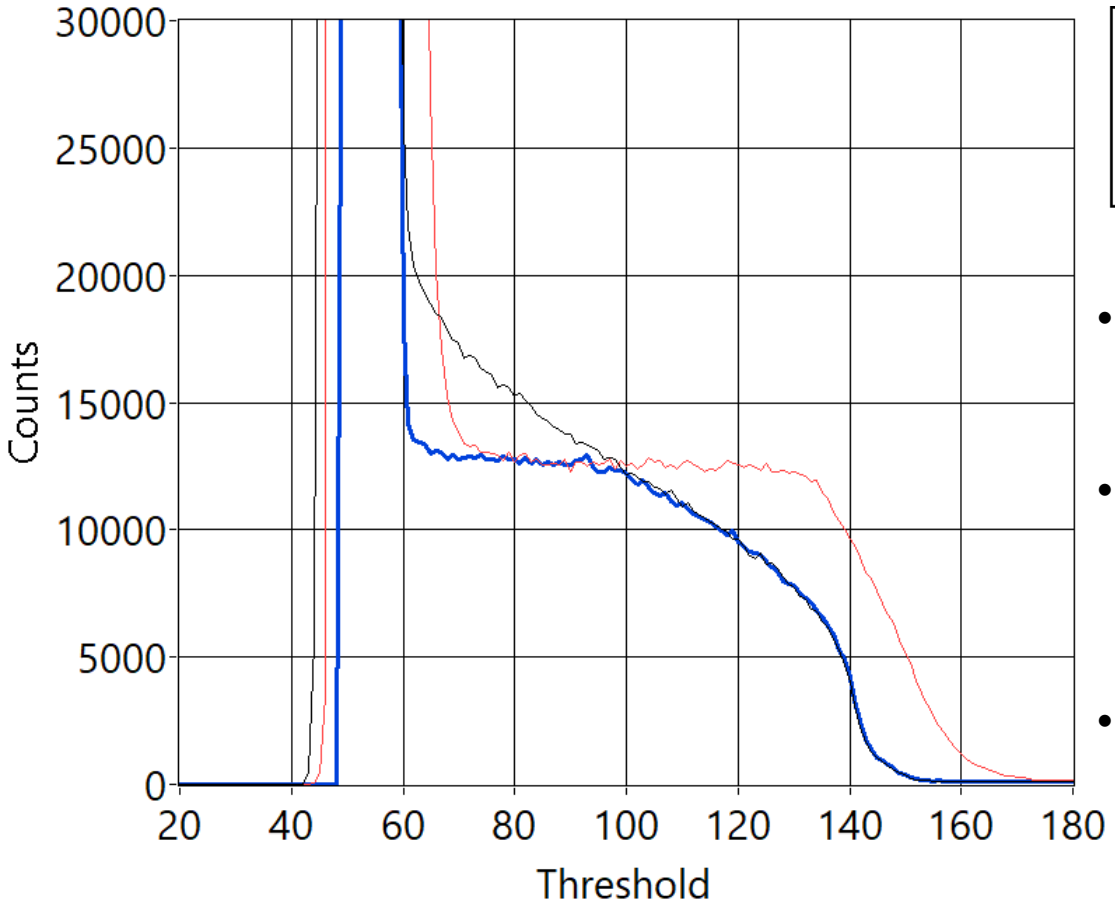
High Gain mode –
Signal summing + Pattern Recognition



- Number of counts is constant for wide threshold range.
- Signal amplitude information distorted because of gain mismatch of four contributing pixels.
- Noise increase.

X-ray measurements – threshold scan

High Gain mode –
Pattern Recognition only

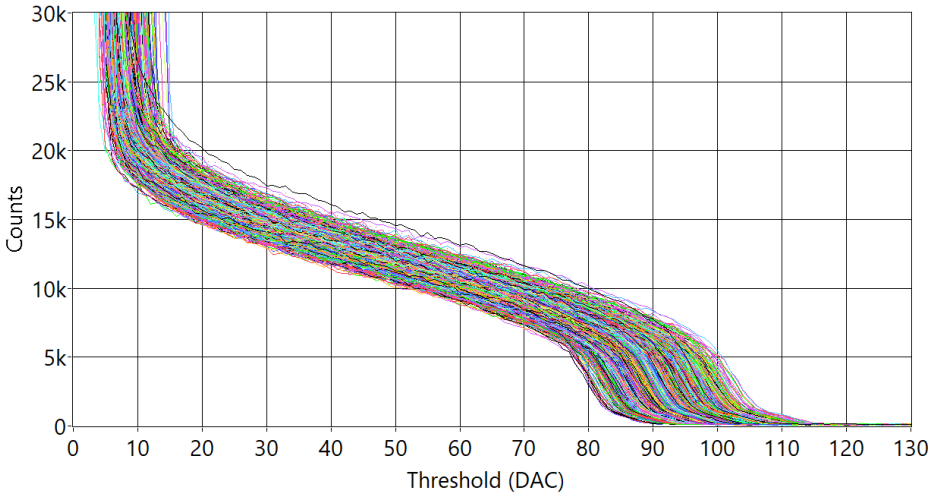


- Number of counts still nearly constant for wide threshold range.
- Signal amplitude information distorted because of charge sharing (as in SPC mode).
- Noise same as in SPC mode.

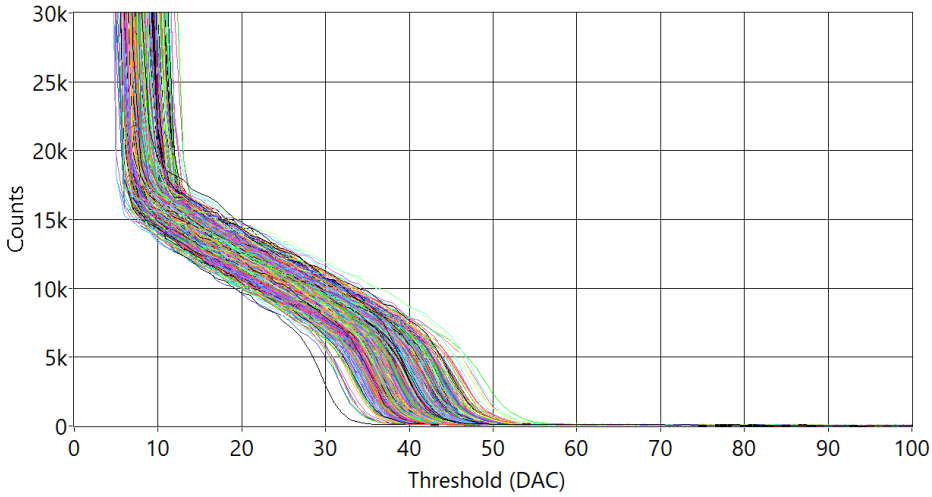
X-ray measurements – energy spectrum

- Off-chip offset and gain correction
- Conventional Single Photon Counting mode
- Averaged data from inner 56 × 56 pixels – 1 bad pixel = 3135 readout channels

High Gain

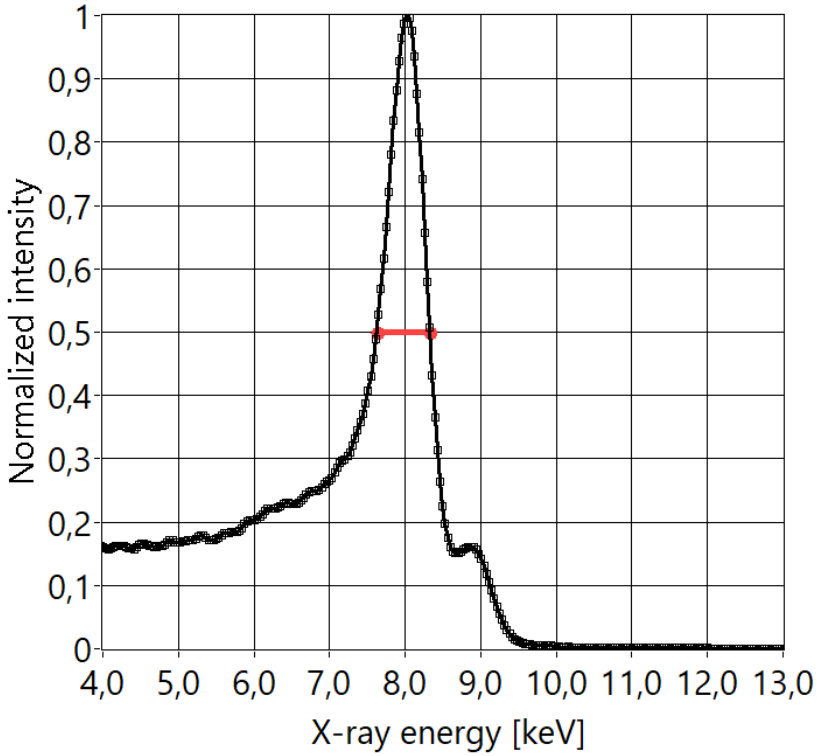


High Speed



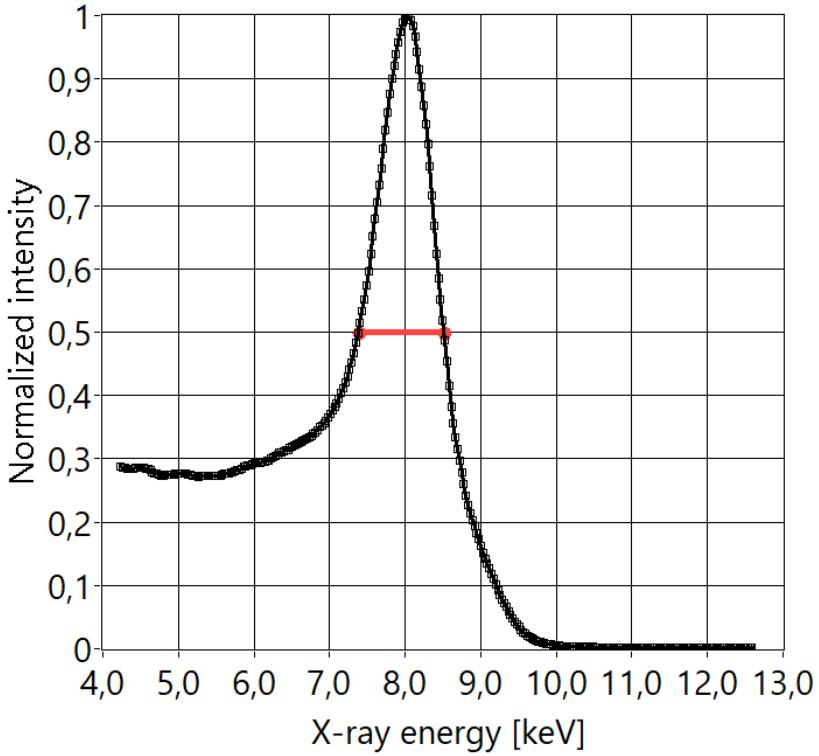
X-ray measurements – energy spectrum

High Gain



- FWHM – **0,71 keV**
- ENC – **84 e$^-$**

High Speed



- FWHM – **1,134 keV**
- ENC – **132 e$^-$**

Comparison with state-of-art

	FRIC		Medipix3RX [1]		IBEX [2]		UFXC32k [3]		PIXIE III [4]
Technology	**40 nm**		130 nm		110 nm		130 nm		160 nm
Array size	**64 × 64**		256 × 256		256 × 256		128 × 256		512 × 402
Pixel size (µm²)	**50 × 50**		55 × 55		75 × 75		75 × 75		62 × 62
CS correction	**Yes**		Yes		No		No		Yes
Power/pixel (µW)	**12**	**18**	7,5		7,4		26		-
FWHM (keV)	**0,71**	**1,13**	0,68 [a]	-	0,85	-	1,04 [c]	1,99 [c]	0,69 [d]
10% input loss count rate (Mcps/mm²)	**TBD**	**TBD**	50,5	81,7	-	230 [b]	-	220	-
FE Dead time (ns)	(550)	(50)	690	400	-	100 [b]	232	85	-

a) Estimated for Si, based on ENC (Ballabriga et al 2016 JINST 11 P01007)
b) Retrigger feature disabled
c) Estimated for Si, based on ENC
d) Calculated with calibration pulses

Summary

- Pixel pitch of 50 µm × 50 µm
- Energy resolution of FWHM = 0,71 keV @ 8 keV
- Estimated FE dead-time of 50 ns
- Pattern Recognition algorithm for charge sharing correction
- Power consumption of 12 µW / 18 µW per pixel
- Matrix size of 64 × 64 pixels

References

[1] E. Frojdh et al ”Count rate linearity and spectral response of the Medipix3RX chip coupled to a 300µm silicon sensor under high flux conditions,” 2014 JINST 9 C04028

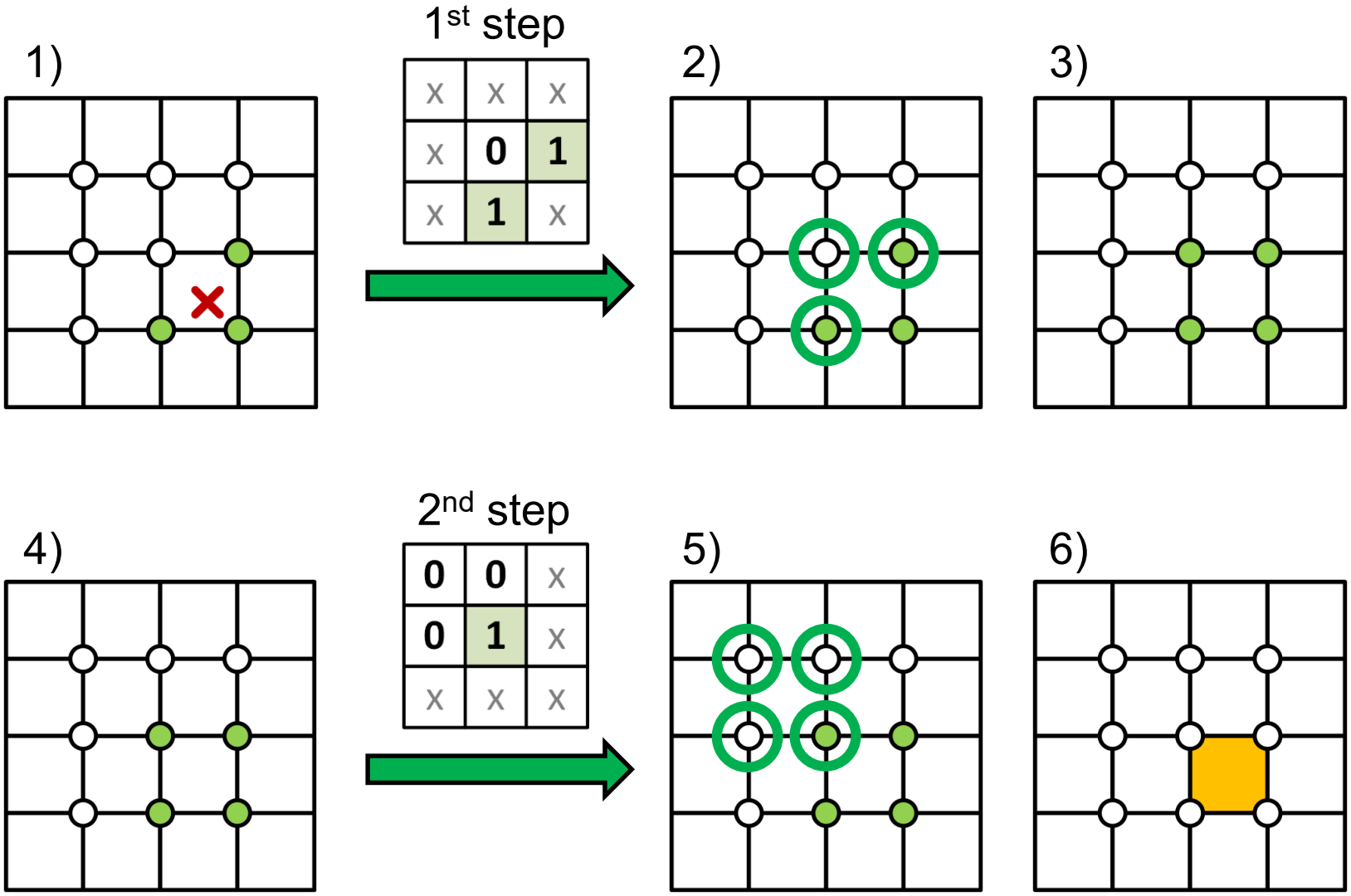
[2] M. Bochenek et al ”IBEX: Versatile Readout ASIC With Spectral Imaging Capability and High Count Rate Capability,” IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 65, NO. 6, JUNE 2018

[3] P. Grybos et al “32k Channel Readout IC for Single Photon Counting Pixel Detectors with 75 µ m Pitch, Dead Time of 85 ns, 9 e − rms Offset Spread and 2% rms Gain Spread,” IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 63, NO. 2, APRIL 2016

[4] R. Bellazzini et al "PIXIE III: a very large area photon-counting CMOS pixel ASIC for sharp X-ray spectral imaging,” 2015 JINST 10 C01032

Backup slides

Pattern Recognition



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