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FRIC - A 50 µm pixel-pitch single photon counting ASIC with Pattern Recognition algorithm in 40 nm CMOS technology

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This work presents the design and implementation details of a 64 × 64 pixel readout circuit designed at AGH UST. The analog front-end [1] is based on an inverter amplifier and uses a novel feedback topology, which allows for very short pulse-shaping times, while maintaining good gain linearity. Fine pixel pitch of 50 µm requires certain measures for charge sharing compensation. For that purpose, the presented circuit uses signal summing together with the Pattern Recognition algorithm [2-3]. The digital back-end composes of two independent 16-bit counters. Additionally, it supports a high-speed burst mode, which allows for sub-microsecond frame times.
The presented ASIC has been manufactured and is currently under tests. Preliminary measurement results will be presented on the conference.

Fig. 1. Layout of the designed ASIC, 64 × 64 pixels, 3.24 × 5.12 mm2.

1. X. Llopart, et al., “Study of low power front-ends for hybrid pixel detectors with sub-ns time tagging,” JINST 14 C01024
2. Piotr Otfinowski “Spatial resolution and detection efficiency of algorithms for charge sharing compensation in single photon counting hybrid pixel detectors,”Nuclear Instruments and Methods in Physics Research Section A, Volume 882, 21 February 2018, Pages 91-95
3. P. Otfinowski, G. W. Deptuch, P. Maj “Asynchronous Approximation of a Center of Gravity for Pixel Detectors’ Readout Circuits,”IEEE Journal of Solid-State Circuits, Volume 53, Issue 5, May 2018

Authors: OTFINOWSKI, Piotr (AGH University); DEPTUCH, Grzegorz (Fermi National Accelerator Lab. (US)); MAJ, Piotr (AGH University)

Presenter: OTFINOWSKI, Piotr (AGH University)

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