Prototype single-ended and pseudo-differential charge processing circuits for micro-strip silicon and gaseous sensors read-out

Weronika Zubrzycka, Krzysztof Kasinski

AGH University of Science and Technology,
Department of Measurement and Electronics
Av. Mickiewicza 30, 30-059 Cracow, Poland

zubrzycka@agh.edu.pl

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Background

The Compressed Baryonic Matter (CBM) experiment-one of the major scientific pillars of the future Facility for Antiproton and Ion Research (FAIR) in Darmstadt

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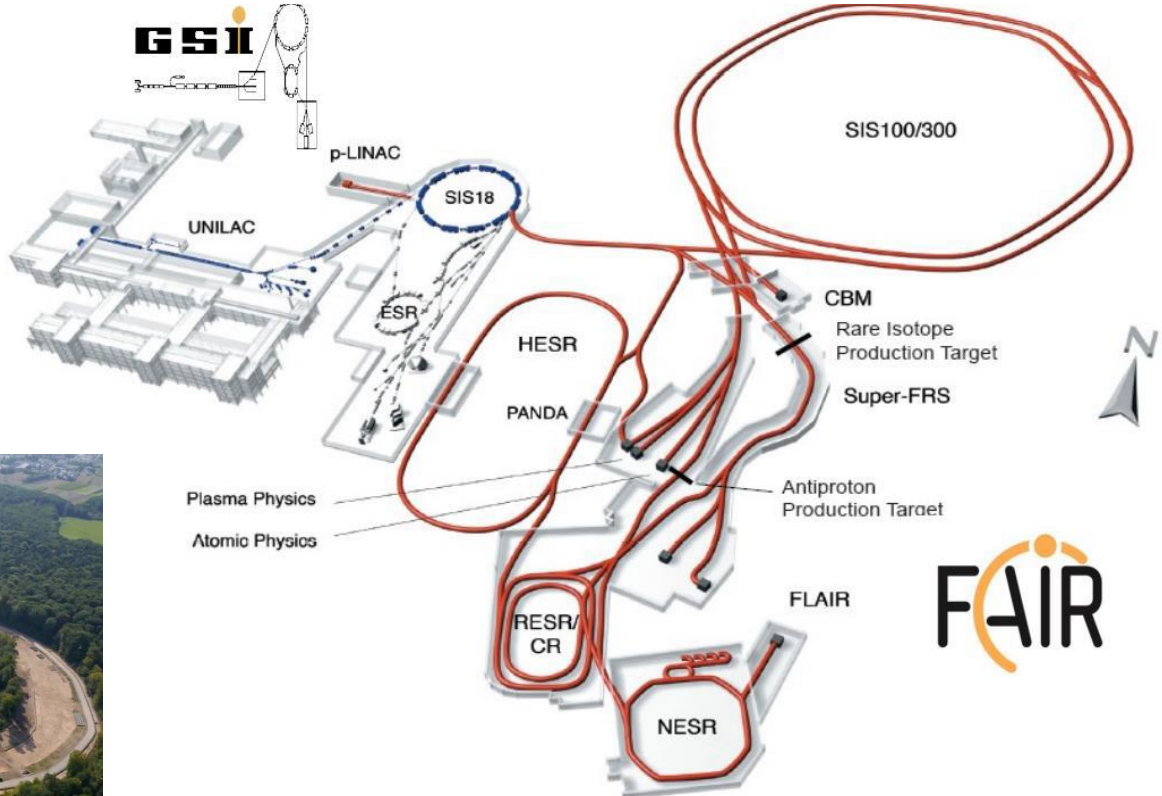
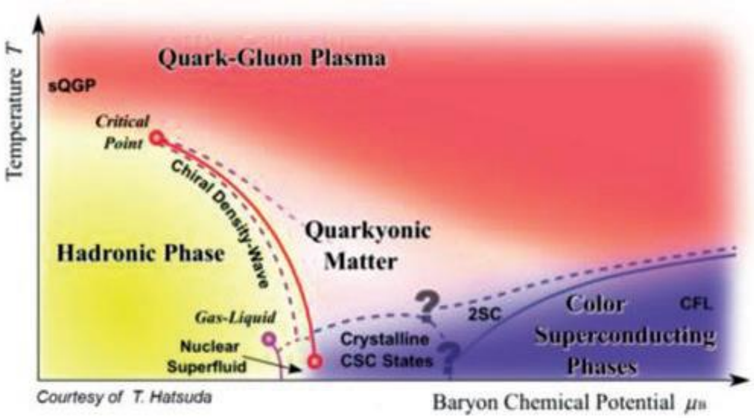
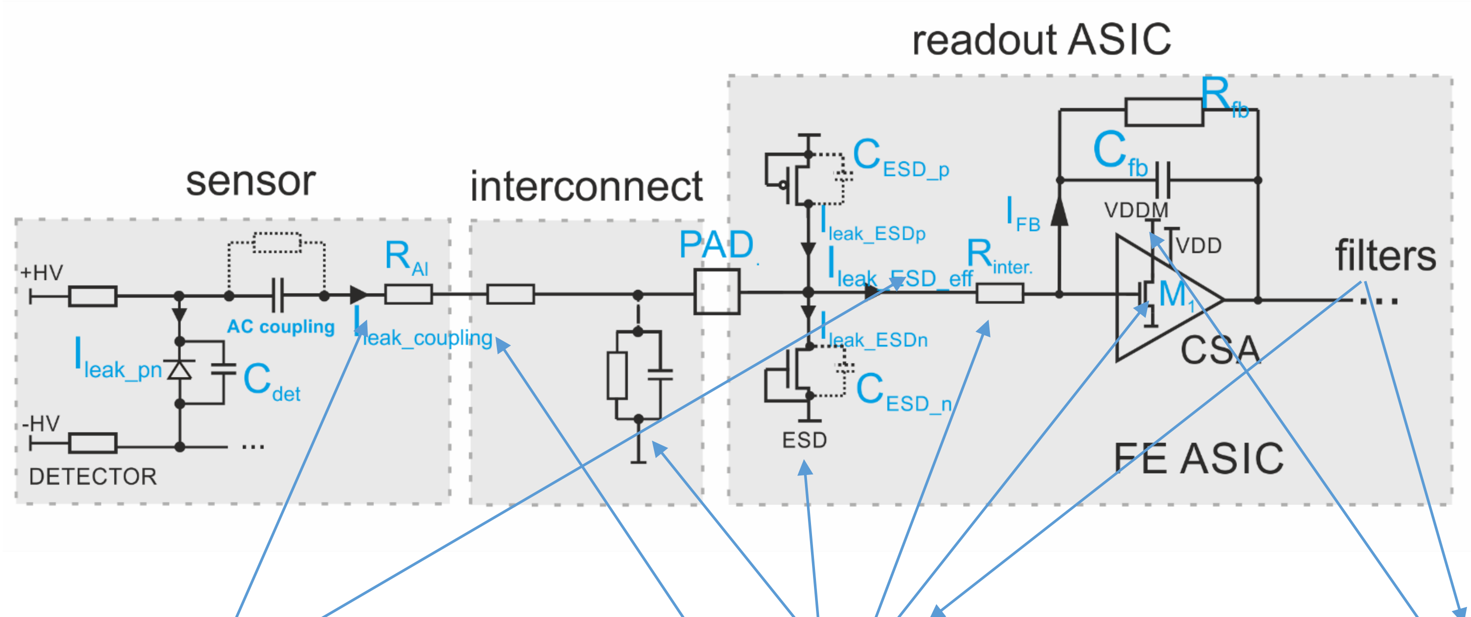




Tracking detection stations:

- Semiconductor strip detectors / gaseous detectors
- Multichannel readout electronics (Front-End)
- Radiation tolerant design
- Detection station within magnetic field

Detectors read-out electronics - challenges



Leakage current	Noise	PSRR

MOS-based ESD protection

Coupling capacitor in AC-coupled detectors
Or
Leakage of sensor in DC-coupled detectors

⇩

Impact on pulsed reset

Various system components
(overall noise)

Various detectors lengths
(different conditions)

Detector leakage

⇩

Adapting to variable conditions

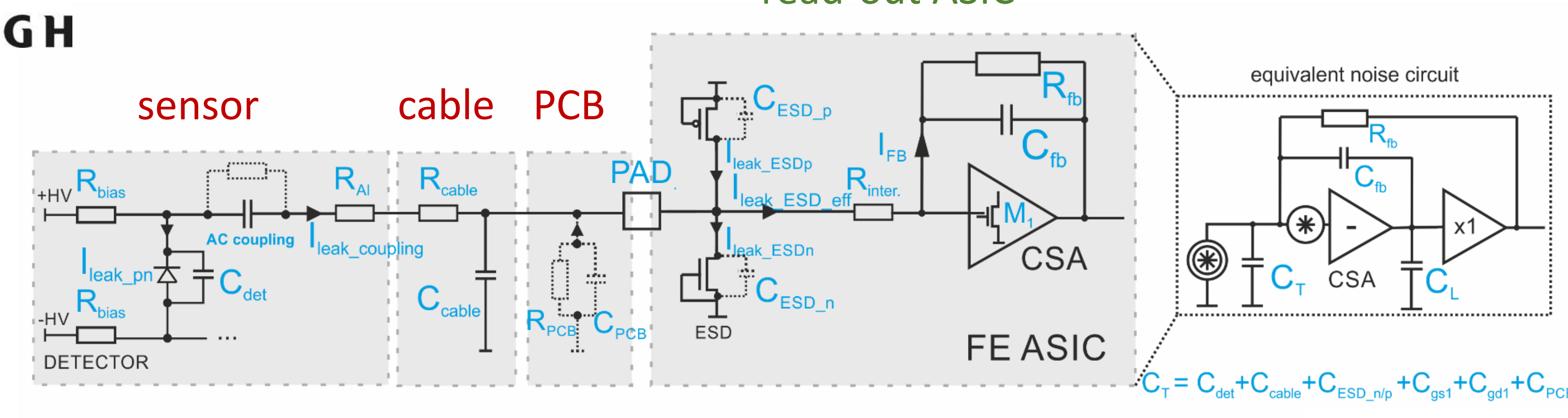
1T magnetic field

Power supply network
(radiation hardened low-voltage regulators)

⇩

Is **differential** AFE always worse?

Detectors read-out electronics: Noise sources



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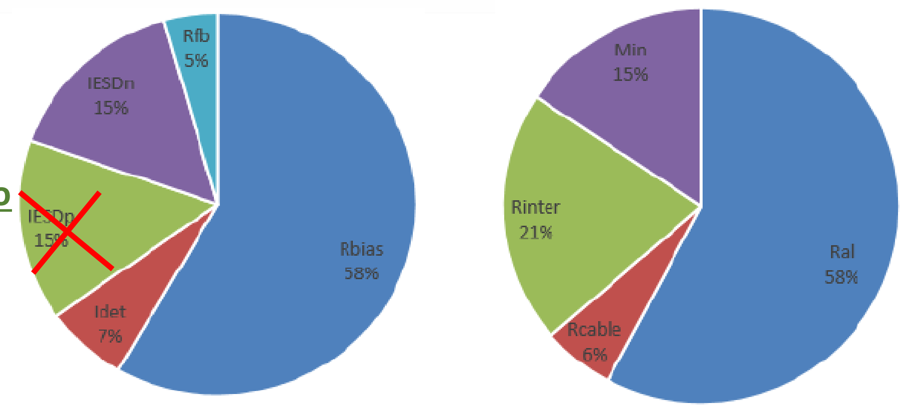
1. parallel current noise:
- **detector leakage current shot noise (I_L),**
- detector bias shunt resistance R_{bias},
- **leakage current flowing through transistors in the Electro Discharge (ESD) protection circuit,**
- **current thermal noise from feedback resistance.**

2. series white noise:
- **input transistor thermal noise ($M1_{th}$),**
- various series resistors' (sensor's metal strip, cable, interconnect on-chip) thermal noise.

3. series 1/f (or flicker) noise:
- **CSA input transistor flicker (1/f) noise (M1f).**



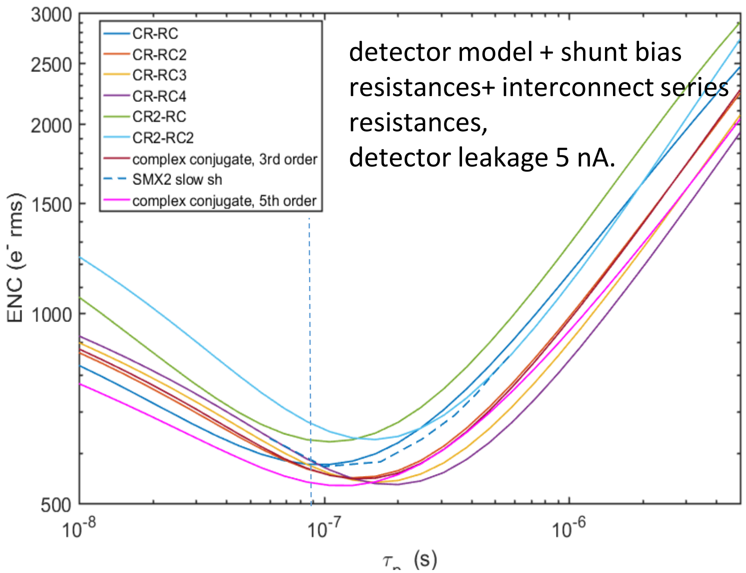
Components of the: a) current noise, b) voltage noise.

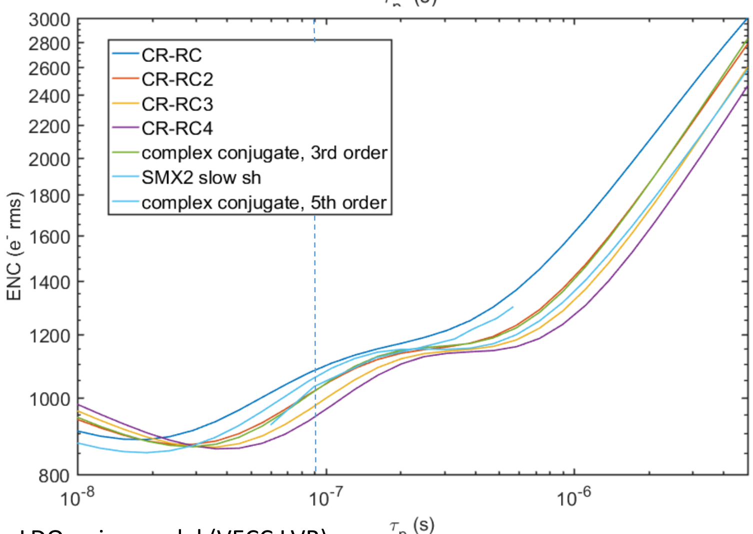
$$ENC^2 = ENC_i^{\,2} + ENC_w^{\,2} + ENC_{1/f}^{\,2} \rightarrow$$

$$ENC^2 = \tau_p \cdot A_i \cdot i_n^{\,2} + \frac{1}{\tau_p} \cdot v_n^{\,2} \cdot A_w \cdot C_T^{\,2} + A_{1/f} \cdot v_{nf}^{\,2} \cdot C_T^{\,2}$$

$$ENC^2 = A_w \frac{1}{\tau_p} \frac{4kT\gamma}{g_m} C_T^{\,2} + A_f K_f C_T^{\,2} + A_i \tau_p \left[2q\left(I_{det} + I_{fb}\right) + \frac{4kT}{R_{bias}} + \frac{4kT}{R_{fb}} \right]$$

Noise optimization - filters





LDO noise model (VECC LVR),
detector model (detector length 4 cm, cable length 49 cm),
detector leakage 5 nA.

ASIC: Weighting coefficients of filters and peaking time can be used for multi-dimensional ENC minimization based on given conditions.

	A_w	$A_{1/f}$	A_i
CR-RC	0.92	3.69	0.92
$CR\text{-}RC^2$	0.85	3.41	0.64
$CR\text{-}RC^3$	0.93	3.32	0.52
$CR\text{-}RC^4$	1.02	3.27	0.45
$CR^2\text{-}RC$	1.03	4.70	1.00
$CR^2\text{-}RC^2$	1.16	4.89	0.72
Complex conjugate poles, 3rd order	0.85	3.39	0.61
Complex conjugate poles, 5th order	0.96	3.27	0.45

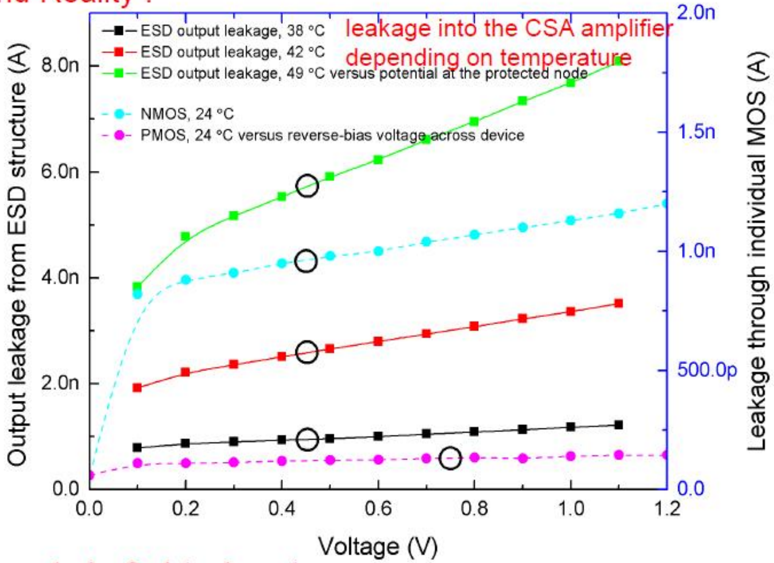
- τ_p , shaper types and order are used for design of **application specific circuit** (various current/voltage noise ratios)
- making circuit more **universal** (changing/unknown parameters)

Leakage current

Models used for leakage simulation

Simulated leakage: I_{leak_total} = 1.3nA , $I_{leak\_to\_amplifier}$=700pA, @ 430mV V_{pad}, 60 °C.

.. and Reality :

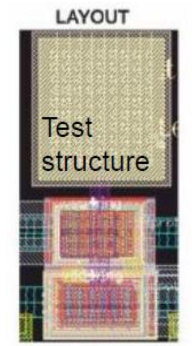


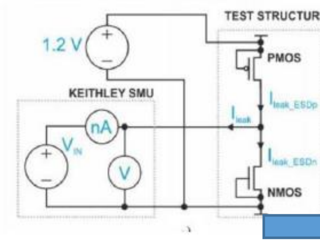
Between 1 nA – 6 nA (and more)
(approx. 8 times more than simulated)
NMOS leaks 10* more than PMOS

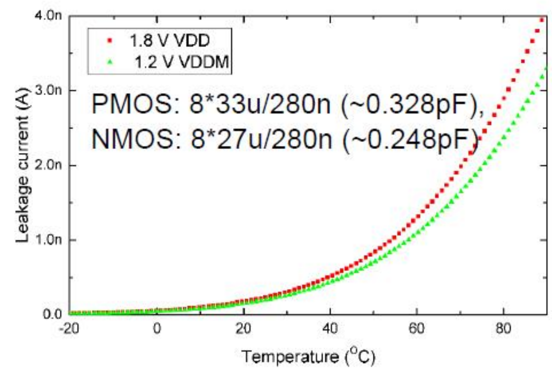
Affects:
Noise, Feedback Resistor (speed & noise),
Fast reset (speed)

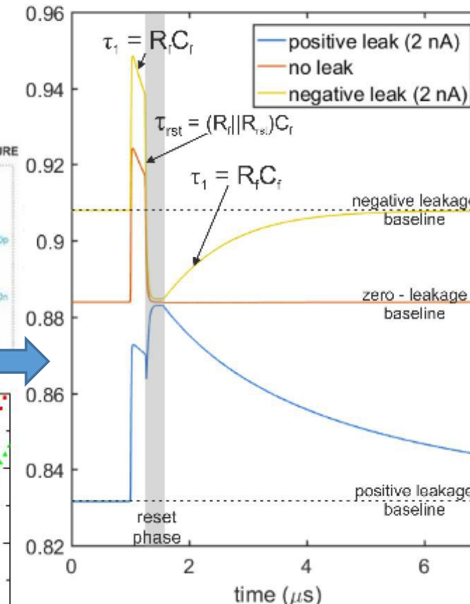
Solution: Switched double-polarity Krummenacher feedback circuit

MOS-based ESD protection (typical)



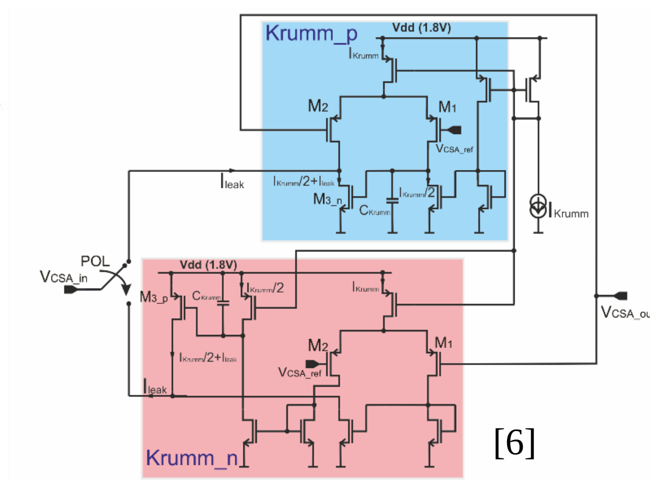






Problems:

- DC level shift
- R_{fb} change
- dynamic range limitation
- problems with pulsed CSA reset



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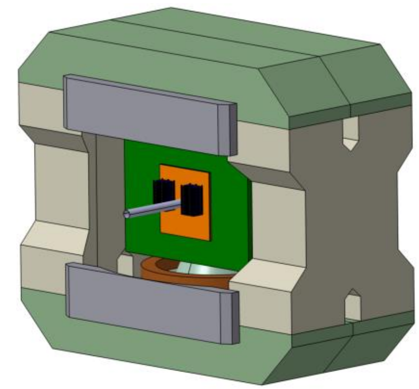
- Both **polarities** of leakage current
- High **R_{fb} value** (independent)

Power Supply Rejection Ratio

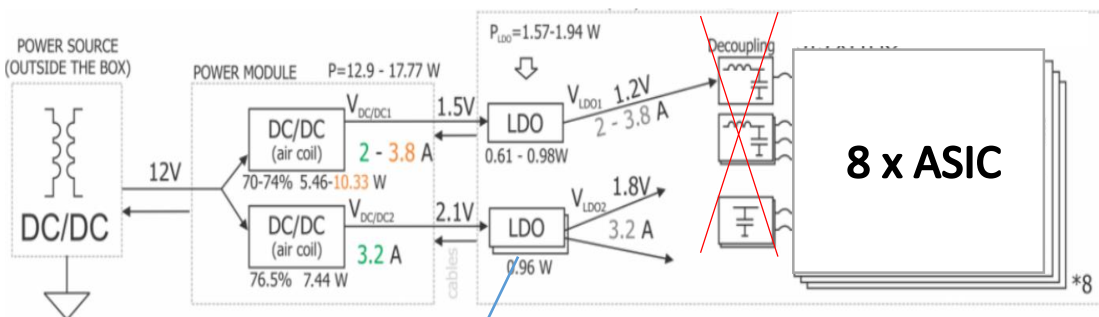
1 T superconducting dipole **magnet**



[2]

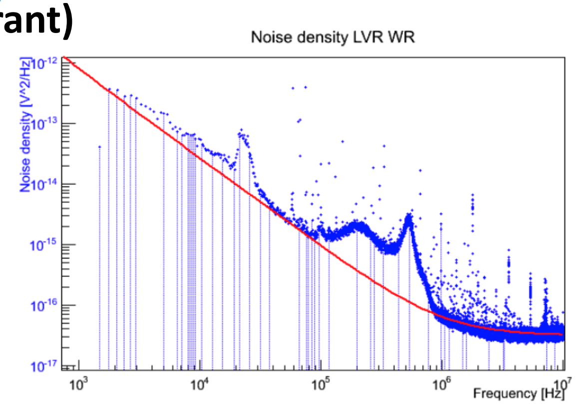
[7]

Many ASICs in the system (high power density) – power supply:
- uniform in all channels / ASICs
- supply network radiation tolerant
- low noise
- power supply interference – **can not** be filtered (LC)



no ferrite-based inductors

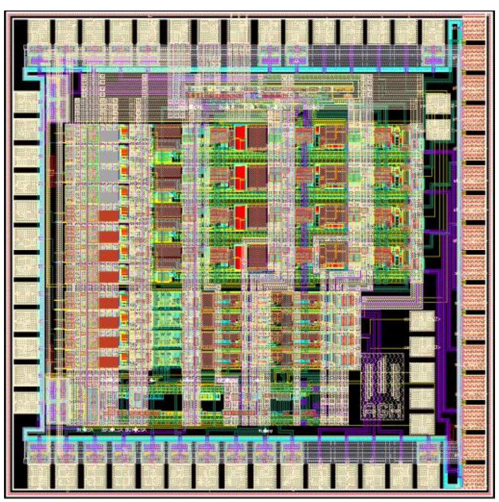
Custom Low-dropout regulator (radiation tolerant)



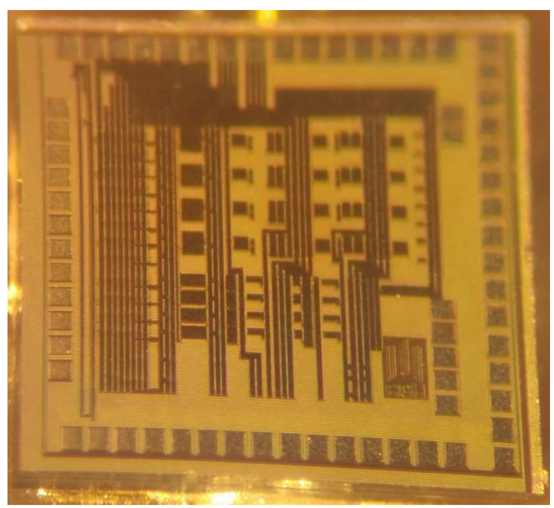
High-frequency noise !

SMX mini

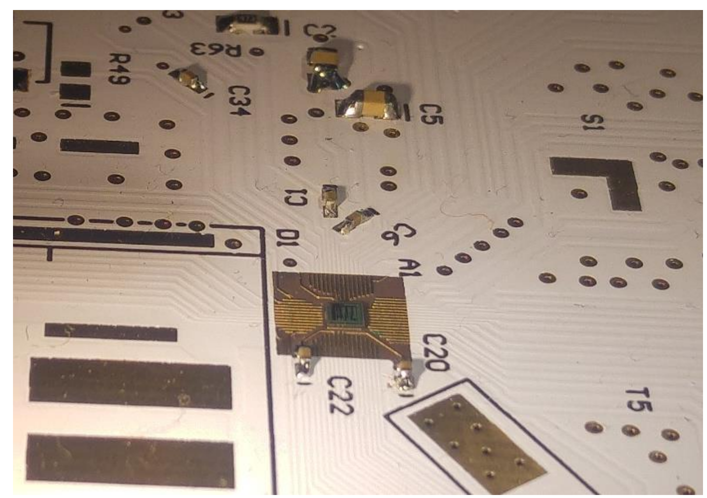
- Designed and fabricated in Q3 2018 using 180 nm process
- Area: 1.5x1.5 mm^2
- 8 channels (4x single-ended, 4x differential)
- Switchable operation modes: 16 for single-ended and 4 for differential channels (various feedback and filters architectures, two polarities)
- Power (all channels): 88 mW (single-ended: ~4.62 mW/ch, differential: ~12.31 mW/ch)



ASIC layout



ASIC photograph



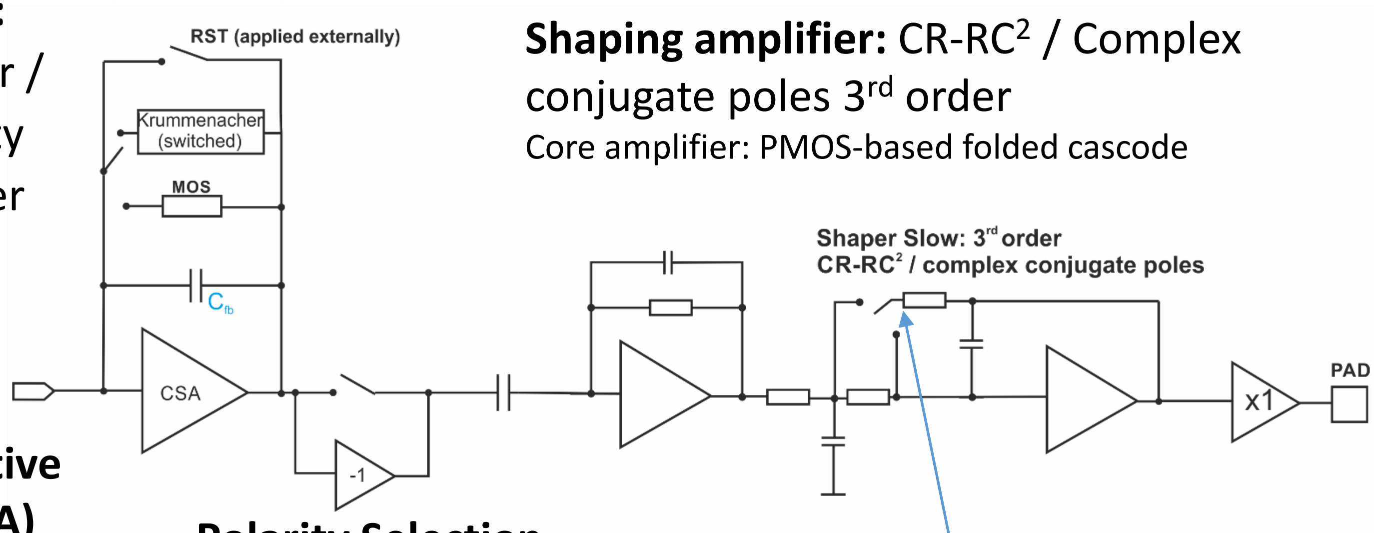
Test PCB

Single-ended channel architecture

CSA reset (external)

CSA feedback: MOS transistor / double-polarity Krummenacher circuit

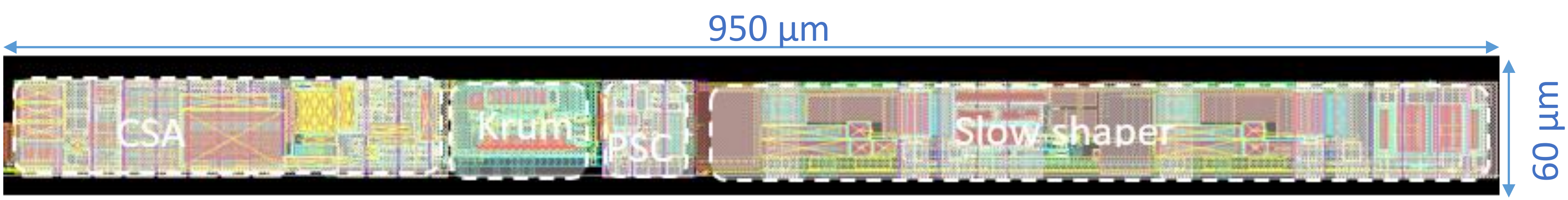
Shaping amplifier: CR-RC^2 / Complex conjugate poles 3rd order
Core amplifier: PMOS-based folded cascode



Charge sensitive amplifier (CSA)
Core amplifier: NMOS-based direct cascode

Polarity Selection Circuit
(electrons/holes)

Switchable – almost no change in the channel area



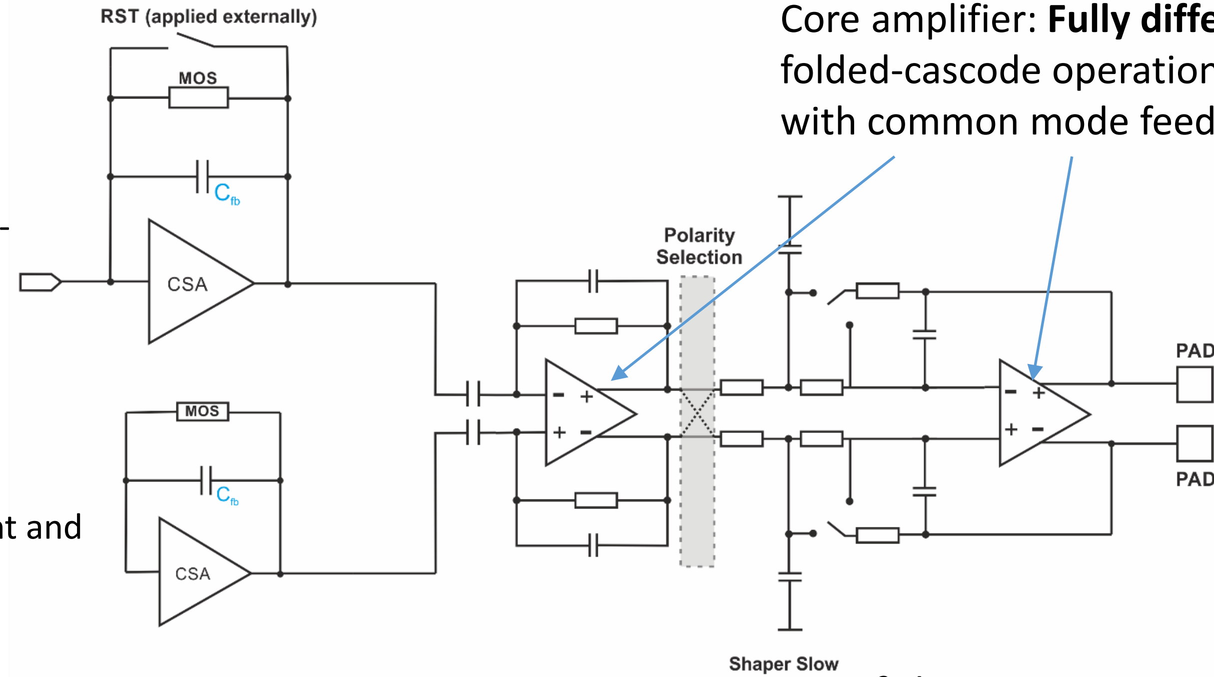
Pseudo-differential channel architecture

CSA reset
(external)

Charge sensitive amplifier (CSA)
Core amplifier: NMOS-based direct cascode

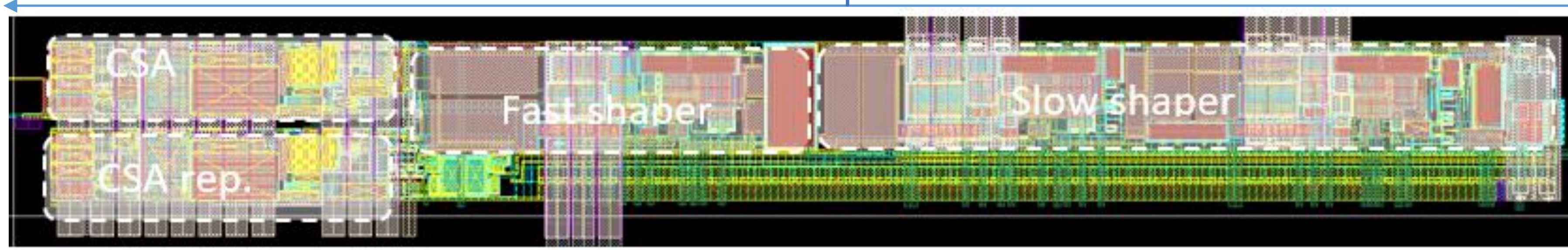
CSA replica
Scale 1:1 (bias current and transistor sizes)

Core amplifier: **Fully differential** folded-cascode operational amplifier with common mode feedback



Shaping amplifier: CR-RC^2 / Complex conjugate poles 3rd order, peaking time ~90 ns

1150 µm



125 µm

Included features

<table>
<tr><th colspan="2"></th><th colspan="2">Single-ended</th><th colspan="2">Differential</th></tr>
<tr><th colspan="2"></th><th>Electrons</th><th>Holes</th><th>Electrons</th><th>Holes</th></tr>
<tr><td rowspan="3">CSA FEEDBACK TYPE</td><td>MOS in linear region</td><td colspan="4">✓</td></tr>
<tr><td rowspan="2">Double-polarity Krummenacher*</td><td colspan="2">for negative leakage</td><td colspan="2" rowspan="2">X</td></tr>
<tr><td colspan="2">for positive leakage</td></tr>
<tr><td rowspan="2">SHAPER ARCHITECTURE</td><td>CR-RC^2</td><td colspan="2">✓</td><td colspan="2">✓</td></tr>
<tr><td>Complex Conjugate Poles 3rd order</td><td colspan="4">✓</td></tr>
<tr><td colspan="2">Polarity Selection Circuit</td><td>✓ (ON)</td><td>✓ (OFF)</td><td colspan="2">N/A</td></tr>
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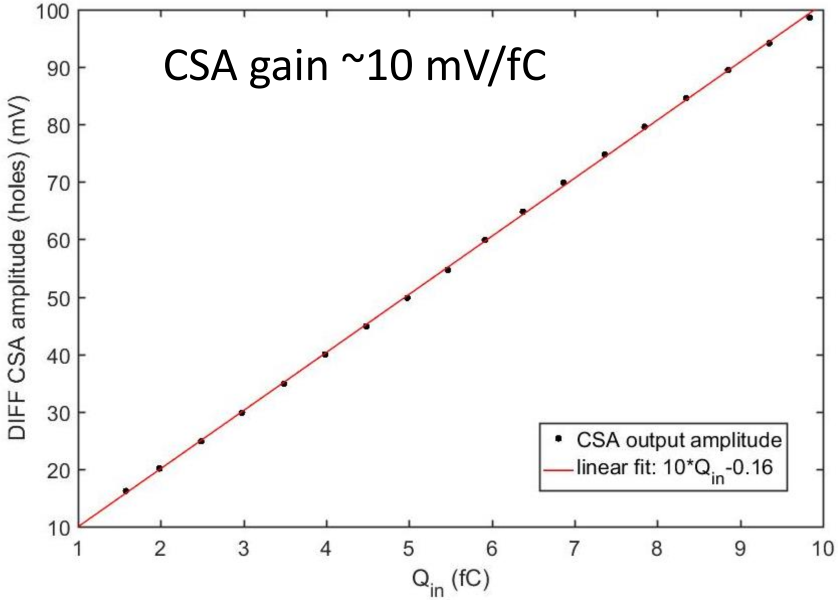
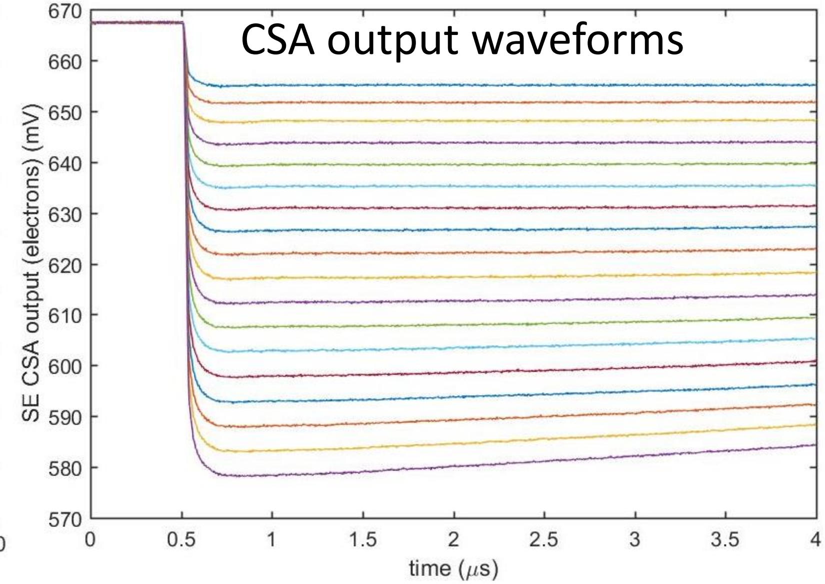
*separate compensation for current flowing into the CSA input and for current flowing from the CSA input

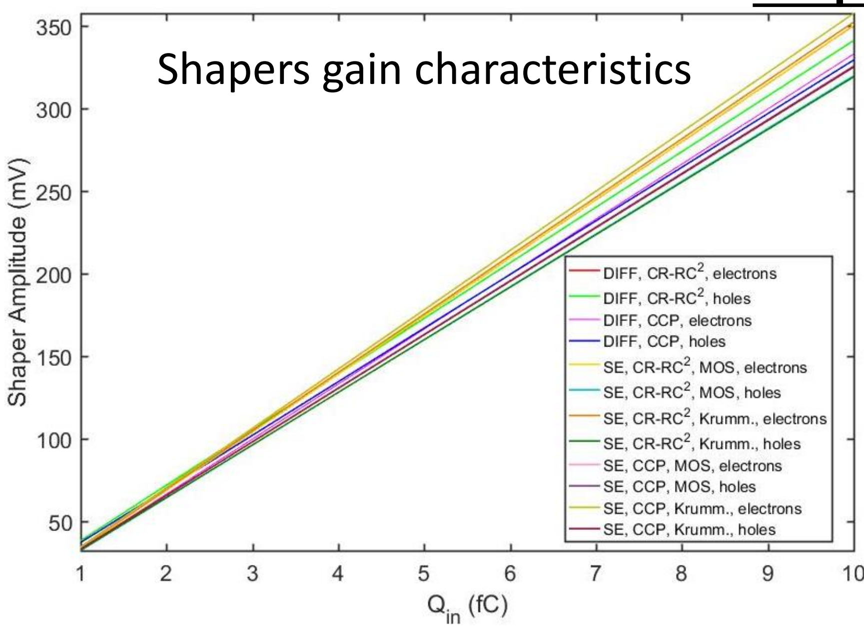
Basic characterization

Charge Sensitive Amplifier

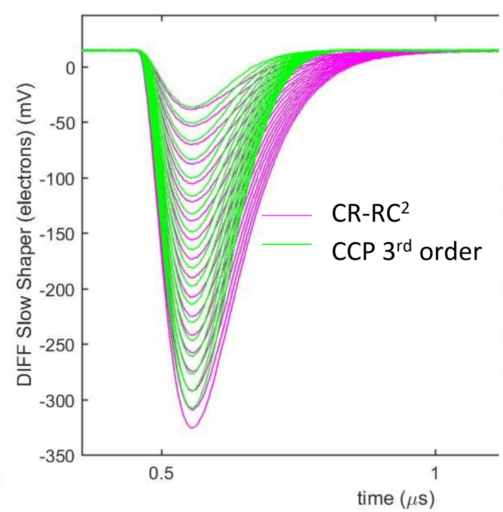




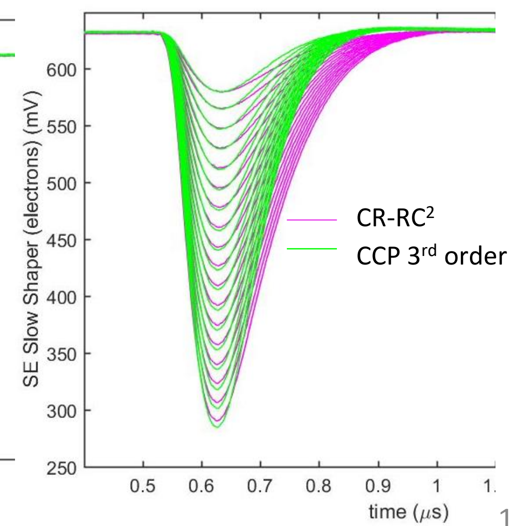
Shaping Amplifiers



Shaper differential (electrons)



Shaper single-ended, MOS feedback (electrons)



Basic characterization summary

Single-ended Slow Shaper Gain (Polarity: Electrons / Holes)

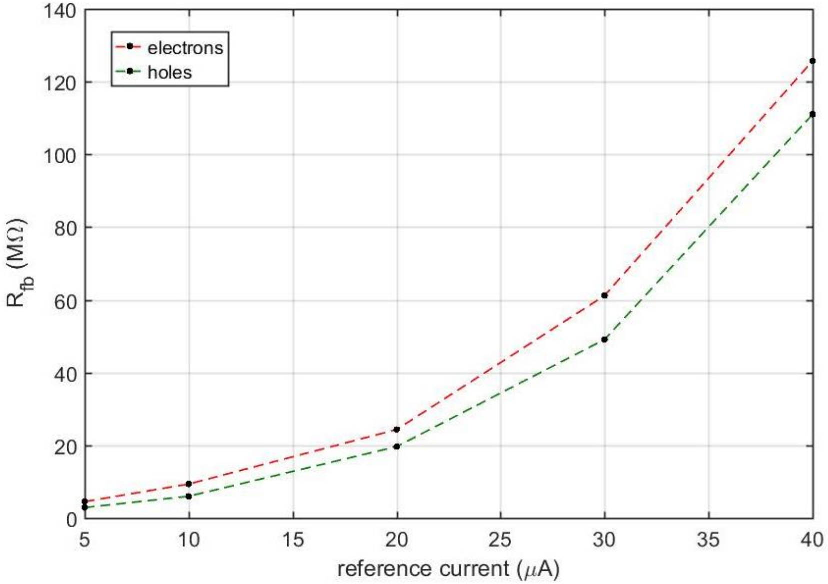
SH TYPE / FB TYPE	MOS transistor	Krummenacher
CR-RC^2	35 mV/fC (e^-) / 32 mV/fC (e^+)	35 mV/fC (e^-) / 32 mV/fC (e^+)
CCP 3rd order	36 mV/fC (e^-) / 32 mV/fC (e^+)	36 mV/fC (e^-) / 32 mV/fC (e^+)

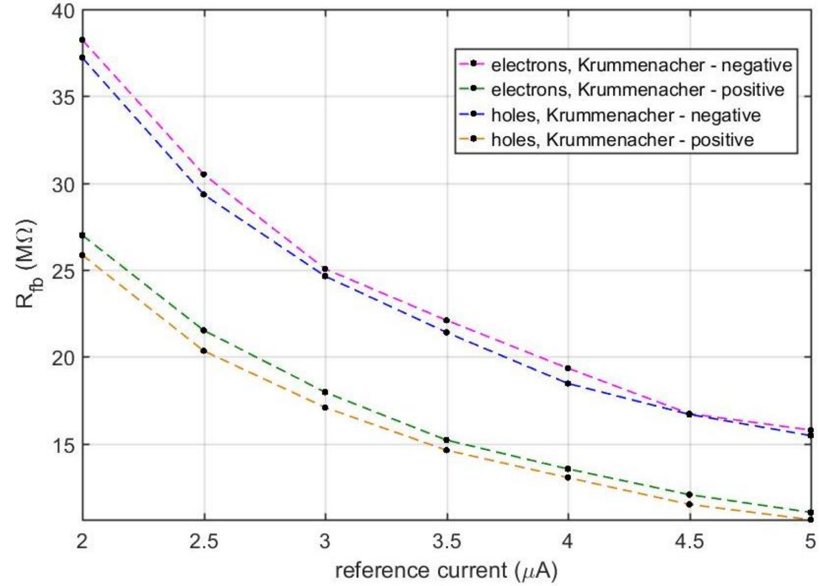
Differential Slow Shaper Gain (Polarity: Electrons / Holes)

SH TYPE	MOS transistor
CR-RC^2	35 mV/fC (e^-) / 34 mV/fC (e^+)
CCP 3rd order	33 mV/fC (e^-) / 32 mV/fC (e^+)

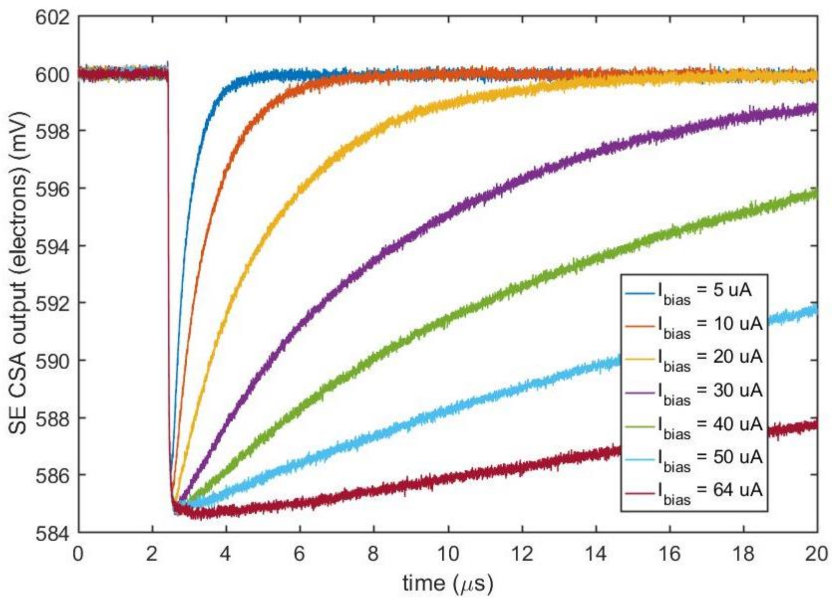
Feedback verification

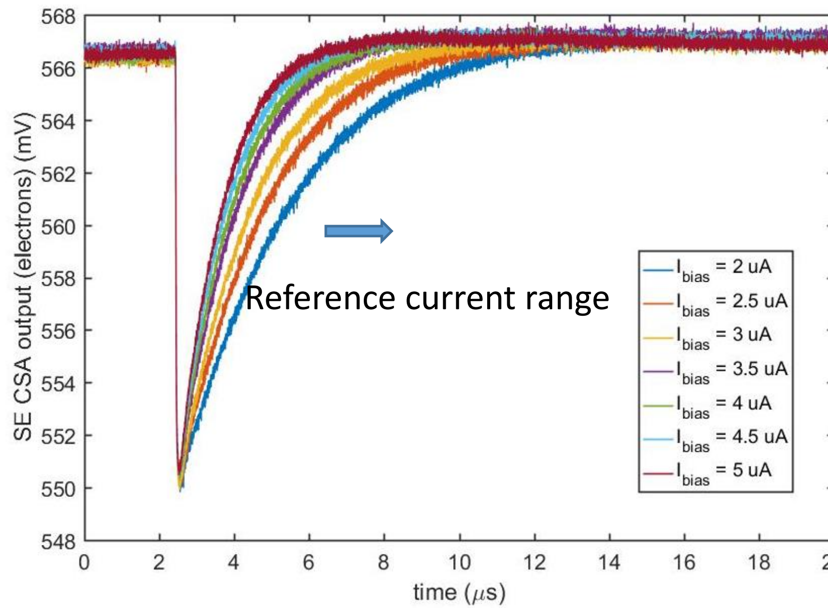
Feedback resistance vs. reference current





CSA output waveforms



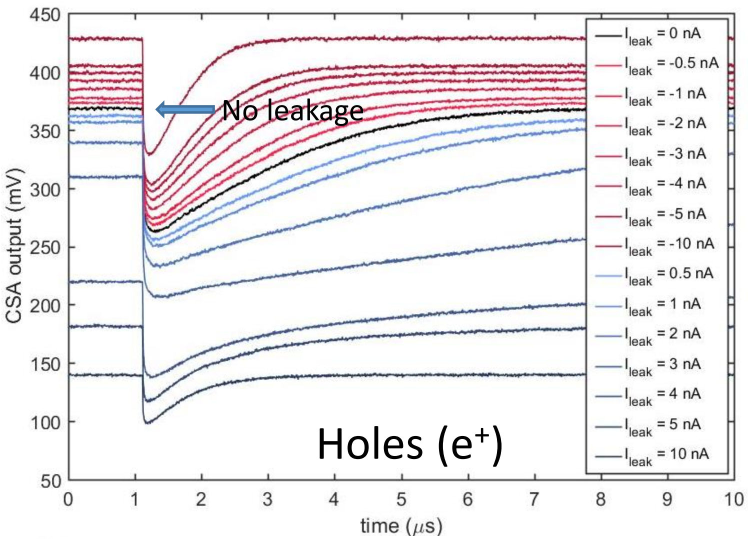


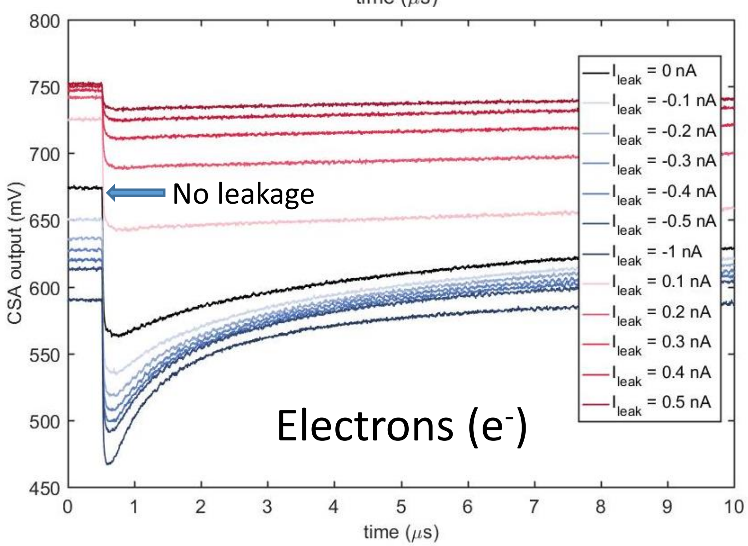
Leakage current compensation

Waveforms acquired for various leakage current values flowing into/from the CSA input

MOS transistor in linear region

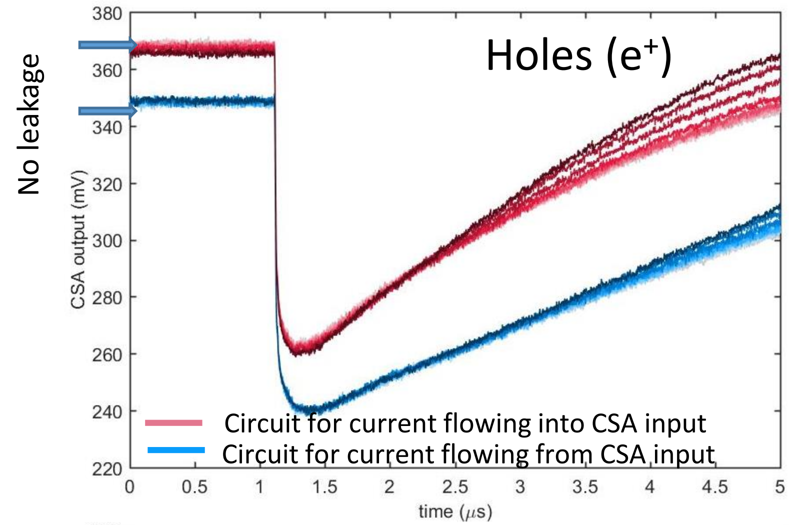
CSA output waveforms

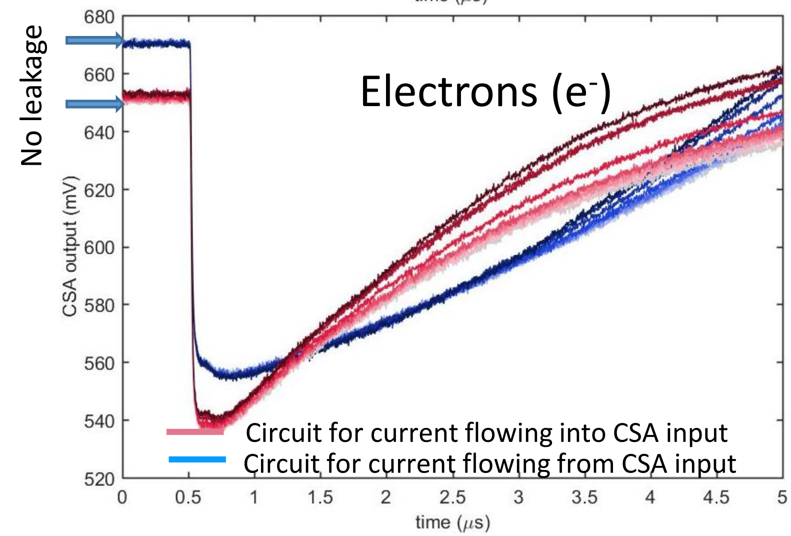




Switched double-polarity Krummenacher circuit

CSA output waveforms



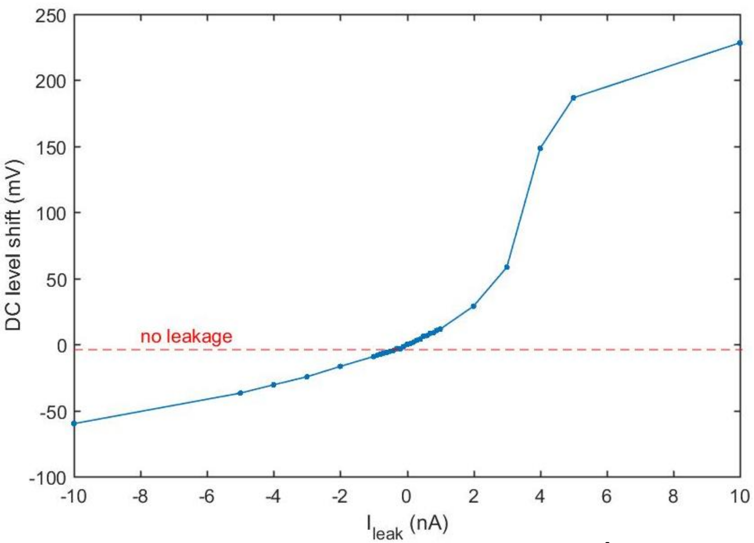


Leakage from – 40 nA to 40 nA

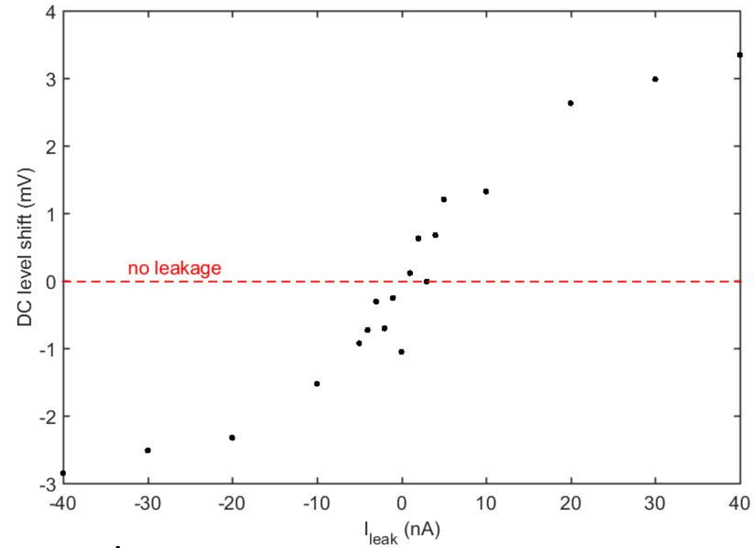
Leakage current compensation

MOS transistor in linear region | **Switched double-polarity Krummenacher circuit**

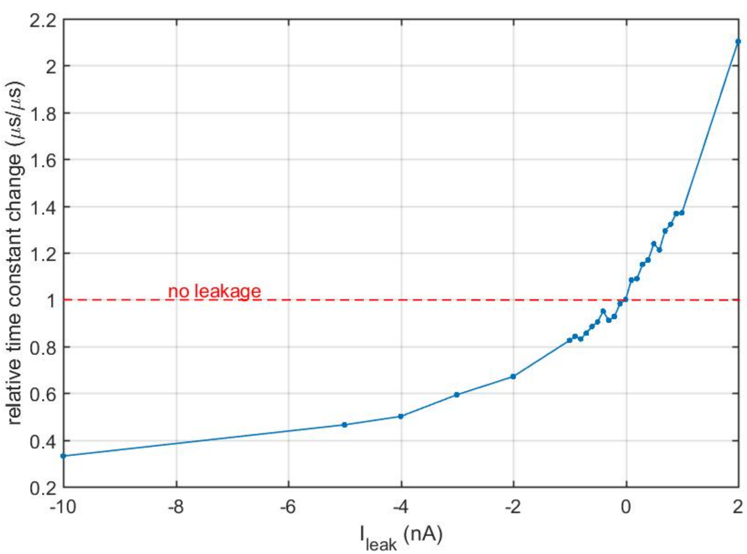
DC level shift



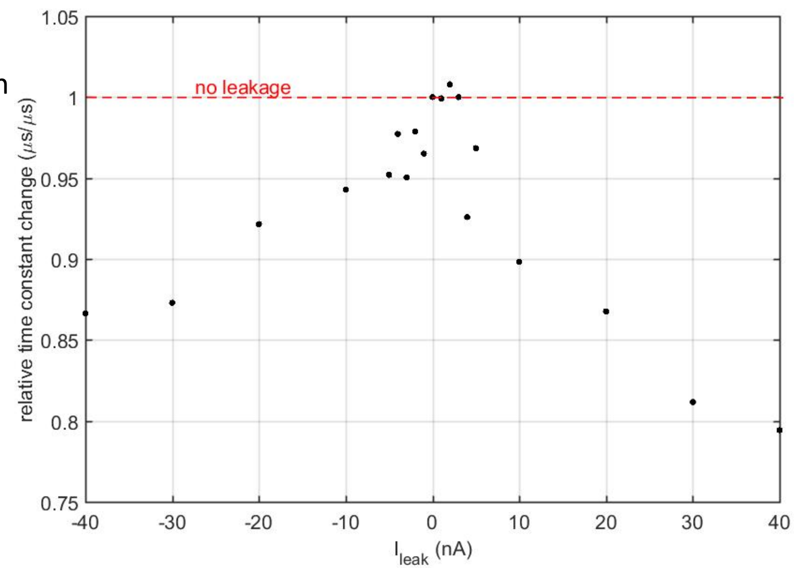
20-80 x lower DC level shift



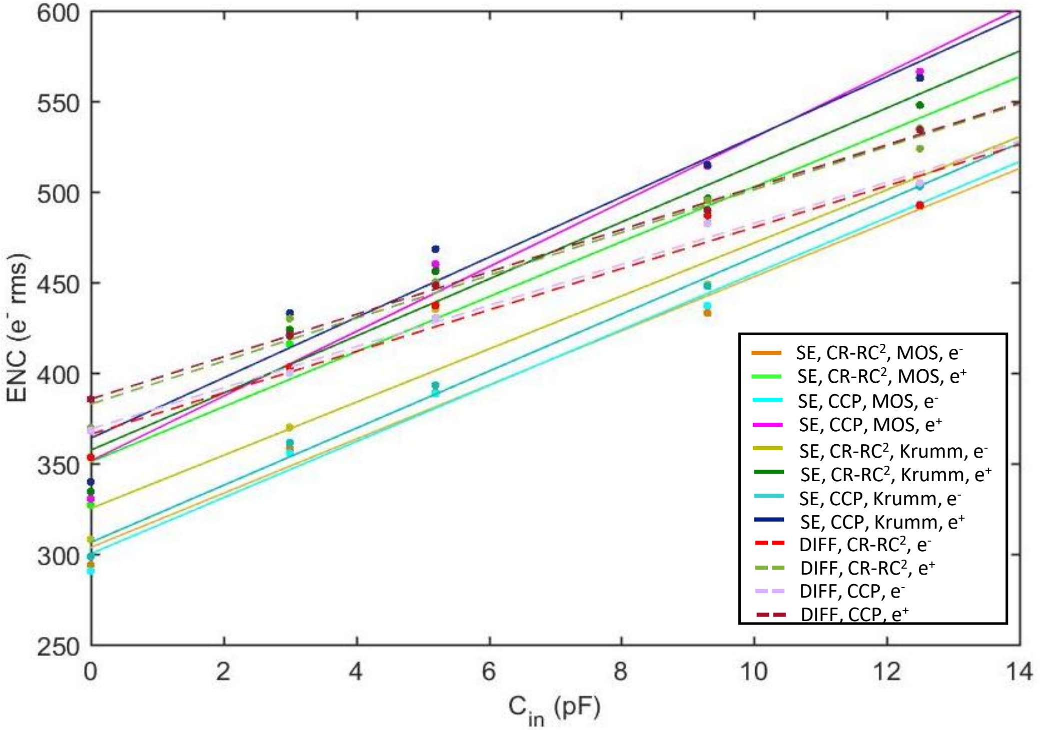
Relative time constant change



3x lower change in time constant (only for extreme cases)

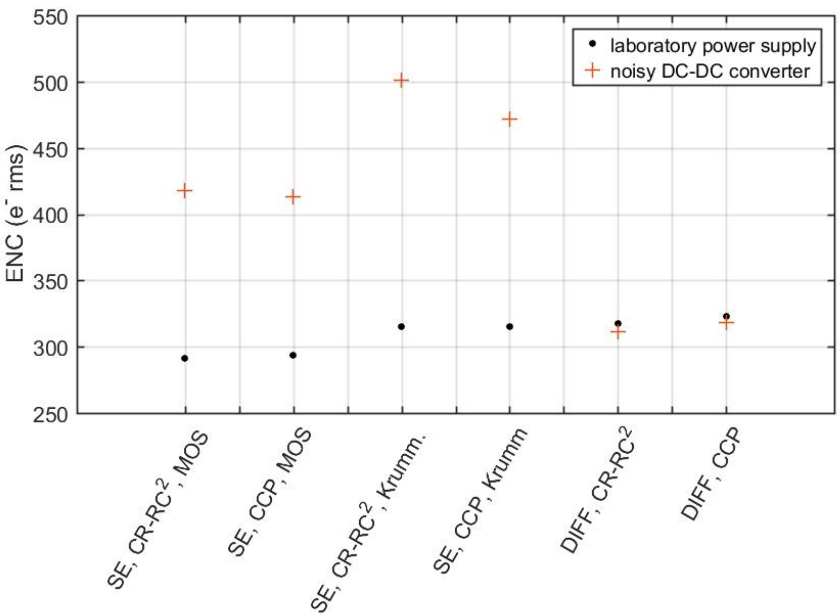


Noise performance



Noise slopes – input capacitances from **0.5 pF to 10 pF** (plus 2.5 pF of PCB traces capacitanes)

Noise for clean power supply (laboratory PS) and with impulse LDO, no input capacitances (inputs not wire-bonded)



Conclusions

- **Leakage with pulsed reset -> problems**
- Leakage can be opposite polarity (e.g. MOS-based ESD protection circuit)
  - ✓ other options: ,,diode" (preparation of configurable cells needed)

switchable Krummenacher circuit

- **Power supply noise**: can be an issue in sophisticated systems:
  - ✓ ultra low-noise LDOs can not be used (radiation);
  - ✓ LC-filtering not feasible in tracking detection stations (magnetic field);

Supply noise rejection by differential shaping (with CSA replica)

- **Configurable shaper type:**
  - ✓ area penalty;
  - ✓ helps adapt noise to required level;
  - ✓ for varying contributions of voltage and current noise
  - ✓ next step: configurable peaking time.

Thank you for your attention.

References

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6. Weronika ZUBRZYCKA, Krzysztof KASIŃSKI, “Leakage current-induced effects in the silicon microstrip and gas electron multiplier readout chain and their compensation method”, Journal of Instrumentation, ISSN 1748-0221. — 2018 vol. 13 art. no. T04003, s. [2], 1–10.
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