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Prototype single-ended and differential charge processing circuits for micro-strip silicon and gaseous sensors read-out

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Read-out electronics for High-Energy Physics Experiments as for example Compressed Baryonic Batter experiment at FAIR, Darmstadt, Germany, should meet tight requirements concerning noise (ENC < 1000 e- rms to guarantee proper measurements of charge), power consumption (< 10 mW/ channel) and high average input hit frequency (250 kHit/s/channel) [1]. The ICs design should take into account not only the charge processing parameters but also the impact of the environment like radiation, noisy power supply and temperature to ensure reliable and stable operation during experiment in a system built with tens of thousands of devices.
The operation with gaseous detectors require protection of the inputs against electrostatic discharge. The ESD protection circuit together with the sensor itself or decoupling capacitors (after irradiation) can be however a source of additional leakage current flowing into the first stage of charge processing chain and contributing to the overall system noise [2]. The read-out electronics (in particular first stage –charge sensitive amplifier, CSA) and detector related noise can be mitigated using proper filtration and signal shaping. However, noise introduced by external sources, like power supply interference can not be limited only via proper shaping and filtration. When no LC filtering is possible (due to high magnetic fields) it may be beneficial to use differential or pseudo-differential signal processing [3].
The purpose of this work was to test several ideas to improve noise performance and to make the architecture of charge processing chain configurable to better adapt to varying target radiation imaging applications. The ASIC comprises four single-ended and four pseudo-differential signal processing channels. In both types of channel configurable slow shaper configuration is used –it is switchable CR-RC2 type shaper and complex conjugate poles 3rd order shaper. CSA feedback in single-ended architecture can be selected between MOS transistor working in linear region and double-polarity Krummenacher circuit for leakage current compensation capability.
The chip was designed and fabricated in Q3 2018 using 180 nm process. Front-end single-ended and differential channels occupy area from 950 x 60 um2 up to 1150 x 125 um2 and consume 4.5 up to 10.5 mW of power respectively. The work presents design and measurements results.

REFERENCES

[1] Heuser, J., Moeller, W., Pugatch, V., Senger, P., Schmidt, C. J., Sturm, C., & Frankenfeld, U. (Eds.). (2013). [GSI Report 2013-4] Technical Design Report for the CBM Silicon Tracking System (STS). Darmstadt: GSI. http://repository.gsi.de/record/54798
[2] O. Bertini, A. Lymanets, Systematic study of sensor properties, CBM Progress Report 2016, GSI, Darmstadt.
[3] Soltveit, H. K., Stachel, J., Braun-Munzinger, P., Musa, L., Gustafsson, H. A., Bonnes, U., ⋯Lang, S. (2012). The PreAmplifier ShAper for the ALICE TPC detector. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 676, 106–119. https://doi.org/https://doi.org/10.1016/j.nima.

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