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Ethernet Embedded Readout Interface for Timepix2 - Katherine readout for Timepix2

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Timepix2 [1] is an improved version of the Timepix with advanced features and functionalities developed by the Medipix2 Collaboration at CERN. It is a frame-based readout chip featuring a 256x256 pixel grid with 55 μm pitch. The chip implements eight modes of operation, of which two allow simultaneous and six continuous measurements. In continuous modes, two sets of pixel counters are available. While the first set is used for measurement, the second one is used data readout. Thus, the dead time is practically absolutely eliminated. Simultaneous modes enable a measurement of energy (Time-over-Threshold) and time-stamping (Time-of-Arrival) simultaneously. In addition, Timepix2 supports matrix occupation checking (which could be valuable for a reduction of overlapping clusters). Special digital pixels outside the matrix enable a connection of external signals (e.g. from single pad diodes, triggers). While the high power consumption of Timepix and Timepix3 are rather high, Timepix2 allows to switch off parts of the matrix absolutely so that power consumption can be reduced. This could make Timepix2 a good candidate for space projects or wearable electronic systems.
The presented readout/acquisition device for Timepix2 is the next generation of the Katherine readout [2]. Katherine is an embedded computer, supporting a connection with the CERN chip board. It manages all communication with the Timepix2 readout chip. The readout device is based on the Gigabit Ethernet interface and profits from all its advantages: cheap and reliable cabling, good bandwidth and operation at long distances (up to 100m) from a computer or server. Thus, the readout system is an ideal solution for places with difficult access.
The introduced system supports all detector modes, including Zero Columns Suppression (ZCS; suppression of zero columns within a readout process). The device implements decoding of pixel data to an easily readable format and zero-pixel suppression directly in hardware. This reduces demands on control/acquisition software. There is also high voltage power supply offering both polarities of bias voltage (up to ±300V) and GPIO ports for triggering or integration of the detector to an existing measurement chain. Since it has enough computational power (dual-core ARM A9 processor + FPGA + DDR3 memory), this platform is suitable and ready for on-line data pre/processing (cluster analysis).
The presented work describes the functionalities and performance of the readout system in detail and also presents a control software with functionalities such as the sensor equalization, DACs dependency scan, Threshold calibration, etc. developed for this system.

Figure 1. Katherine readout for Timepix2 with CERN's chipboard.

REFERENCES

[1] W.S. Wong et al. Introducing Timepix2, a frame-based pixel detector readout ASIC measuring energy deposition and arrival time. Radiation Measurements. Under review.
[2] P. Burian et al 2017 JINST 12 C11001

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