Karlsruhe Institute of Technology

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KIT ASIC and Detector Laboratory

Development of CMOS Sensors for Electron Microscopy

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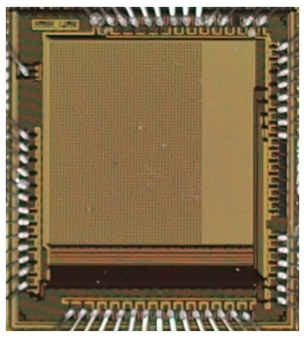
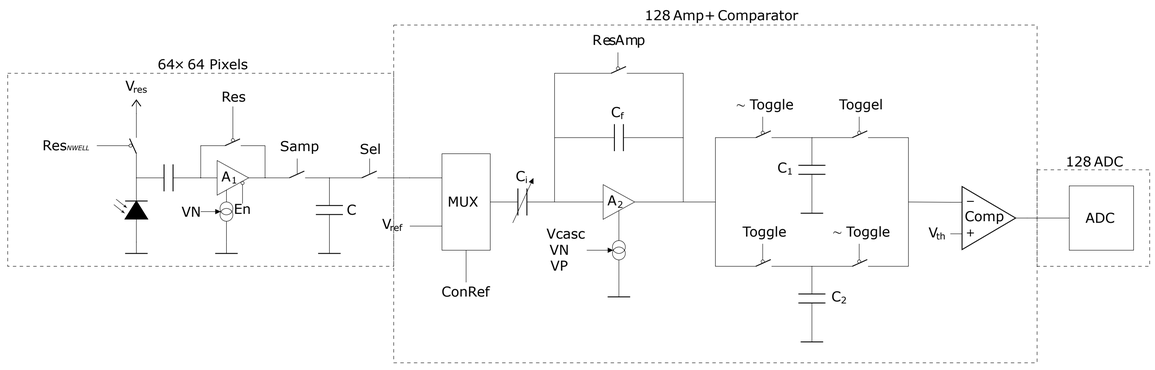


The HPixel Sensor

The current prototype for the proposed sensor was developed in 180nm AMS HV-technology [1] with a 64x64 pixel matrix and a rolling shutter readout. Single pixels exploit deep n-wells on p-substrate diodes. Secondary particles are collected on the deep n-wells which include the front-end pixel electronics. Front-end electronics contain a charge sensitive amplifier and a correlated double sampling circuit. Signals are then passed to 128 readout channels at the chip periphery, each channel containing an amplifier and an 8-bit digital-to-analog converter (D/A converter). The digitalized signals are serialized and output via 8 Low Voltage Differential Signals (LVDS).

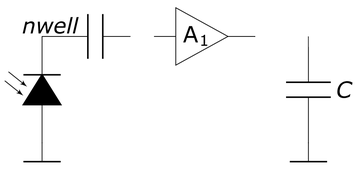
Chip Architecture



There are two types of pixels, the most complex is discussed here. The pixel electronics contains a charge sensitive amplifier A1, a capacitor C used to store the reset-level and several switches.
The readout block includes a multiplexer, an amplifier, a two-capacitor system, a comparator, and a counter. There are 128 channels on the chip, twice as many as the pixels in one row. By reading out two-pixel rows at the same time, the speed of the system is increased. Correlated double sampling is enabled by proper control of the switches Samp, Sel and Res Amp. A two-capacitor system is exploited to increase parallelism and throughput; one capacitor is in the signal-track mode while the other is charged by a constant current. By measuring the time needed to charge the capacitor to a certain voltage, A/D conversion is performed.

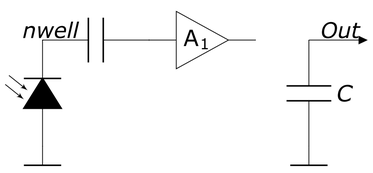
Sensor Operation

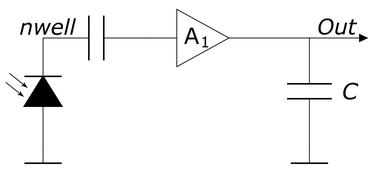
The sensor operation can be separated in 4 stages:



Initial state:
Capacitor C stores the RESET voltage value while the charge signal is being collected at the nwell node.
During this state, the charge sensitive amplifier A1 is disabled.
The charge generated by photons or particles decreases the voltage at the nwell node.

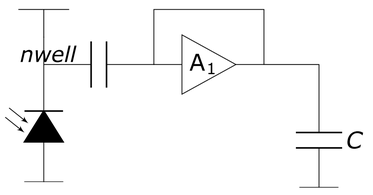
State 1:
The Reset voltage is sent to the next block (amplifier) for CDS (Correlated Double Sampling).
At the same time, the charge sensitive amplifier A1 is enabled, making possible to amplify the charge received by the sensor.





State 2:
The amplified signal is sent to the CDS stage.
The CDS blocks compute the difference between the signal voltage and the reset voltage. This is possible due to the correct control of the switch that shortcircuits the feedback of the amplifier A2 (next stage).

State 3:
Reset of the pixel. The nwell node is reset and the reset voltage is now connected to capacitor C, which will store this value.
The Out node is now disconnected from the capacitor, making possible to the amplifier of the next stage to acquire the reset value of the next pixel (state 1).



The system

The hardware system consists of the chip under test, two PCB, one where the chip is bond and the other to make the physical interface between the FPGA and the chip (Figure 1). The FPGA used is a Nexys Video, which creates the link between the PC and the chip. The FPGA receives the configuration data for the chip, from the PC. Then FPGA generate all the relevant signals to control the chip and it receives the data from the chip and sends it to the PC in the correct form and order.

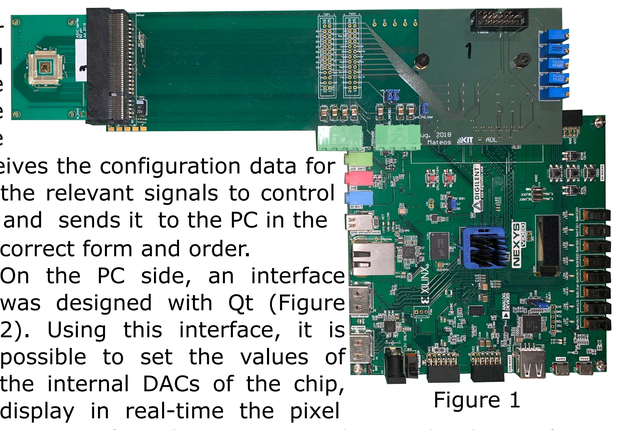


Figure 1

Figure 2

On the PC side, an interface was designed with Qt (Figure 2). Using this interface, it is possible to set the values of the internal DACs of the chip, display in real-time the pixel matrix values, histograms, and store the data.. Also, it is possible to change the functioning mode (normal measurement or Zero Suppress), and to select the type of pixels that will be used (current pixels, above described, or voltage pixels, the simple ones).

Measurements

The chip has been irradiated with X-Ray and electrons.
For the X-Rays, it was used a Seyfert ISO-DEBYEFLEX 3003 X-Ray tube with 7 different targets to obtain specific energies.
By fitting a normal distribution function around the peak is possible to compute the mean output value over the pixel matrix (Table 1). The sigma value is representative of the measurement error (from the Gaussian approximation around the bottom of the scale), and the average noise measured along the matrix was 86e-.
To test the chip with electrons, a TECNAI-F20 transmission electron microscope has been used with 200 KeV electrons.

Target	Energy [eV]	μ [bin]
Fe	6403.13	105
Cu	8048.11	115
Zn	8639.1	118
Mo	17479.1	157
Ag	22162.99	172
In	24209.78	177
Sn	25271.34	180

Table 1

X-Ray

- 7 differents targets
- Energy range 6.4 KeV ~ 25.3 KeV
- Noise floor of 86 e-

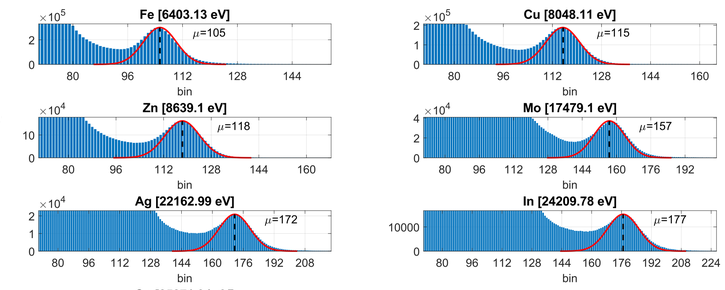


Figure 3

Figure 3 shows the histograms of each irradiation, and the Gaussian approximation for each peak (red curve). The mean value in ADC counts of the Gaussian is related to the source energy applied and can be used for calibration.
A presence of low-energy peak (around 110) on the histograms of the high energies measurements is due to residual Copper on the tube setup. After the energy test, a total dose measurement was carried out. After 50 Mrad, the chip worked, with with a noise floor of 201 e- (average over the whole matrix). After 250 Mrad, the chip continued to respond, however, the noise increased to 245e-.

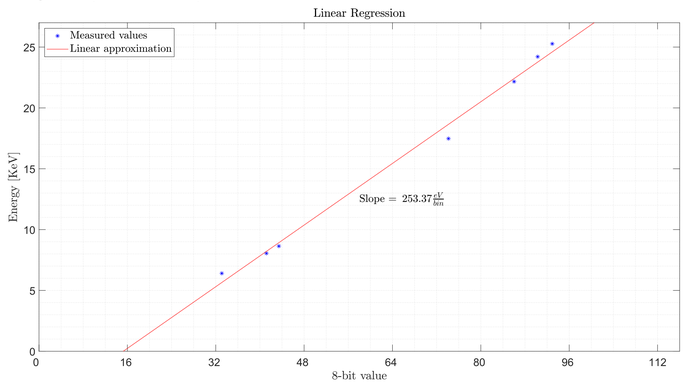


Figure 4

To obtain the conversion factor between the ADC count output of the chip and the beam energy, the least-squares method was used. The dataset was fitted with a linear expression, due to the fact that the response is expected to be linear within the energy range. The conversion factor is the slope of the linear approximation, which was calculated as being 253.37 eV/bit (R^2=0.996).
After 50 Mrad, the conversion factor changed to 329.18 eV/bit (R^2=0.997). After 250 Mrad, the chip continued working, however, due to the high background noise, it was not possible to calculate the factor conversion.

Electrons

The chip was tested with electrons, the beam was first calibrated with a Faraday Cap, and then the whole silicon sensor was uniformly irradiated.
The chip was able to detect single electrons hits (Figure 5). However, the readout block (possibly switched capacitor amplifiers) stops to work properly and the pixel gain changed when the ionizing radiation dose was around 78 Krad.

- Background noise before irradiation start was 47 ADC counts
- Background noise after last working measurement (61.42 Krad accumulated dose) was 65 ADC counts

Due to the fact that the first circuit that stops to work properly was the readout block, another chip was tested. In this case, the beam was focused only on the sensor matrix, in order to irradiate as low as possible the surrounding circuitry.

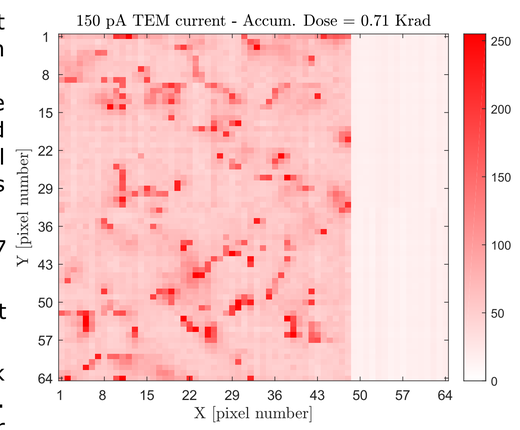


Figure 5

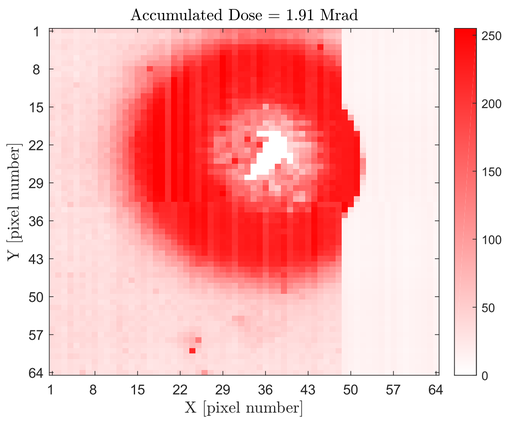


Figure 6

The irradiation was done in stages, and the noise was measured between each step. Figure 6 shows one of the irradiations. The hot spot is where the beam was focused.
After 3.5 Mrad, the pixels at the center of the spot were saturated without the beam on.
Under these circumstances, the chip was able to stand ~63 Mrad (due to the set up of the beam, the surrounding received an unknown dose). After this dose, the chip stoped working, showing no output data. This second measurement demonstrated the radiation hardness of the sensor matrix and the need for improvements on the circuitry of the chip. The measurement also shows the difference in radiation tolerance tolerance of the pixel when a different type of radiation is delivered. With photons the background noise increased from 44 to 71 at 50 Mrad, while with electrons the noise shows a much higher variation, increased from 39 to 142 at 3.5 Mrad.
This measurement showed that the matrix can stand more radiation, however, the surrounding circuitry could not.

Conclusions

The chip shows a linear response for the energy range between 6.4 KeV ~ 25.3 KeV, with a noise level of 86e-. The chip was also tested for total dose up to 50 Mrad without showing signs of damage but with an increase of noise (from 86e- to 201e-), and the charge conversion factor, from 250.28 eV/bit to 329.18 eV/bit. After 250 Mrad, the noise is too high, making impossible to distinguish the energy peaks. Further experiments will be carried out, like the influence of annealing.
It is possible to detect single electrons hits with the system, however it is necessary to improve the radiation hardness of the design to ionizing dose in order for the chip to withstand higher levels of electron irradiation. Measurements show that the sensor matrix can stand high dose, but the surrounding electronics can not.
The higher the substrate voltage the greater the depletion region is. We expect a lower charge spreading with higher voltages due to the increased collection by drift. However, the substrate is currently 200 μm thick and it cannot be fully depleted. The charge spread could be reduced by back thinning the chip.
Further investigation on the ionizing dose tolerance is to be carried out. Also, an HVCMOS sensor with different peripheral circuitry will be tested to investigate which periphery circuit is the weak point of the design in terms of radiation tolerance.
A next generation of the chip is being designed, to avoid using too many digital signals. The chip will generate the control signals inside, and the output will be 1-bit serial output. In this way it is expected to decrease the noise level.

References

[1] Ehrler, F., Blanco, R., Leys, R., Perić, I.; "High-voltage CMOS detectors"; Nuclear Instruments and Methods in Physics research Section A Accelerators Spectrometers Detectors and Associated Equipment; 2015; 650. 10.1016/j.nima.2015.09.004.

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Smart Sensor Technologies and Training for Radiation Enhanced Applications and Measurements (STREAM) has received funding from the "European Union's Horizon 2020 Research and Innovation Programme" under the Grant Agreement No 675587.