Designing the first Mexican SiPM Data Acquisition System - MexSiC

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Introduction

This work describes the concept and the first simulation results for a data acquisition (DAQ) system designed to process and digitize signals delivered by clusters of *SensL J-Series 30035* [1] SiPMs. The core part of the system is the MexSIC chip, currently under development in a 180 nm commercial CMOS technology, aimed at acquiring nine input SiPM current pulse signals in parallel, discriminating the detected events of interest using a Triggering Logic Unit (TLU), defining their exact time of arrival using an internal 2 Ghz digital oscillator that forms part of both, the time-to-digital converter (TDC) and the charge-to-digital converter (QDC), respectively, calculating the signal´s time-over-threshold (ToT) values, and finally delivering the 12-bit digitized signals and their integrals using a Delta-Sigma (ΔΣ) ADC and an external FPGA module.

Methodology

Fig. 1 shows the operational diagram of the proposed system. The SiPMs are placed off-chip whilst the rest of the components, with the exception of the Field Programmable Gate Array (FPGA) modules, are placed on-chip. **Trans-impedance amplifiers** (TIA) are used as input stages for SiPM current pulse signals. A **triggering logic unit** (TLU) is used to discriminate and validate these input signals by comparing them with externally programmable threshold levels. Once validated, the input signals are further processed at the **time-to-digital converter** (TDC) and the **charge-to-digital converter** (QDC) stages, respectively. Using the TDC, the times of arrival of TLU validated signals are defined using a master-clock triggering signal and an on-chip PLL unit running at 2GHz. 10 bit on-chip counters are used to store these times of arrival ready for delivery off-chip. The **time-over-threshold** (ToT) is calculated by sampling the signals each 500ps, until their amplitudes sink again below the defined threshold values. The system delivers in this way the arrival time of validated signals and their time-over-threshold, additionally labeling the SiPM detector that first triggered the event.

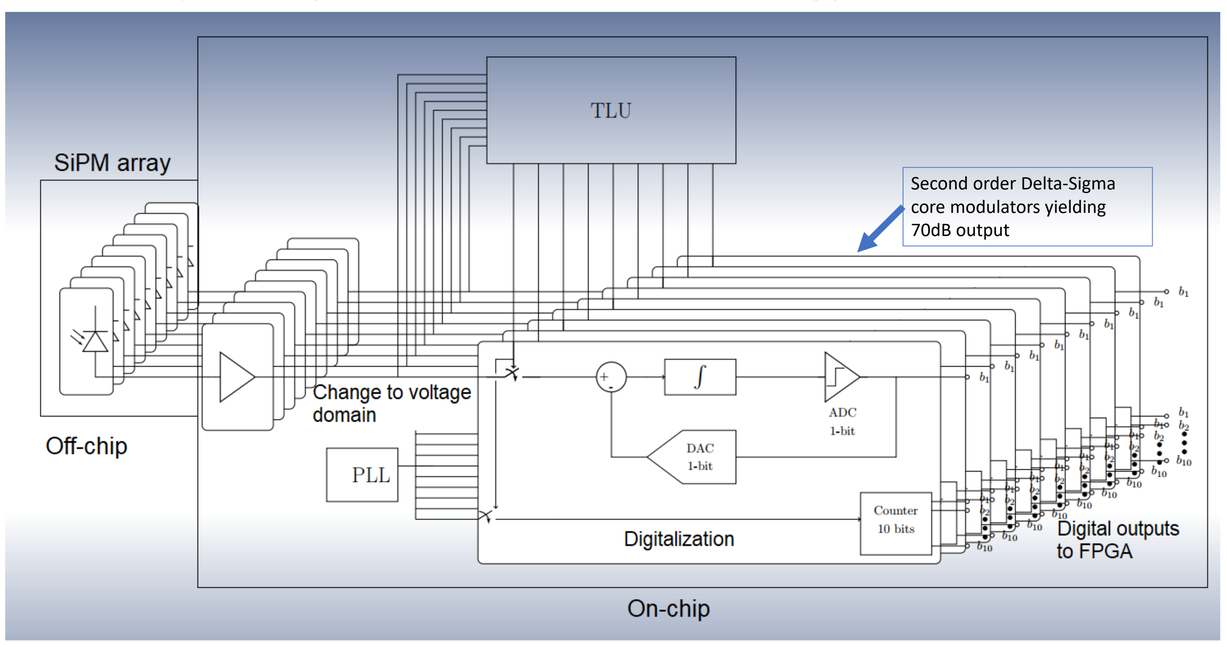

Fig. 1. Operational diagram of the proposed MexSIC-chip, the core element of the MexSiC SiPM DAQ system.

The input signals are furthermore modulated in time using the 2GHz filtering and modulating core unit of a **Delta-Sigma (*ΔΣ*) ADC,** delivering 1 bit output pulse trains. An on-board **FPGA** performs low-pass digital filtering and down-sampling of the oversampled signals delivered by the ΔΣ ADC, finally storing two additional digital output signals: the sampled shape of the **original SiPM input signals**, and the integral over time of these signals, performed in digital domain, yielding the **total amount of charge** in each validated signal.

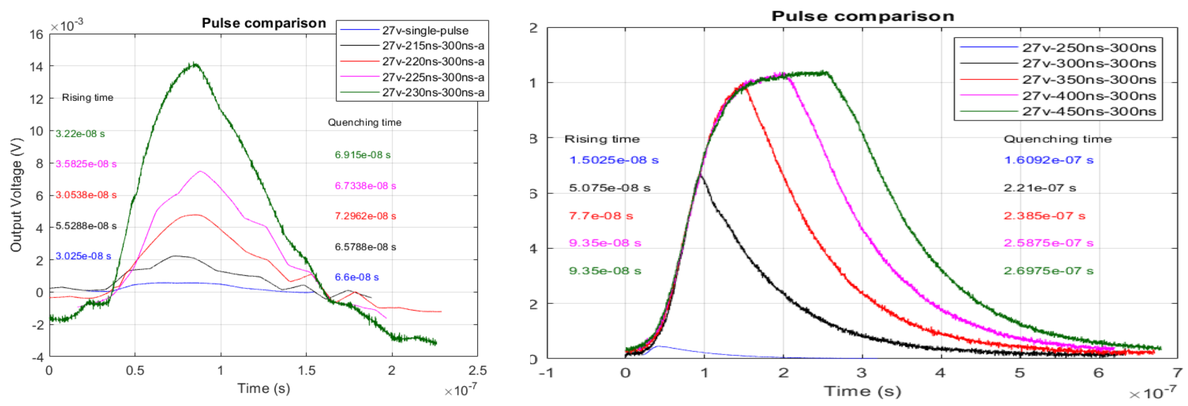

Fig. 2. SiPM output for different LED illumination pulse durations.

Results

The following figures show the TDC and QDC output signal shapes as well as the digital output delivered by the FPGA (*Xilinx Kintex-7*) unit.

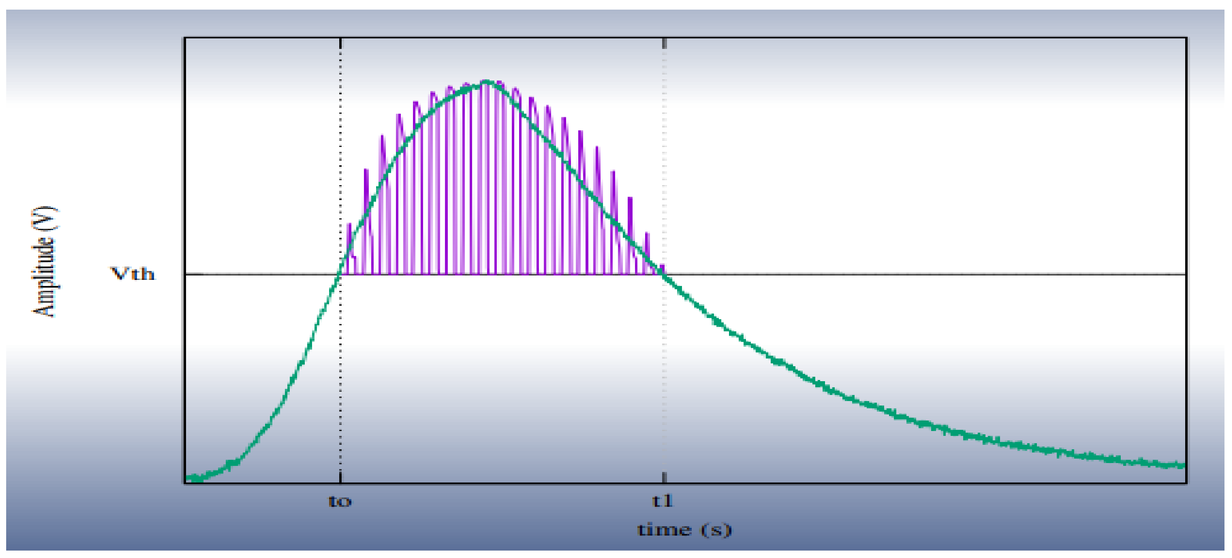

Fig. 3. TDC output signal shape.

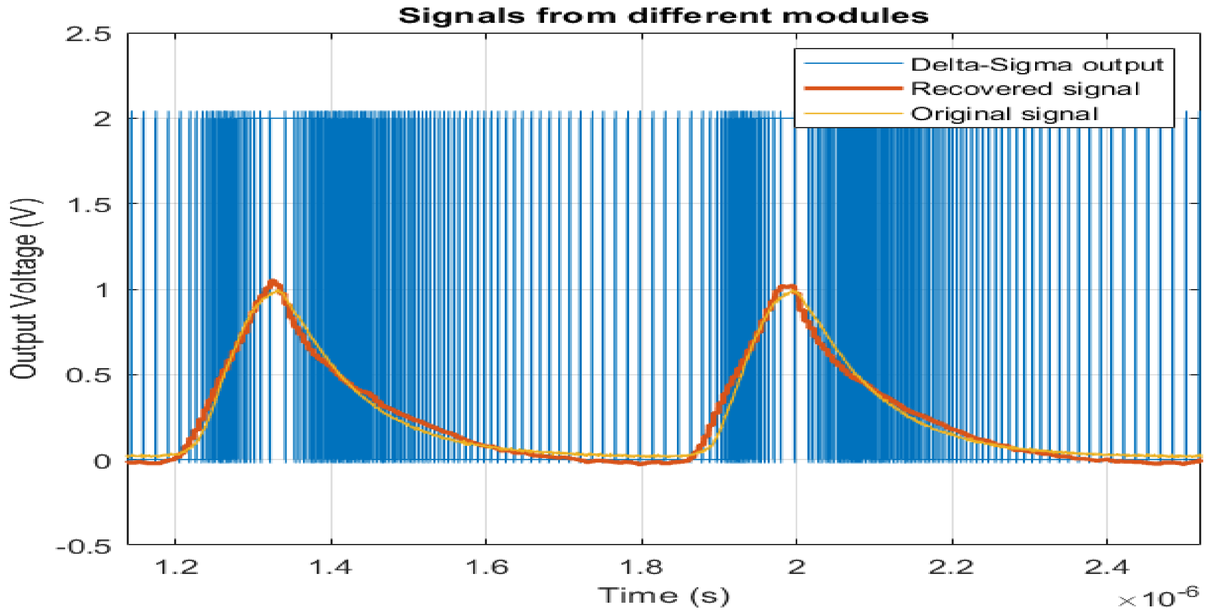

Fig. 4. The blue signal in the graph is the 2V rail-to-rail* Delta-Sigma (*ΔΣ*) ADC core unit *1-bit output digital signal generated in the MexSIC chip, obtained for the original SiPM analog pulses plotted in yellow. The orange line represents the 12-bit fully digitized output signal obtained after proper processing (and decimating) at the FPGA. The 12-bit fully digitized recovered signal represents in this case a standard deviation of 0.28 if compared to the original analog SiPM input signal. The whole system runs at 2GHz frequency.

Conclusion

The analog SiPM DAQ system designed for several parallel input signals (72) features the application specific integrated circuit MexSIC, fabricated in a 180nm commercial CMOS technology, as its core element. The MexSIC, with 9 input channels working in parallel, was conceived and simulated to run at 2GHz frequency, yielding event triggering times with 500ps time-resolution, 10-bit event time-over-threshold information, 12-bit ΔΣ ADC digital reconstruction of the SiPM input signals, as well as 12-bit digital event charge information.

References

[1] http://sensl.com/products/j-series/, visited on April 5, 2019