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The SEU and TID characterization of a novel X-CHIP-03 monolithic pixel detector

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The presented study concerns the effects of cumulative and transient ionizing radiation damage on the novel monolithic pixel detector, X-CHIP-03 [1], manufactured in a 180 nm SoI technology. The X-CHIP-03 contains analog and digital parts, where the latter includes a long shift register useful for SEE measurements. Its predecessor X-CHIP-2 [2], manufactured in the same SoI technology, contains transistor testing matrices for TID measurements.

A high-flux Co-60 medical radiation source was used for the TID measurement. The samples under irradiation were placed in a Pb/Al enclosure, which provides an approximate electron equilibrium. This study compares the effects of two different dose rates of 16 Gy/min and 460 Gy/min on the threshold voltage shifts of the CMOS transistors of different geometries as well as the effects on the off-state and maximal current. Moreover, the effects of placement in HV P-wells are studied. In addition, integral current consumption of the device was measured and it was found to be correlated to the increase of the off-state transistor current. The test structures were irradiated up to a dose of 38 kGy (low dose rate measurement) and 100 kGy (high dose rate measurement). The measurement showed that the radiation effects are negligible up to a threshold TID of 1.6 kGy. A consistent annealing behavior was observed in both transistor test structures and ASIC circuits.

The SEE study was performed using heavy charged particles produced at Tandetron (NPI Rez, Czech Republic) and U400M (JINR, Dubna, Russia) accelerator complexes. While the Tandetron accelerator was used as a source of He-4 and Li-7 ions, the isochronous cyclotron U400M was the source of accelerated Ne-22, Ar-40, Xe-136 and Kr-84 ions. The measurements were performed in vacuum for different detector-beamline angular configurations to increase the extent of available LET ranges. During irradiation, a checkerboard test pattern was written into the shift register and the data were read-out periodically and analyzed off-line. A bit-flip cross section as a function of particle LET was measured for the D-flip flops, which make up the shift register in the X-CHIP-03 ASIC.

[1] Havranek, M., et al., X-CHIP-03: SOI MAPS Radiation Sensor with hit-counting and ADC mode, submitted for publication to the Conference Record for the 2018 IEEE NSS/MIC/RTSD.

[2] Havranek, M. et al., MAPS sensor for radiation imaging designed in 180 nm SOI CMOS technology, 2018 JINST 13 C06004.

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