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Implementation of the interpolator for signal peak detection in read-out ASIC

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One of the trends in the development of front-end electronics is a digitization of analog signals at the earliest stage, followed by their application specific processing in digital domain. Digital processing allows to filter data, remove uninformative or spoiled data, detect overlays and calculate of peak signal. The processing functions are usually assigned to the remote data acquisition system. The stream of digital data coming from read-out ASIC can easily reach a few Gb/s. To reduce the output data flow, it is required the selective digital signal processing, being built-in the ASIC.
For peak detection inside read-out ASIC with high resolution (e.g. 10 bit) for fast signal (e.g. one coming from shaper with peaking time 100 ns), sampling rate must be very high –at least 100 Msps. In this case high-speed ADC will have high power consumption, which is usually inappropriate for low-power read-out channel.
To determine the signal maximum (peak) with the required accuracy (amplitude resolution), it is proposed to use an interpolation. The interpolation allows to find the fit function of a curve that passes through a given set of points. Knowing the equation of the curve, it is possible to calculate the values of the function at intermediate points in the area of the desired maximum of the signal. This will allow to find peak with necessary accuracy, reduce the required sampling rate of the ADC and finally minimize the output data volume.
Comparison of various interpolation methods has shown that interpolation of polynomials in the Lagrange form is most appropriate. This type of interpolation gives high accuracy and is not resource-intensive in its implementation.
The accuracy of the coincidence of the obtained curve with the desired one (the output response of the shaper) is determined by the set of points (the location of the points relative to the signal peak and their number), as well as the accuracy calculating of the coefficients for polynomial.
The behavioral modeling of the interpolator was carried out with variation of the design parameters such as shaper peaking time, ADC sampling rate, upsampling coefficient (count of intermediate points). Method of choosing the optimal parameters for required peak amplitude error is described. Simulation results showed that interpolator usage allows to achieve the accuracy of peak determination < 1 LSB for 10 bit ADC with 30 MHz sampling rate at shaper peaking time 200 ns. The implemented interpolator has polynomial of 6-th degree and uses 3 upsampling points, that is equivalent to 120 MHz ADC using. The interpolator is described as a building block for the read-out ASIC in UMC 180 nm MMRF CMOS process.

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