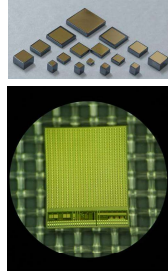


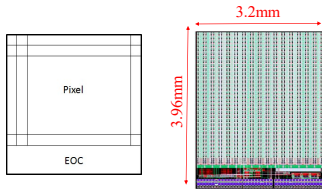
Introduction

- Spectral X-ray Photon-counting imaging
 - Noise suppression
 - Image quality
 - Material discrimination
- Cadmium Zinc Telluride(CdZnTe)
 - High atomic number
 - Proper band-gap energy
 - Operational at room temperature
 - Ideal for hard X-ray and gamma-ray detection
- Pixelated readout ASIC



Architecture and Specification

Overall architecture



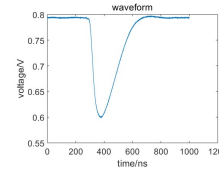
- the pixel array makes the majority of the ASIC
- End-Of-Column(EOC) circuit is placed on the bottom

Main design specifications

design specification	value
pixel size	100 μ m \times 100 μ m
array	32 \times 32
power consumption	<100 μ W/pixel
gain	70mV/fC
dynamic range	10fC
ENC	<100e ⁻ @C _{in} = 100fF
pulse width	200ns
energy window	2
counter	12bit
readout frame rate	1kHz

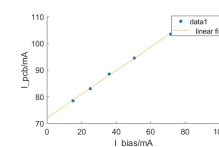
Test Results

Waveform



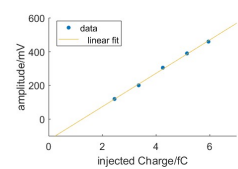
- Pulse width=200ns

Power consumption



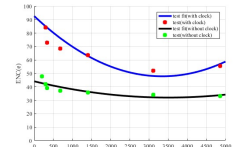
- power consumption=38.9 μ W/pixel

Gain



- (Estimated) gain =79.8mV/fC

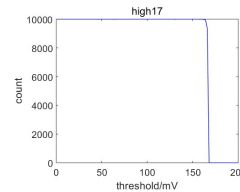
Noise



- ENC < 100 electron

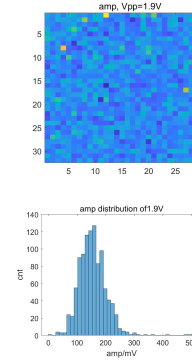
S-curve fit

S-curve

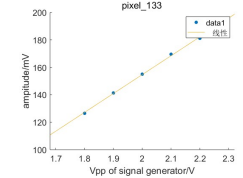


- ✓ Measured with different amount of charge injection
- ✓ Fitted with Gaussian cumulative distribution functions
- ✓ Sigma: spread of the signal amplitude
- ✓ mu: average value of the signal amplitude

Average value distribution



Linearity

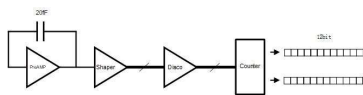


- ✓ Each pixel: average value versus the amount of charge injection
- ✓ Fitted with linear functions
- ✓ slope: charge-amplitude gain
- ✓ intercept: uniformity of baseline

ASIC Design

Pixel circuit

- Block diagram



- ✓ One low-noise charge sensitive preamplifier
- ✓ One CR-RC shaper
- ✓ Two discriminators
- ✓ Two 12-bit counters
- ✓ Several registers

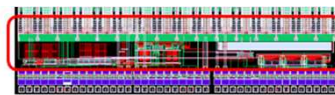
Layout



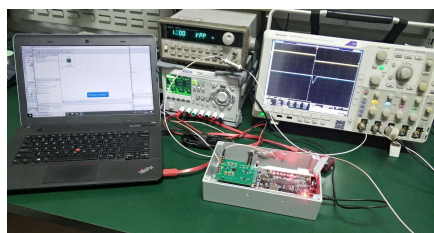
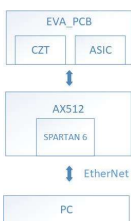
- ✓ The analog part and the digital part are divided by slow control registers
- ✓ Mirror placement of two adjacent columns of pixels

EOC circuit

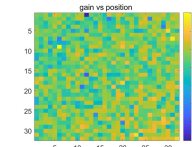
- ✓ Bias generation
- ✓ Slow control
- ✓ Data readout control



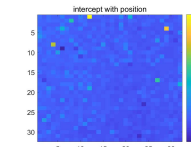
Test Systems



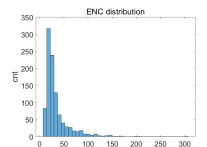
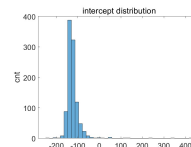
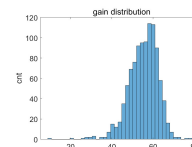
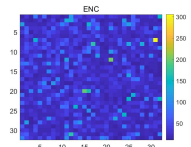
Gain distribution



Intercept distribution



ENC distribution



Summary & Future Plan

- A pixelated photon-counting ASIC was developed. The prototype chip was evaluated. The power consumption was measured to be 38.9 μ W per pixel. The gain of the analog front-end was approximately 79mV/fC and the ENC was less than 100 electrons for different shaping times and the input capacitance of about 100 fF. The results showed that our chip worked well and agreed with our design specifications.
- Test of the new version prototype chip with larger pixel array and more functions.
- Test of the prototype chip bump bonded with CdZnTe detector.

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