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Development of a pixel readout ASIC for CZT detectors for spectral X-ray photon-counting imaging applications

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This paper presents the development of a prototype pixel readout ASIC for CZT detectors fabricated in a 180 nm CMOS process. It consists of a 32×32 array of pixels in 100 um pitch and the EOC (end-of column) circuit for control and data readout. Each pixel integrates a charge sensitive preamplifier, a CR-RC shaper, two discriminators, two 12-bit counters and registers, allowing us to acquire and readout images simultaneously. A local 6-bit register has also been integrated for each pixel for calibration enable and threshold fine tuning, which can be programmed through a SPI slow control interface.
A dedicated chip evaluation system was developed and the initial test results showed the chip worked well. The power consumption was measured to be 38.9uW per pixel, which could be adjusted by a master bias unit. The gain of the analog front-end was approximately 79mV/fC and the ENC was less than 100 electrons for different shaping times and the input capacitance of about 100 fF. The results were in good agreement with our design specifications. More detailed design and test results will be discussed in this paper.

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