HARDROC2B: A Readout ASIC for INO-ICAL RPCs

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Overview

Introduction

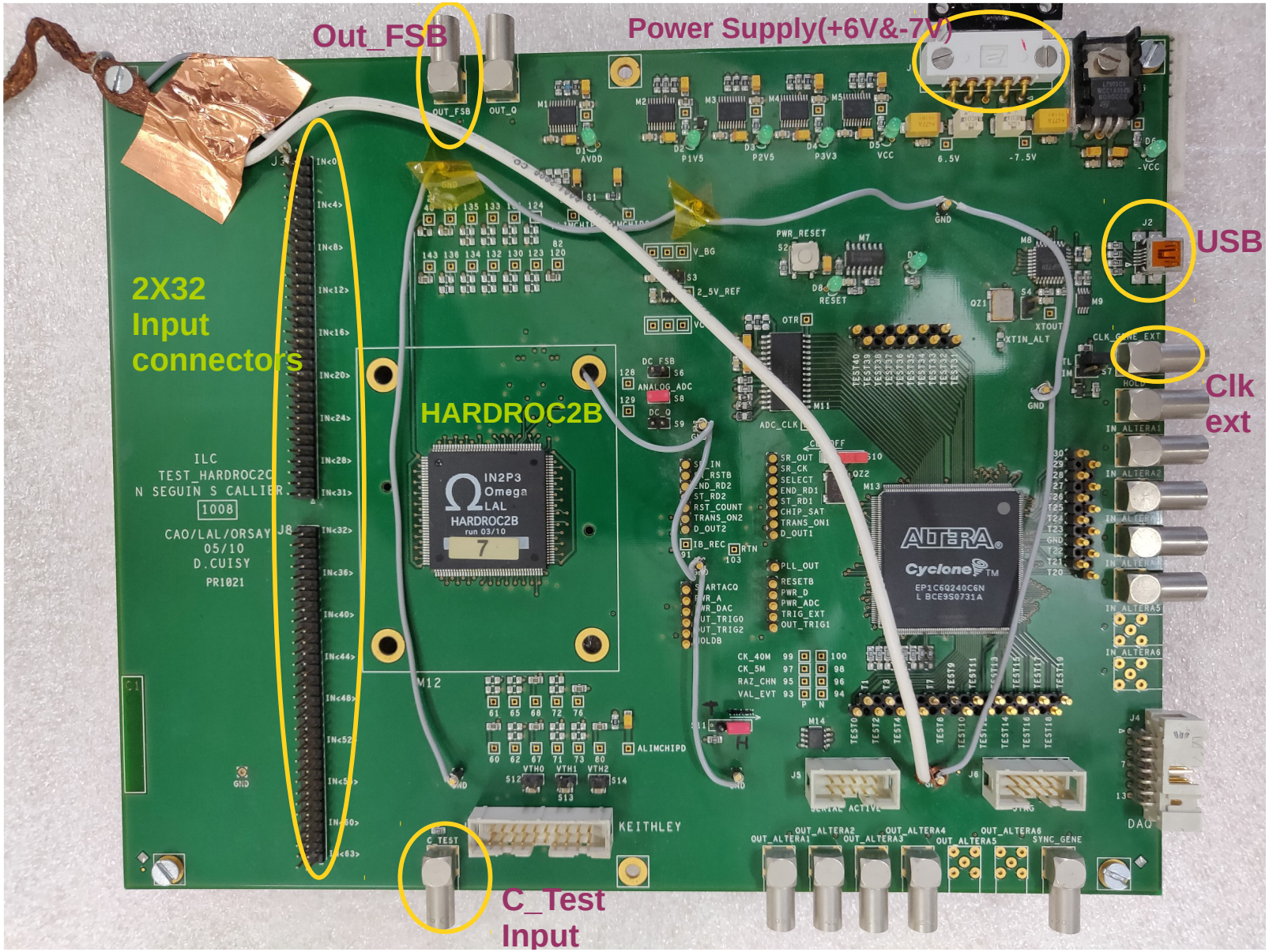
In order to achieve the physics goal, the complete ICAL detector in the future will require more than 3 million readout channels. A challenge is to cope with such a tremendous amount of external connections and cables and to reduce the power consumption to the lowest level.

Such a large number of channels require an efficient, robust and cost-effective readout system.

In view of this, the University of Delhi group tested and commissioned multichannel system HARDROC as an readout option for the ICAL RPCs.

HARDROC (Hadronic Rpc Detector ReadOut Chip) is a 64-channel front end ASIC designed primarily for the readout of gaseous detector like RPCs.

Testboard

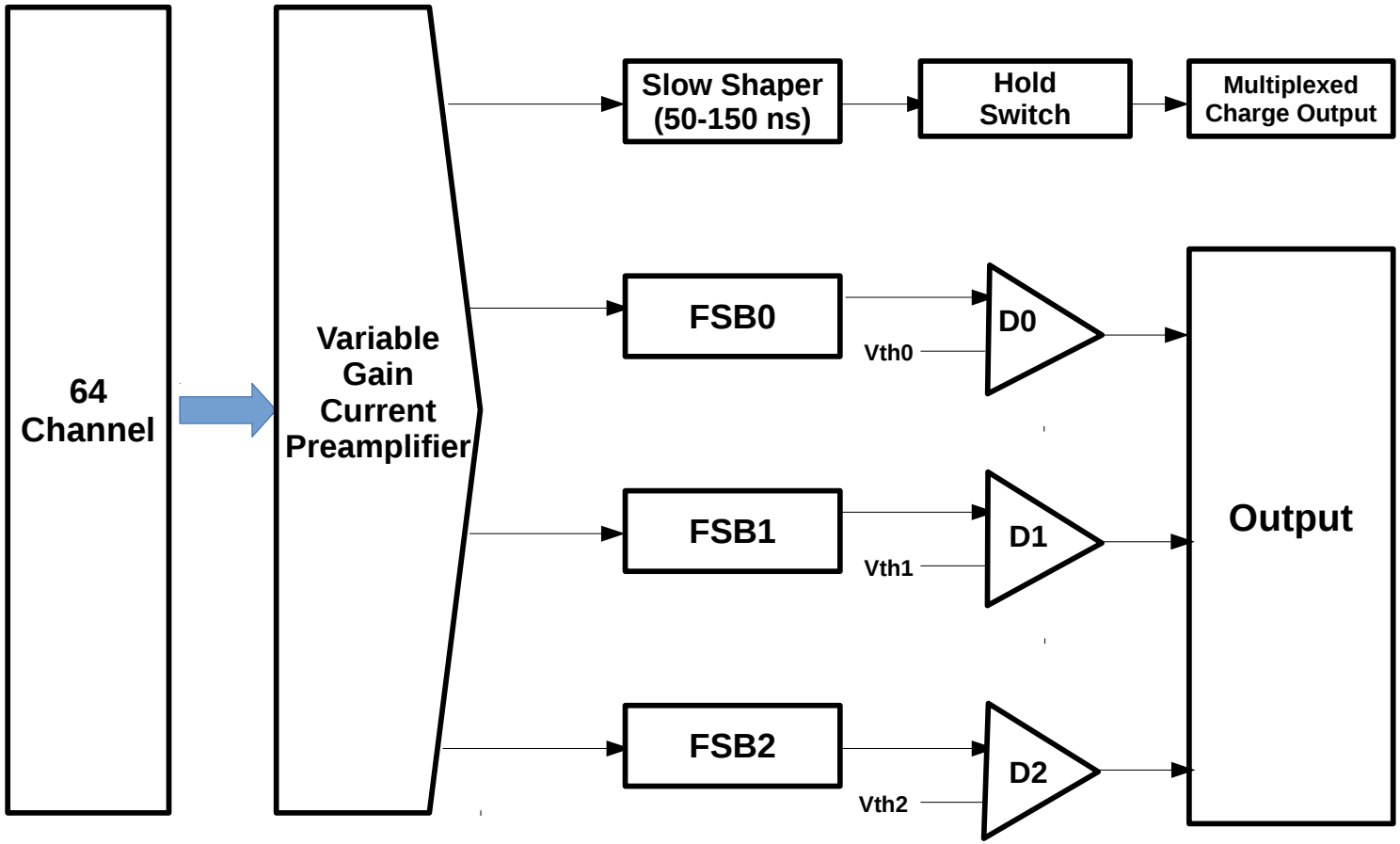

Out_FSB
Power Supply(+6V&-7V)
USB
2X32
Input
connectors
HARDROC2B
Clk
ext
C_Test
Input
IN2P3
Omega
LAL
HARDROC2B
run 03/10
ALTERA
Cyclone
EP1C6Q240C6N
L BCE9S0731A
KEITHLEY
DAQ

Characteristics of HARDROC

The 64 channels of the HARDROC2 are made of:

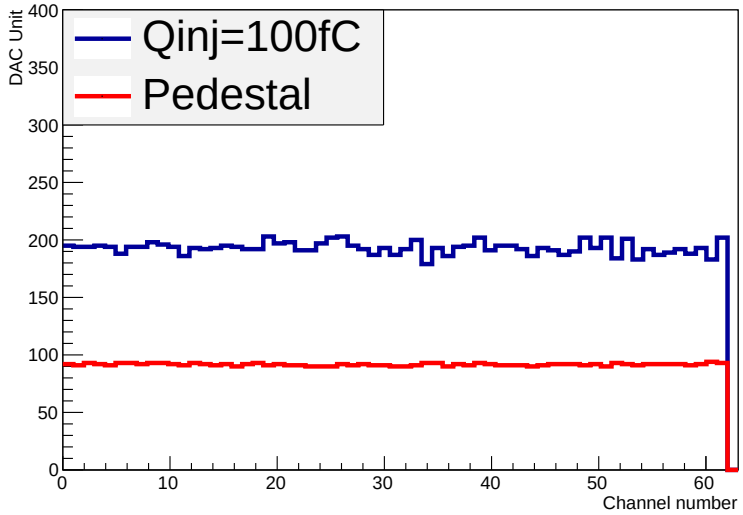
- A fast low impedance current preamplifier with 8-bit variable gain (analog G=0 to 2)
- A variable slow shaper (50-150ns) followed by a Track and Hold buffer to provide a multiplexed analog charge output up to 10pC
- 3 variable gain CRRC fast shapers (peaking time 20-25 ns)
  FSB0 is dedicated for input charges from 10fC up to 100fC
  FSB1 for input charges from 100fC up to 1pC
  FSB2 for input charges from 1pC up to 10pC
- 3 low offset discriminators
  3 internal 10 bit- DACs to set the thresholds
  3 discriminators are sent to a 3 input to 2 output encoder.

Synoptic layout of HARDROC2 chip

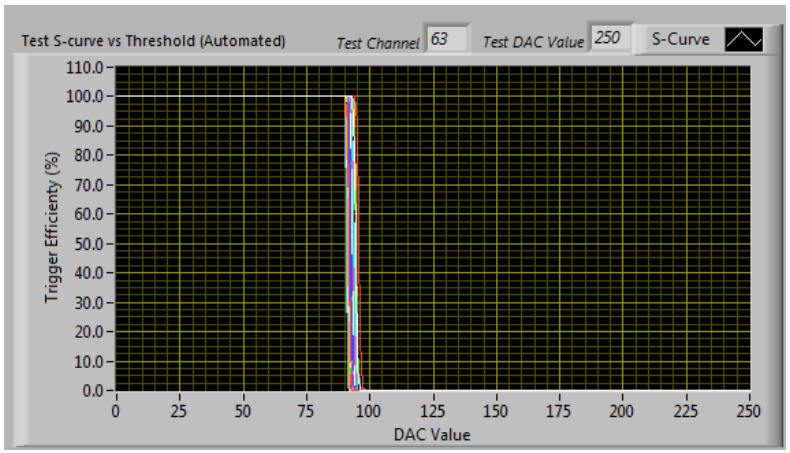


FSB: Bipolar Fast Shaper
D0,D1,D2: Discriminators

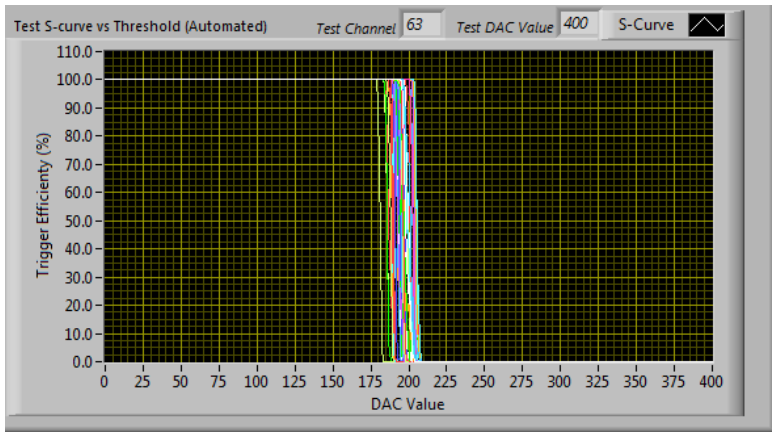
S-Curve



Threshold value in DAC units corresponding to 50% efficiency of the curve

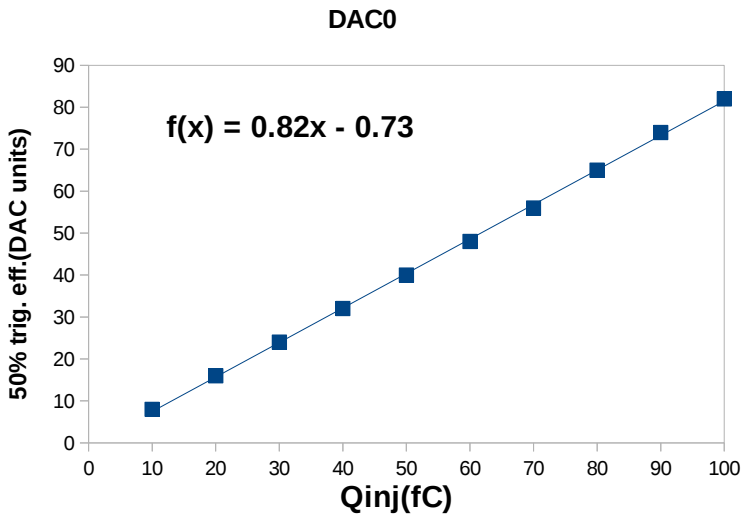


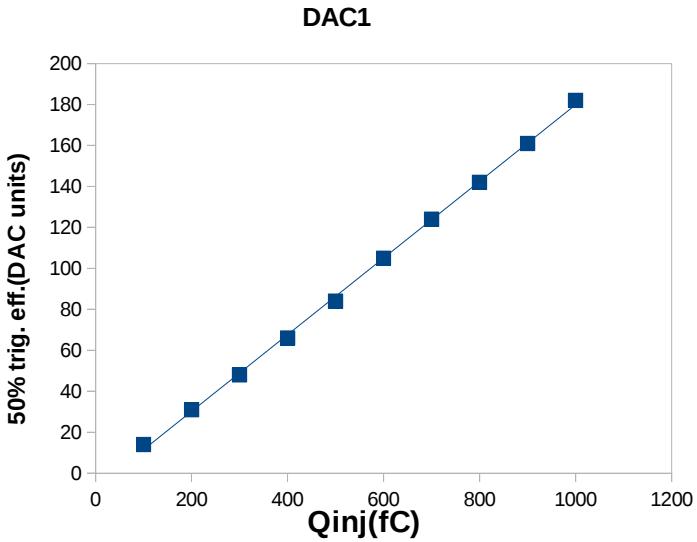
S-curve: dispersion of 64 pedestals

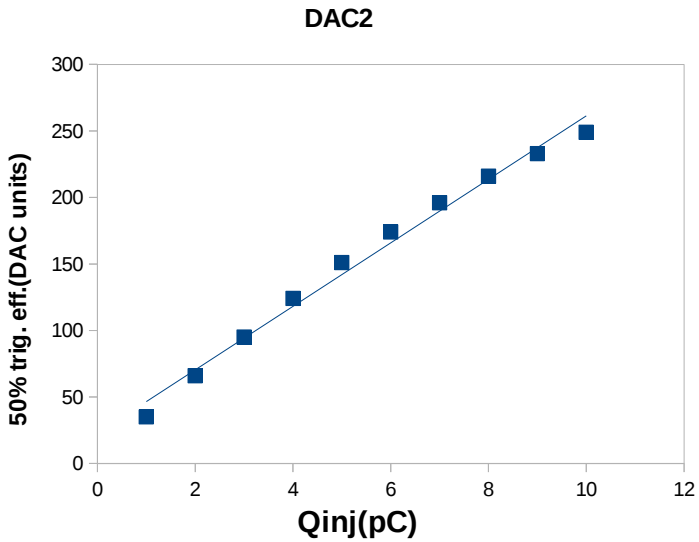


Injected Charge=100fC

FSB Linearity

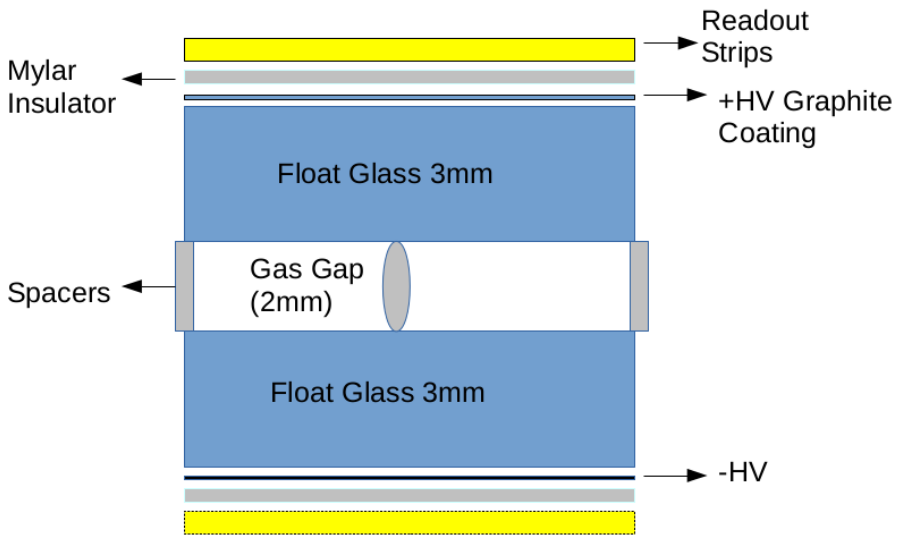






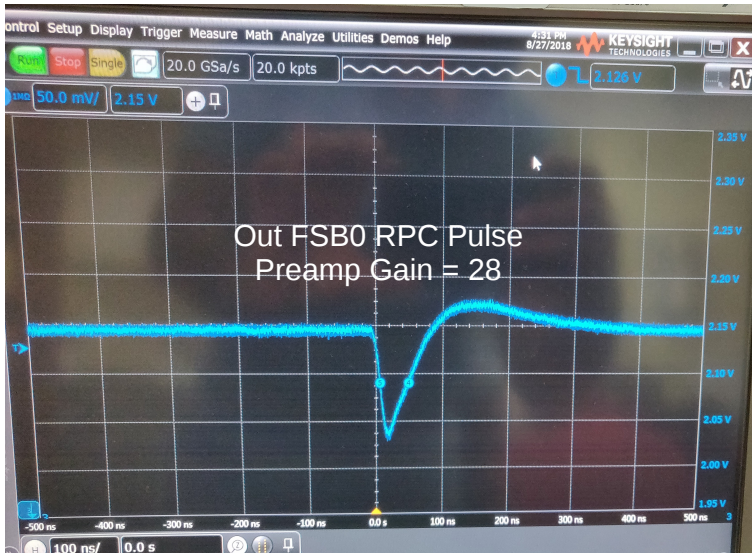
RPC Detector

- RPC: Low cost, Simple, Reliable, Large uniform surface area coverage
- Avalanche Mode
- Gas Mixture :
  95% R134a(TFE)
  4.5% CO2(γ quencher)
  0.5% SF6(e quencher)
- Chamber: 30cmX30cm
- Glass: Saint-Gobain
- Copper readout strips(3cm pitch)

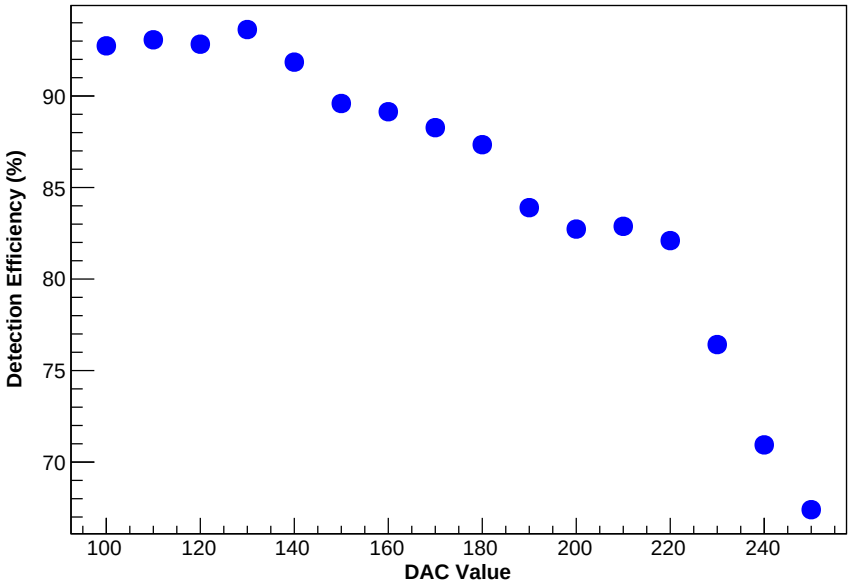


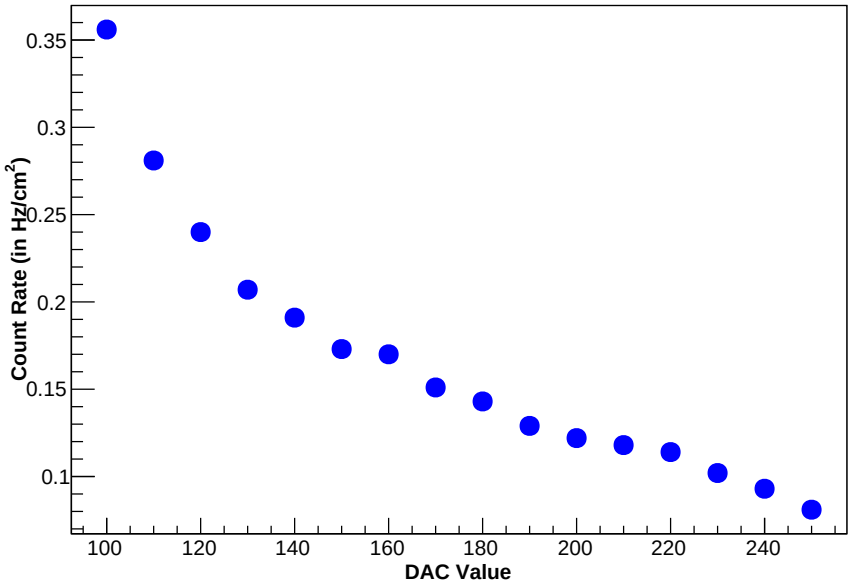
RPC/HARDROC pulse

Detector Read-out	RPC
No of Channels	64
Polarity	Negative
Dynamic Range	10fC-10pC
Power Consumption	$10\mu W$/channel
Input	64 current input



Threshold Scan

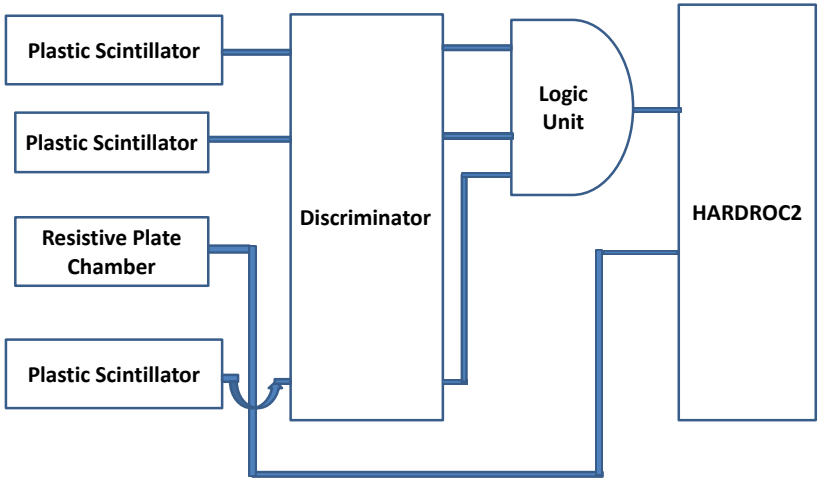


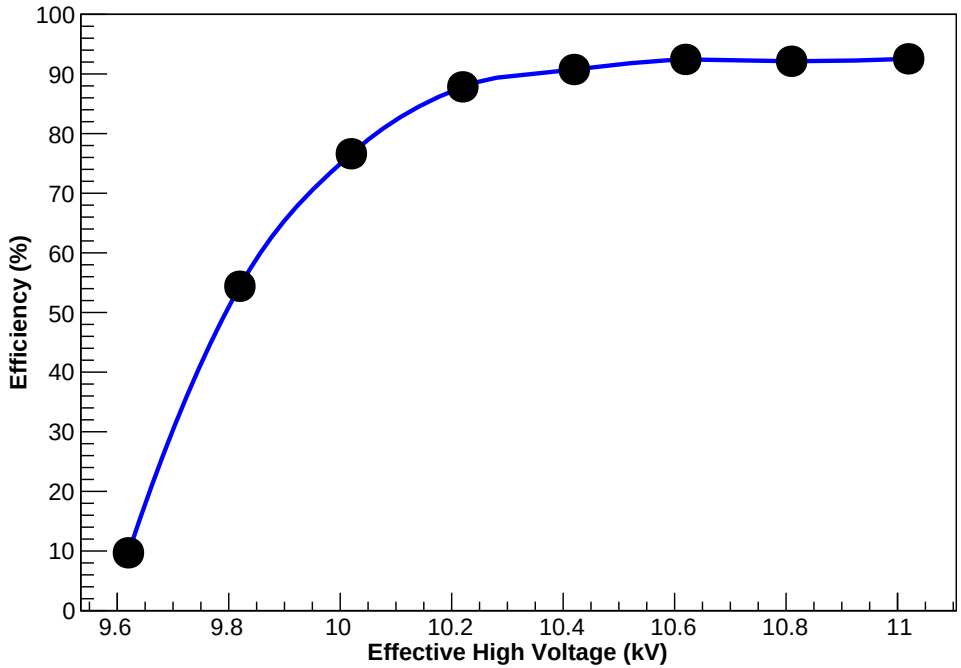


1. Efficiency decreasing down to 70% at 240 DAC value.
2. Count rate moving as expected $\Rightarrow$ lowering as threshold increases

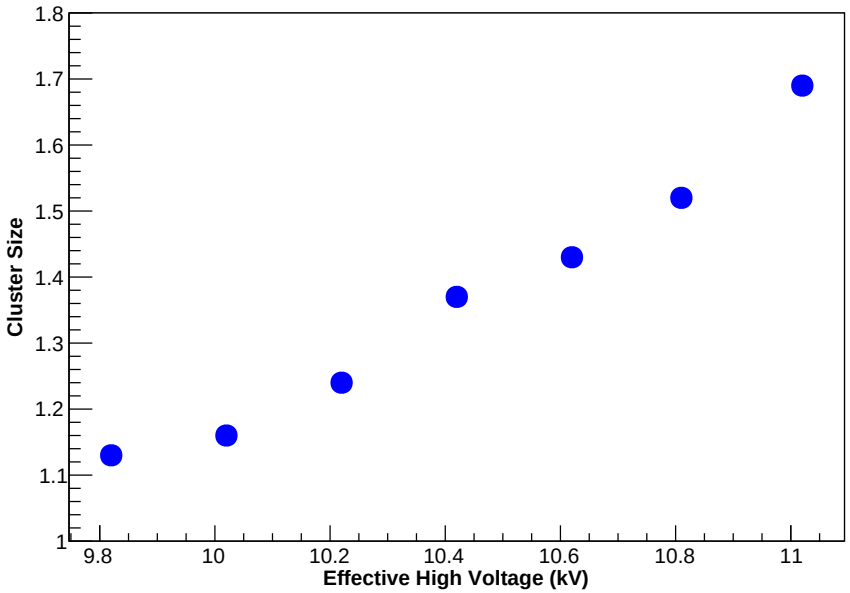
Efficiency

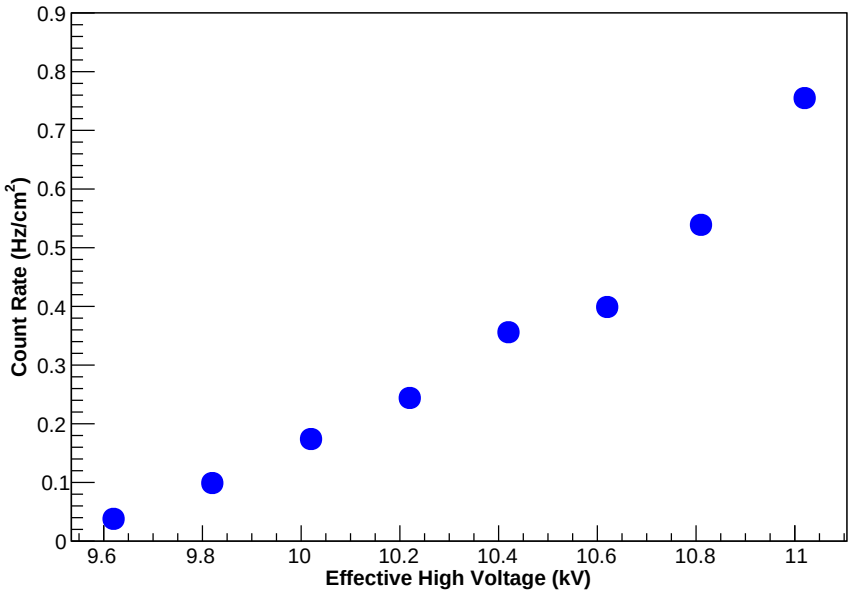
The trigger system is made of three scintillators each couples to a PMT. The detector performance and characterization were carried out by using cosmic ray muons. The efficiency is obtained by evaluating the ratio between the number of events in which RPC strip under consideration has fired to the total number of triggered events in the time window of 200 ns.



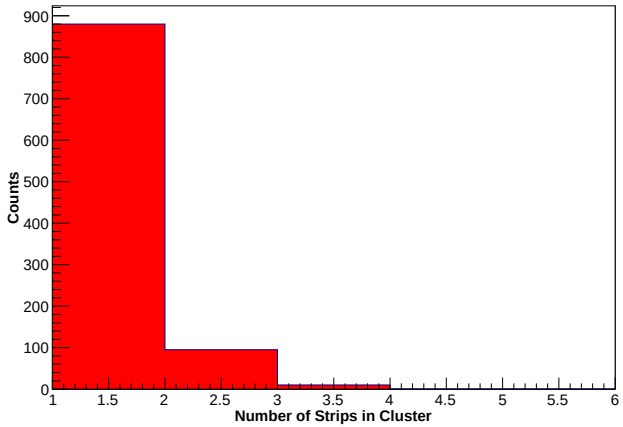


Cluster Size & Count Rate

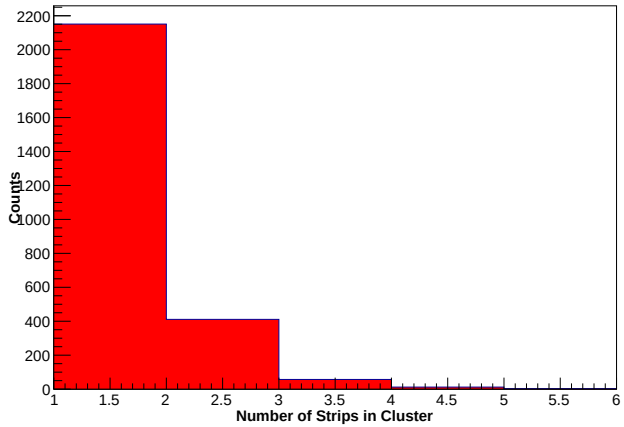




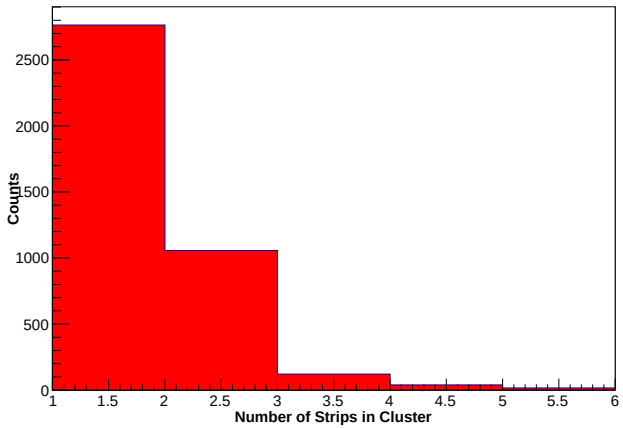
Cluster Size



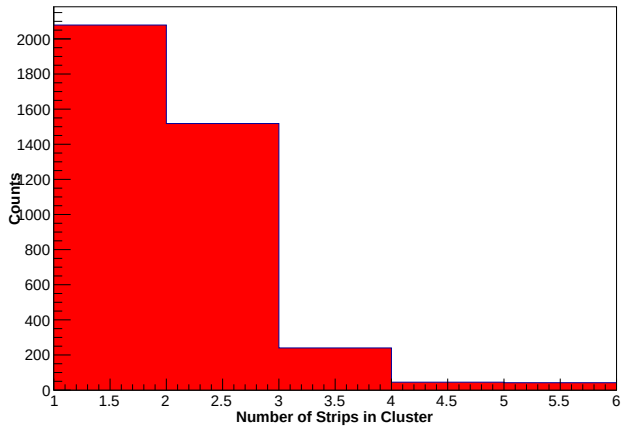
HV=9.8KV



HV=10.2KV



HV=10.6KV



HV=11KV

Summary

DAC Threshold

The pedestals average was found to be around 92 DAC units
A common triggering threshold of 130 DAQ units and 28 gain is used
The choice of the threshold value of 130 DAC allows the detection efficiency to be optimized while keeping the noise rate low

Efficiency

Plateau: 10.22-11.02 KV with efficiency between 88 and 94%

Multiplicity

Lowest multiplicity is preferred with very good efficiency
Multiplicity of ~ 1.4 at 10.42KV

Count Rate

The count rate was measured to be less than $0.8 Hz/cm^2$
The signal contamination is thus negligible

References

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The End