ALICE Inner Tracking System upgrade at the LHC

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High-luminosity program at the LHC in Run3 and Run4

A Large Ion Collider Experiment (ALICE) is specially designed to study the properties of Quark-Gluon Plasma

ALICE Physics goals for Run 3 and 4:

- Parton-medium interaction
- Thermal properties, EoS
- Particle production mechanism

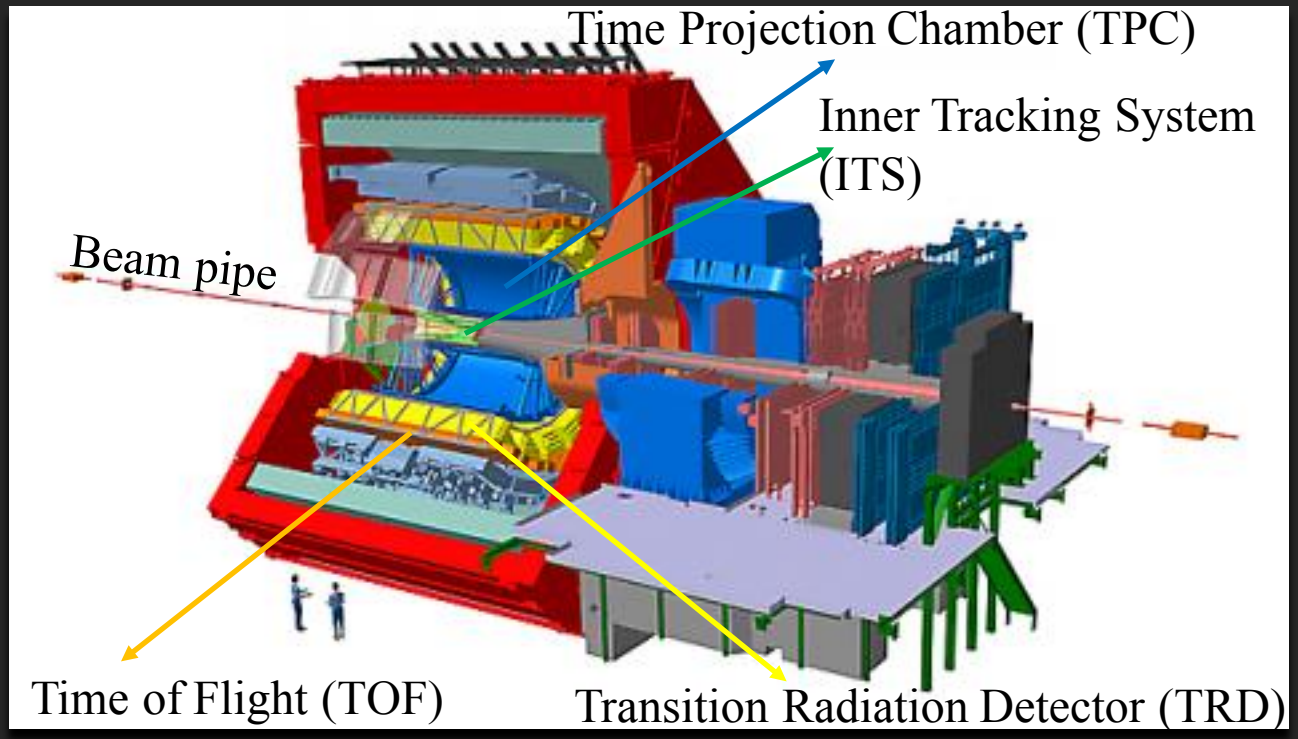
➤ Heavy-flavor and quarkonia measurements down to low p_T
➤ High precision measurement of light and hyper-nuclei

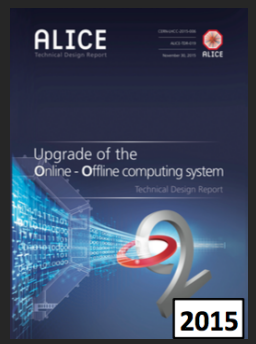
➤ High event statistics.
➤ Precise measurement of vertex.

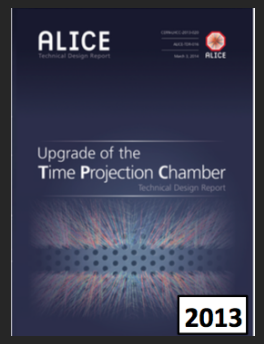
Improve tracking efficiency and vertex resolution => Detector upgrade

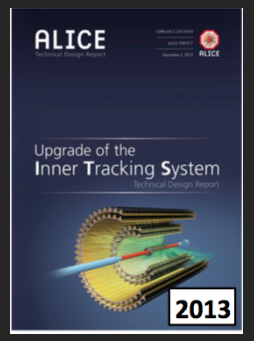
ALICE upgrade plan for Run 3 and Run 4

The ALICE detector (Current setup)





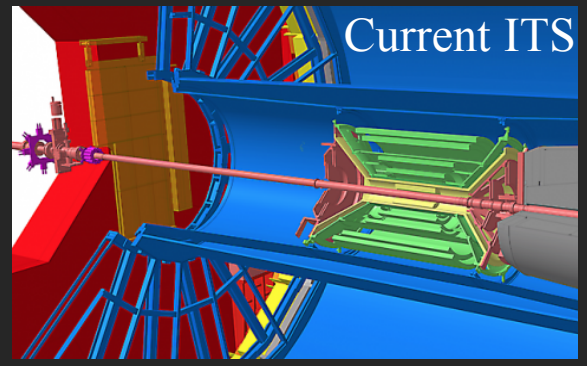


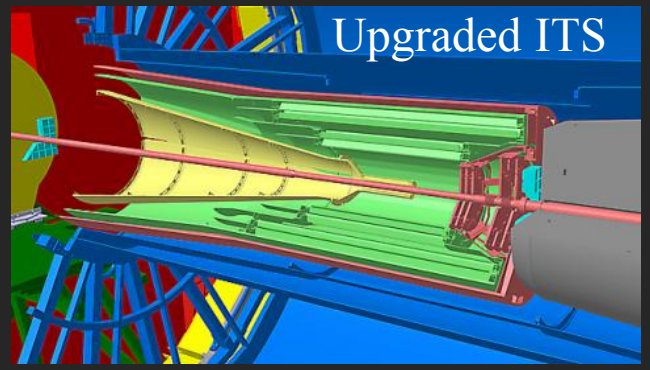


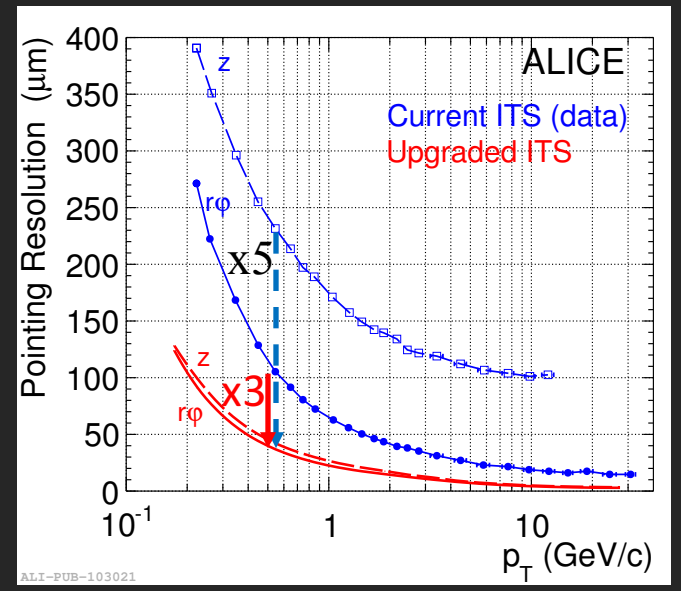
- New TPC readout Chambers (ROCs)
  - Gas electron multiplier (GEM) technology
  - Continuous read-out electronics
- Read-out upgrade:
  - TOF, TRD, Calorimeters
- Upgrade of Online-Offline computing system (O^2):
  - DAQ, Trigger system
- New Muon Forward Tracker (MFT):
  - MAPS technology based COMS pixels
  - Forward tracking
- ITS upgrade:

  Next slide

ALICE ITS upgrade plan for Run 3 and Run 4

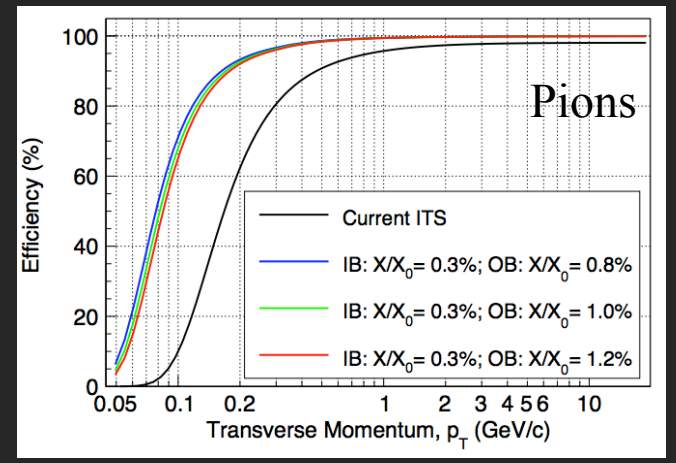






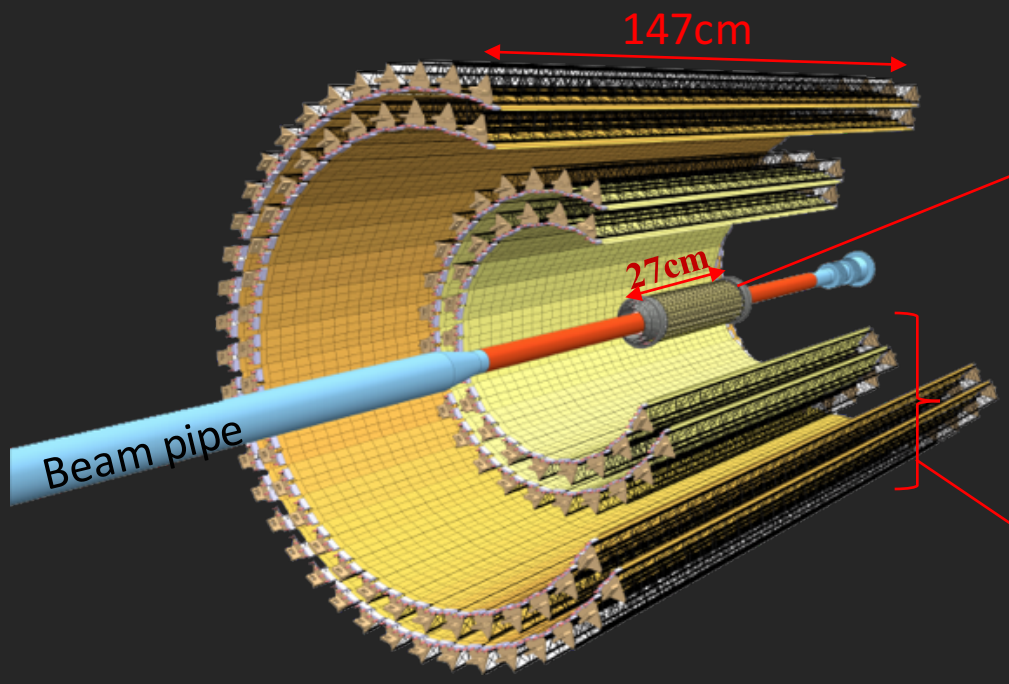
ALICE ITS upgrade objectives: current vs new

- Improve impact parameter resolution
  - Close to beam pipe: 39mm → 23mm
  - Reduce material budget: 1.14%X_0 → 0.3%X_0(inner layers)
  - Reduce pixel size: 50 × 425 μm² → O(30 × 30 μm²)
- Improve tracking efficiency and p_T resolutions at low p_T
  - 6 layers → 7 layers
  - Silicon drift and strips → pixels
- Increase read-out rate
  - 1kHz → 100kHz (Pb-Pb)



ALICE ITS Upgrade TDR
J. Phys. G: Nucl. Part. Phys. 41(2014) 087002

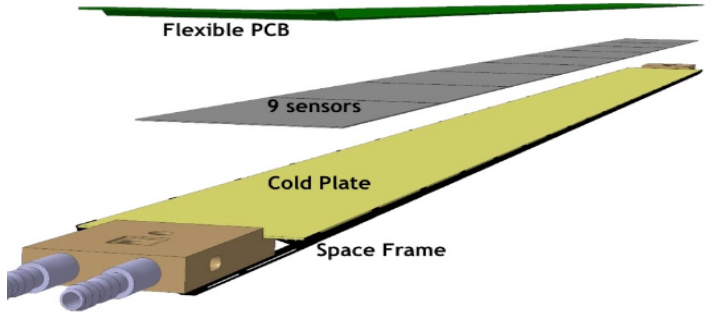
The new ALICE ITS detector



7 layers of Monolithic Active Pixel Sensor (MAPS)

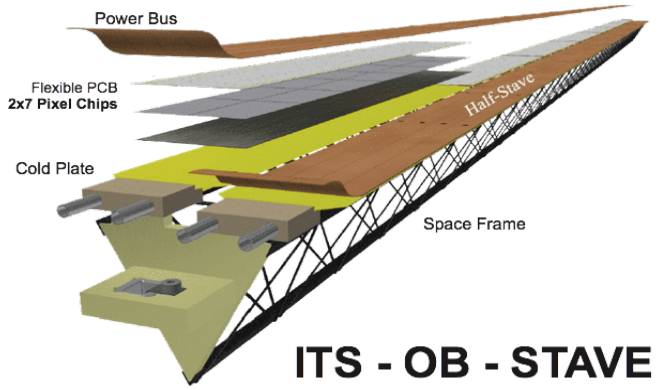
Inner Barrel (IB)

- 3 layers:
  - 12+16+20 (48) staves
  - 1 module per stave
  - 9 sensors per module



Outer Barrel (OB)

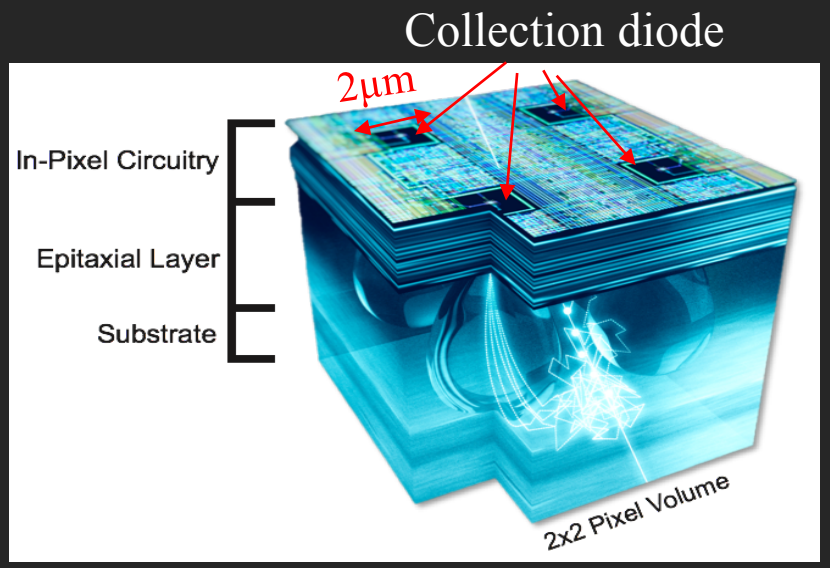
- 2 middle layers
  - 30+24 (54) staves
  - 2×4 modules per stave
- 2 outer layers
  - 42+48 (90) staves
  - 2×7 modules per staves
- 2×7 sensors per module

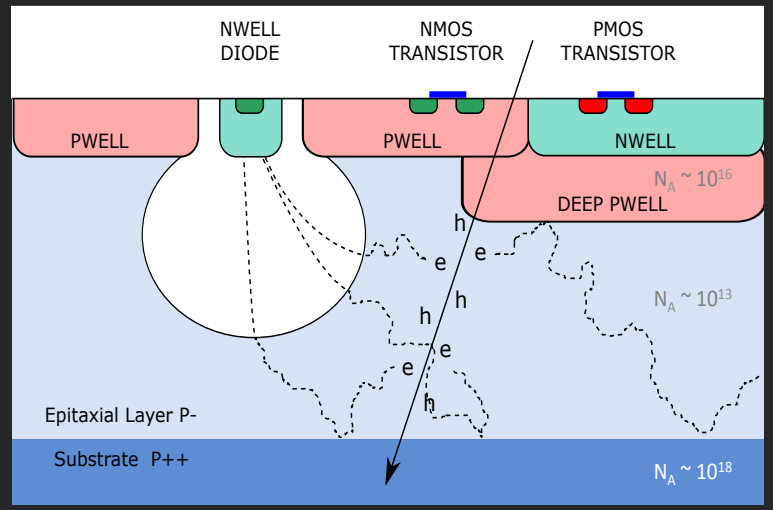


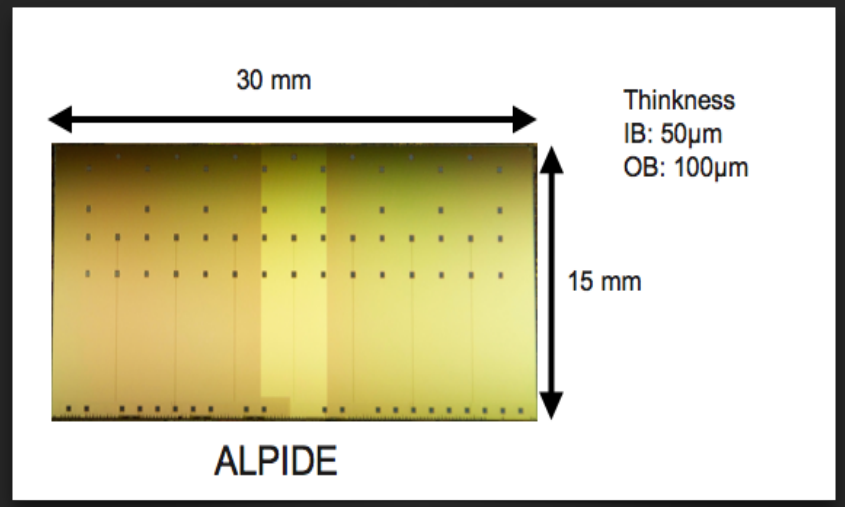
- Total 24k chips
- 10m^2 active silicon area
- 12.5 G-Pixels

The ALPIDE chip

ALice PIxel Detector (ALPIDE)





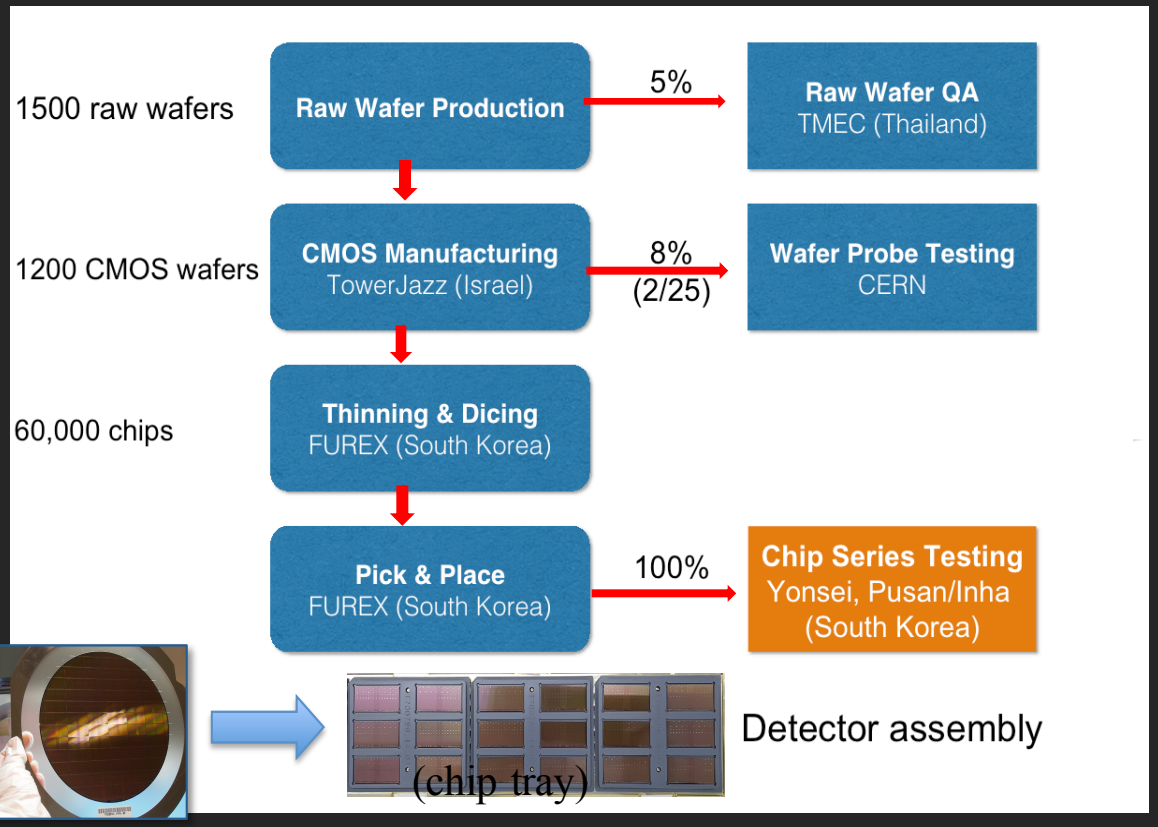


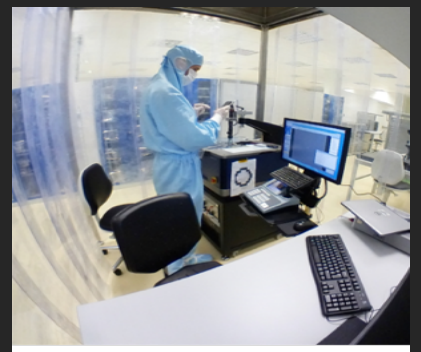
- TowerJazz 180nm CMOS imaging process.
- High resistivity (> 1kΩcm) p-type epitaxial layer on p-type substrate.
- Small NWELL diode (2μm diameter) → small capacitance (~fF).
- Reverse bias voltage to substrate ($-6V < V_{BB} < 0$).
- Deep PWELL shields NWELL of PMOS transistor.
- Full CMOS circuitry within active area.

- Pixel size ($27\times29\ \mu m^2$).
- 1024×512 pixels.
- Max. particle rate: $100MHz/cm^2$.
- Power consumption: ~300nW/pixel.
- Fake hit-rate: 10^{-10} pixel/event.

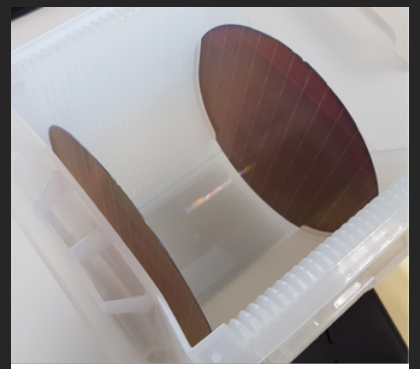
ITS construction: from raw wafer to module assembly

Chip series test

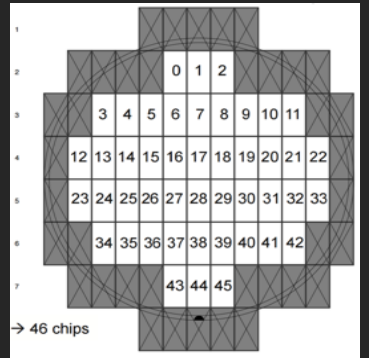




CERN
Wafer Probe Testing



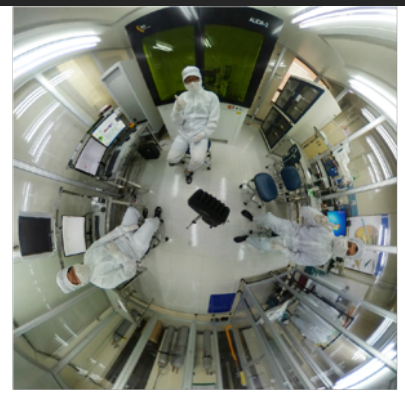
Imaged Wafer



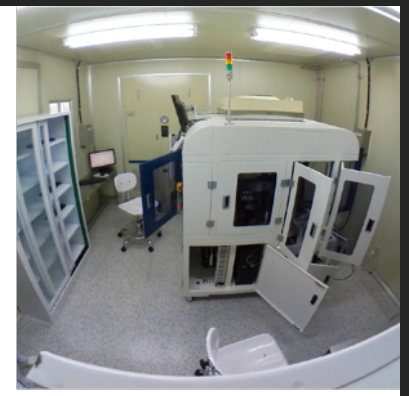
Dicing Diagram

Chip series test: 3 sites

CERN
Chip Test and IB HIC Assembly
50μm ALPIDE



Pusan/Inha
Chip Test and OB HIC Assembly
100μm ALPIDE



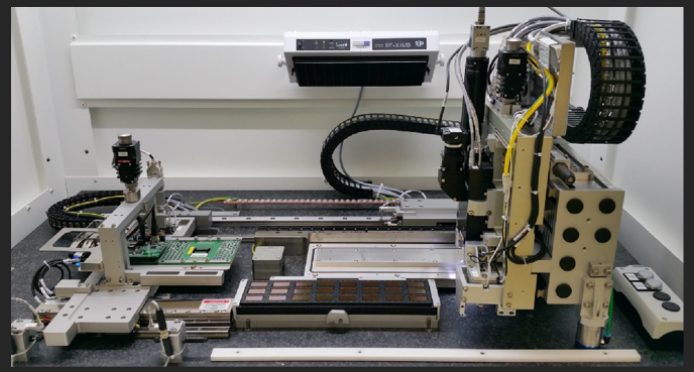
Yonsei
Chip Test
100μm ALPIDE

Chip series test:

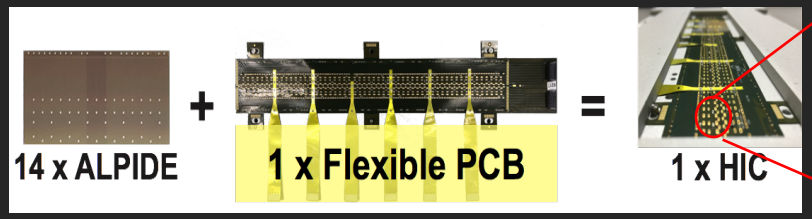
- Functional test of digital and analog circuitries.
- Full characterization of chip including response of every single pixel.

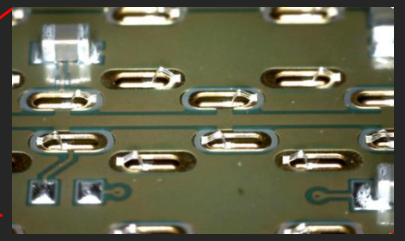
ITS construction: From raw wafer to module assembly

Hybrid integrated circuit (HIC) assembly



(Module Assembly Machine (MAM)





(Wire bonding)

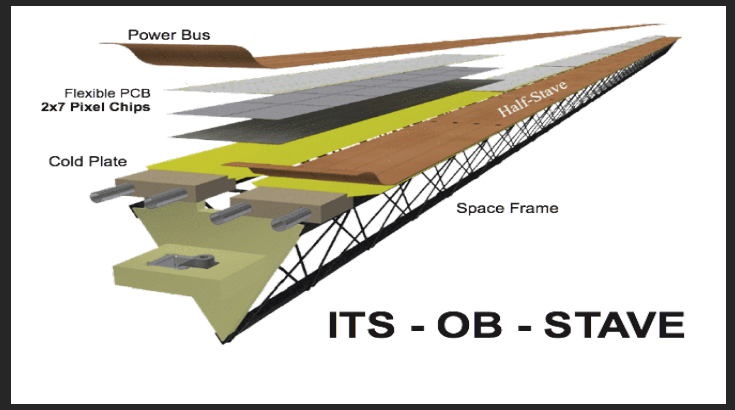
- **HIC assembly:**

Chip alignment (position precision < 5μm)
+ mechanical connection of FPC to chips with glue
+ wire bonding (electrical connections)

- **Assembly sites:**

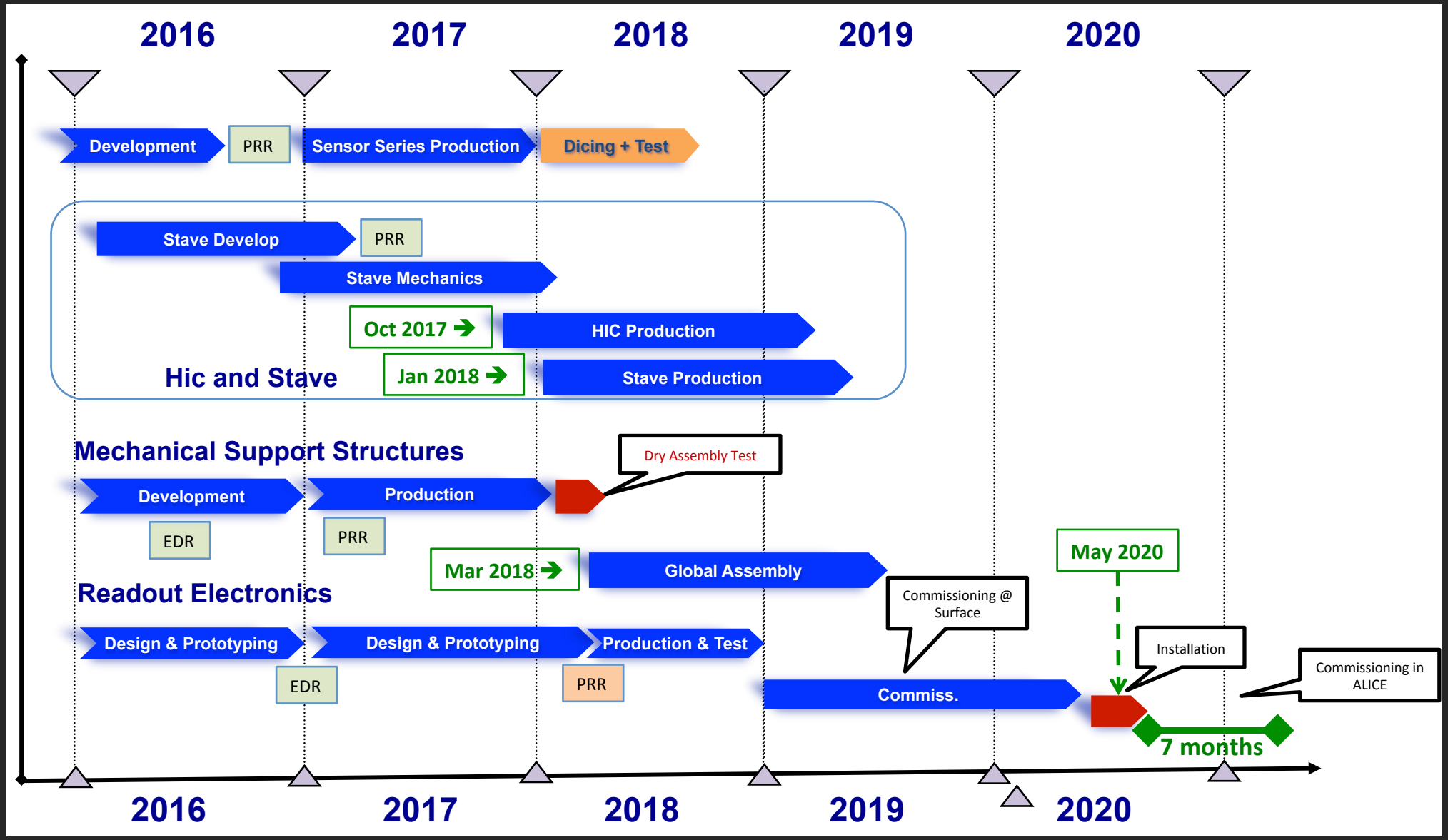
Liverpool, Pusan-Inha, Strasbourg, Wuhan

OB Half stave/stave assembly

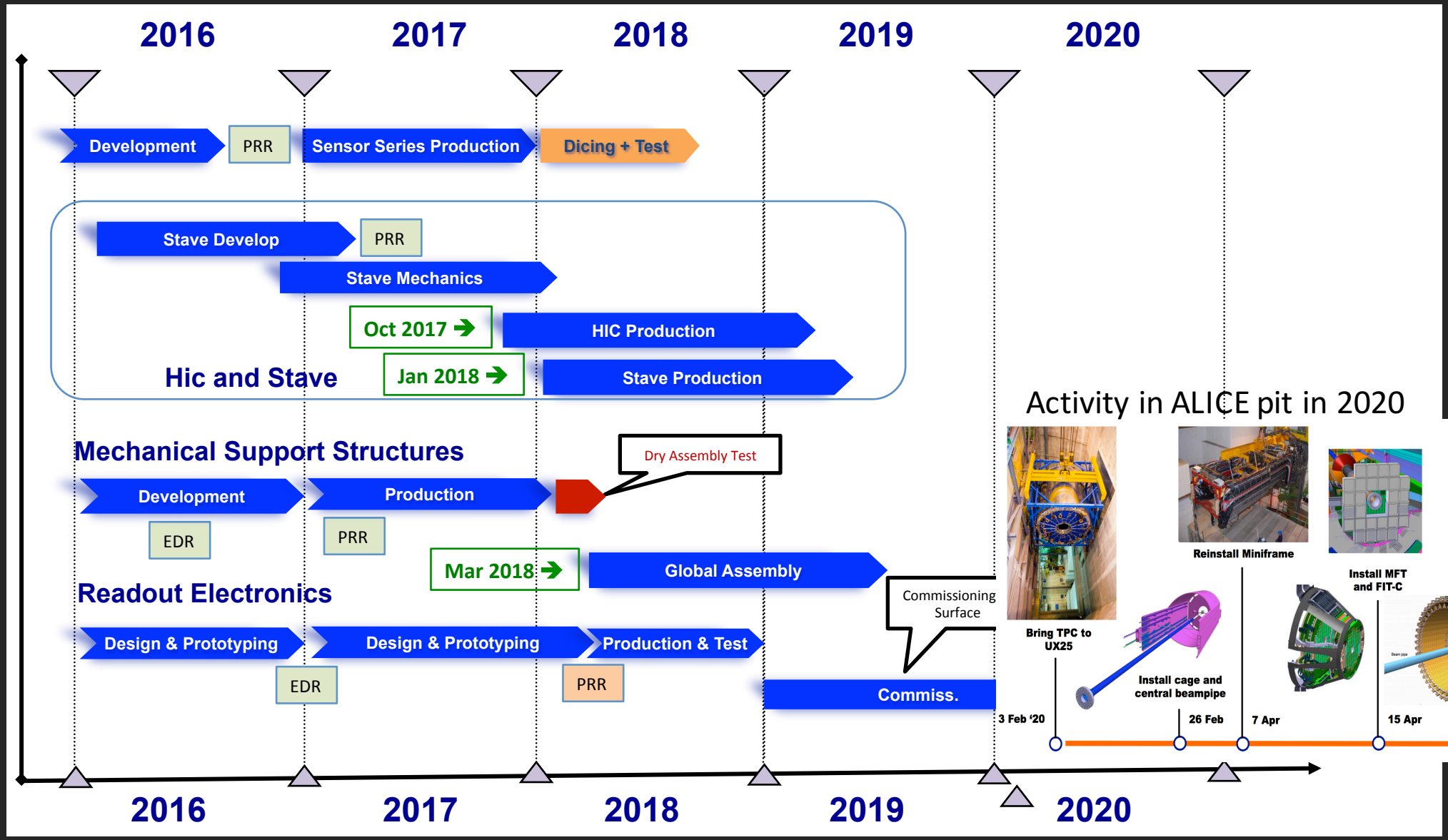


- HICS are aligned and glued to the cold plate (10-20μm precision).
- Soldering of power-bus to cross-cables.
- Half-staves are aligned and glued onto a carbon space frame.
- **Assembly sites:**
  - LBNL, Berkeley
  - INFN, Torino
  - LNF, Frascati
  - STFC, Daresbury
  - Nikhef, Amsterdam

ITS construction: installation and commissioning time line



ITS construction: installation and commissioning time line



L. Musa, 12th ALICE ITS upgrade, MFT and O2 Asian Workshop

Summary

- ALICE ITS upgrade is ongoing for LHC high-luminosity program in Run3 and Run4
- The new ITS consists of 7 layers of MAPS technology based CMOS sensor:
  - Improved resolution
  - High read-out rate
  - Low material budget and radiation hard
- One of the first of its kind in high-energy physics experiment.
- Mass chip test, HIC and stave assemblies are going on at different assembly sites in full swing.
- Korea ITS group (Inha University, Pusan Nat'l University, Yonsei University) participated in mass chip test and HIC assembly.
- Commissioning and installation will start in LS2 period (2019-2020).

Thank You !!

Backup slides

Pixel chip requirements

	Requirement	Requirement
Spatial resolution	≈ 5 μm	≈ 5 μm
Integration time	< 30 μs	< 10 μs (global shutter)
Fake-hit rate	< 10^{-6} /pixel/event	< 10^{-6} /pixel/event
Detection efficiency	> 99%	>>99%
Power consumption	< 100 mW/cm^2	< 40 mW/cm^2
Radiation hardness*	> 2.7 Mrad (IB), 100 krad (OB) (TID) > 1.7×10^{13} 1MeV neq (NIEL)	**tested to 1 Mrad (TID) > 1.7×10^{13} 1MeV neq (NIEL)

* including safety factor of 10
** tests ongoing (slow irradiation needed to avoid rate-related effects)

ALICE ITS Upgrade: different stages