Velo Safety Interlock System

EP-DT-DI CONTRIBUTION

EP-DT
Detector Technologies

VELO Safety Interlock System

WP: Revision, not yet published

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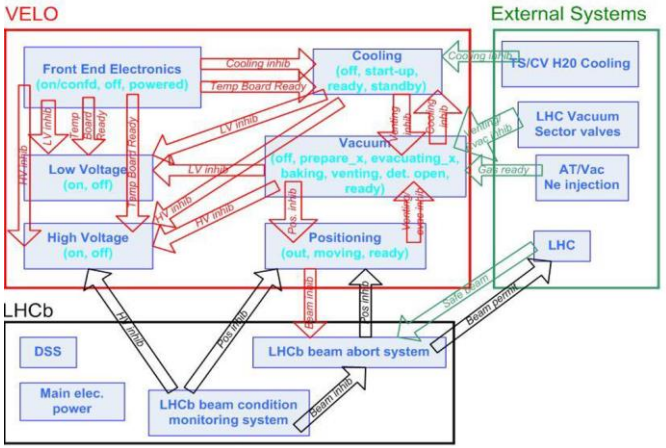
Due to high complexity of present Velo Interlock System and large number of critical interactions between the subsystems it has been decided to implement a central node for surveying and keeping the detector **always in a safe state** in case of unexpected events.

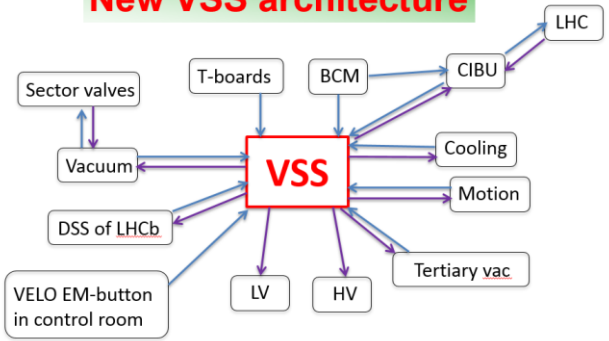
EP-DT-DI will upgrade the Safety Interlock Logic of the detector VSS to new system based on experience on similar equipments e.g. the Magnet Safety System (MSS) or Roman Pot Position Control System

Old VELO safety system (3)

All sub-systems and their mutual dependencies



New VSS architecture



VELO Safety Interlock System

The proposed solution is based on National Instruments Compact RIO FPGA Technology. The same used by DT-DI in the Magnet Safety Systems (MSS) in the LHC experimental magnets.

A dedicated rack will be produced by DT-DI including all the connections of all subsystems involved in the interlock logic.

Due to the large number of I/O's, specifically temperature sensors (up to 100) the Compact RIO will be expanded with 3 slave modules communicating with EtherCAT network.

The safety logic will be performed by the backplane FPGA while the Real Time Controller performs the communication to the LHCb VELO DCS users.

The cost of this upgrade has been evaluated up to 50 kCHF

VSS Rack