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CERN R&D lines for the mechanics of future tracking detectors

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Recent innovations in the field of silicon imaging technology for consumer applications open an extraordinary opportunities for new detector concepts, and hence offer strongly improved physics scope. ALICE has presented and expression of interest for the construction of a novel vertex detector, to be installed during LS3, consisting of truly cylindrical layers based on curved wafer-scale ultra-thin silicon sensors, featuring an unprecedented low material budget of 0.05 % X0 per layer.
In standard CMOS manufacturing, the maximum size of a chip is limited to the reticle area defined by the field of view of the photolithographic process, which is typically a few centimeters in both directions. For this reason, at present small sensors are mounted edge to-edge on top of a flexible PCB module that provides the power distribution and data bus.
However, a recent technology, called stitching, allows fabricating sensors of arbitrary dimensions, the only limit being the size of the wafer. The key new idea is to make use of the stitching technology to replace such a module with a single large sensor, where power distribution is managed internally, confining to the sensor edge the interconnections to the outside world.
The large sensor will be thinned to values of about 20 µm to 40 µm, and its surface finished with plasma polishing to release mechanical stress. The possibility to bend and operate ultra-thin sensors to a curvature radius of about 20 mm seems very promising, opening the way to the construction of a silicon-only cylindrical layer. This opens the possibility of fabricating a pixel sensor with the dimension of an entire stave. The distribution of power and electrical signals could then be done entirely inside the silicon chip and the electrical substrate would terminate close to the chip edge, where the interconnections to the chip would be realized. Concerning the elimination of the material associated with the cooling circuit, the possibility of using a low-speed (< 2 ms 1) air flow to remove the heat produced by the ITS Inner Layers by convection, in combination with peripheral liquid cooling, is considered a viable option for sensors with a power density below 20mW/cm2.
In addition the concept of a large-area sensor extended to the construction of a large silicon pixel tracker would represent a real breakthrough. ALICE has also developed plans for LS4 for a compact, next-generation multi-purpose detector, where the vertex detector is integrated with a number of tracker layers on larger radius, all equipped with MAPS pixel sensors. For such a detector the large areas of the outer layers, the costs, the assembly and the QA will drive the mechanics design choices. A “lego”modular concept, based on a modular substrate, to serve one or a limited number of chip (stitched) sensors, will allow for single module test and replacement, while it will pose the design challenge in the module’s electrical and hydraulic interconnections. Alternatively, the research of technologies that can be scaled to large areas without joints shall be investigated. Ideally a continuous structural/electrical/cooling substrate with a flexible shape, interconnecting thin MAPS shall provide a cheap fully integrated solution. Cheap and disposable substrate such as carbon fibre structures embedding polyimide pipes will be exploited. At the same time the material investigation shall be extended to carbon composites that can be processed with cheaper processes for large detector volumes, especially relevant respect to the new detector dimensions; i.e. out of autoclave curing that represent a promising faster and more cost-efficient process.

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