Introduction to 3D Digital SiPM and Latest Results for Particle Physics

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2019 CAP Congress – Simon Fraser University (Burnaby, BC)

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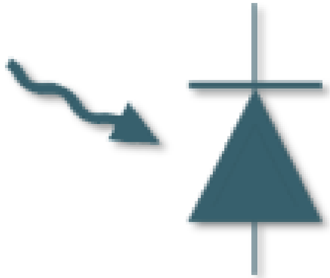
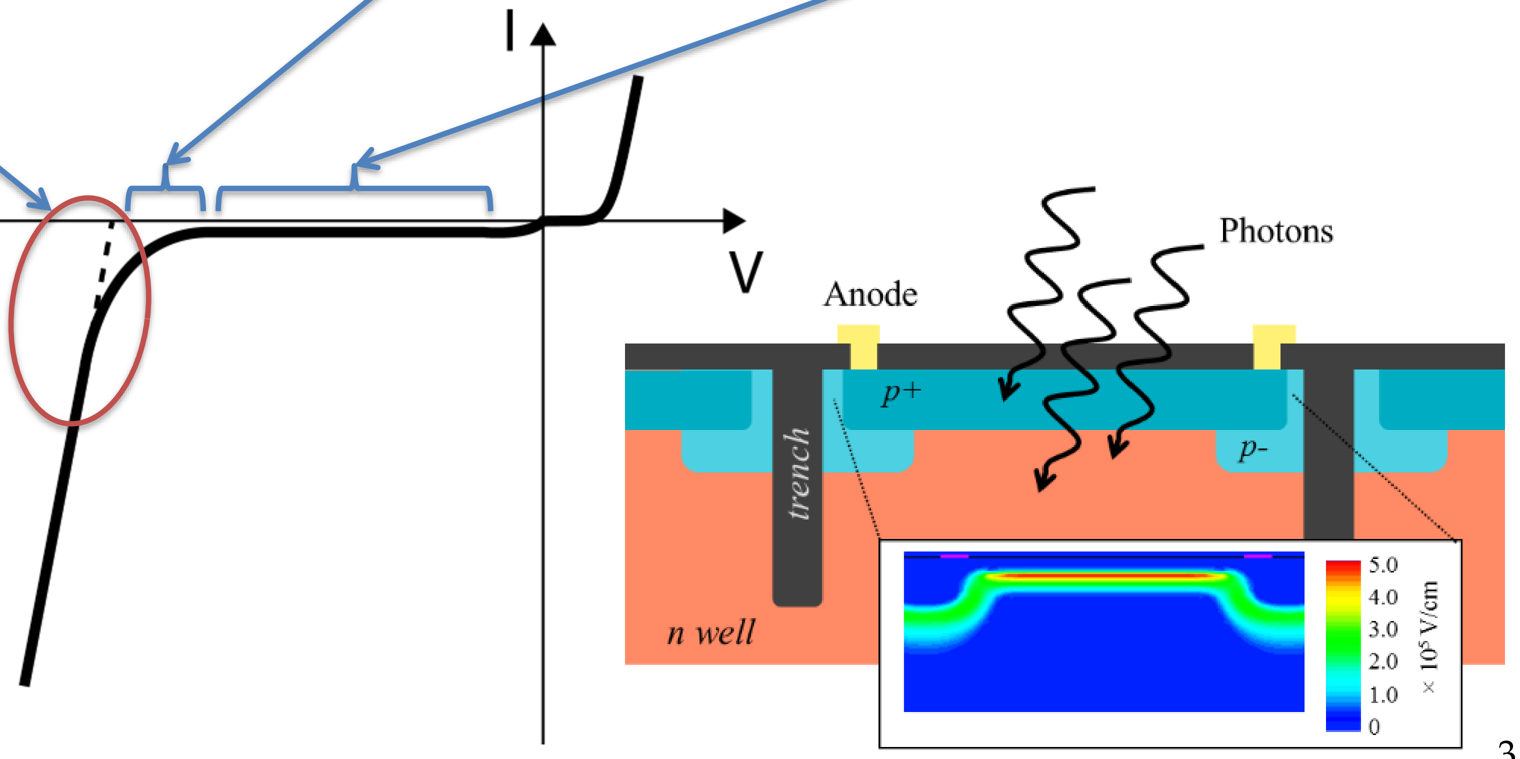
GRAMS

What is a Single Photon Avalanche Diodes (SPAD)?

Diode I-V Curve and Operating Regime

SPAD (Geiger mode)	**Avalanche Photodiode**	**Photodiode**
Gain = 10^4-10^6	Gain = 10-1000	Gain = 1
$V_{bias} > V_{Breakdown}$	$V_{bias} < V_{Breakdown}$	$V_{bias} << V_{Breakdown}$
Metastable		

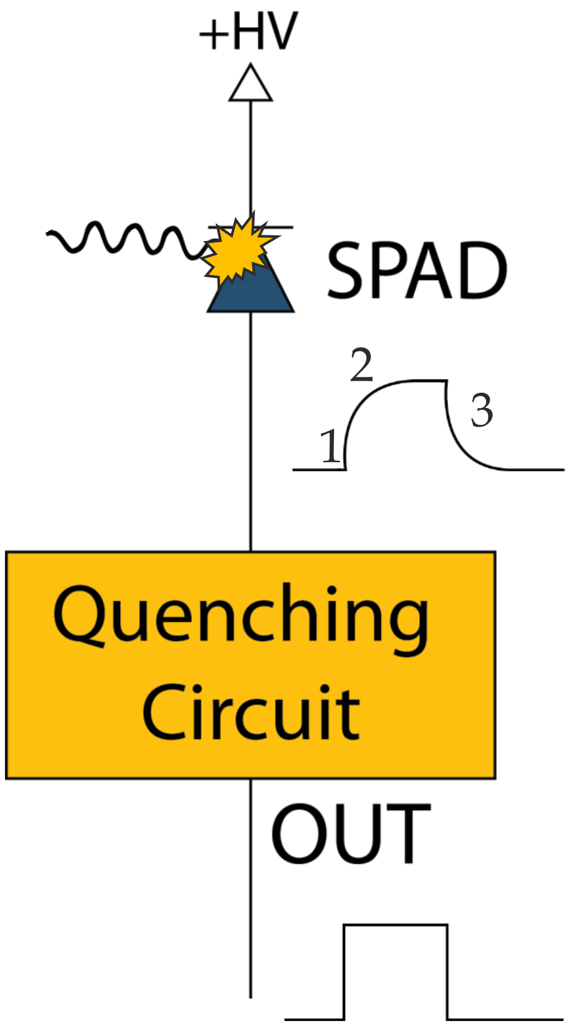


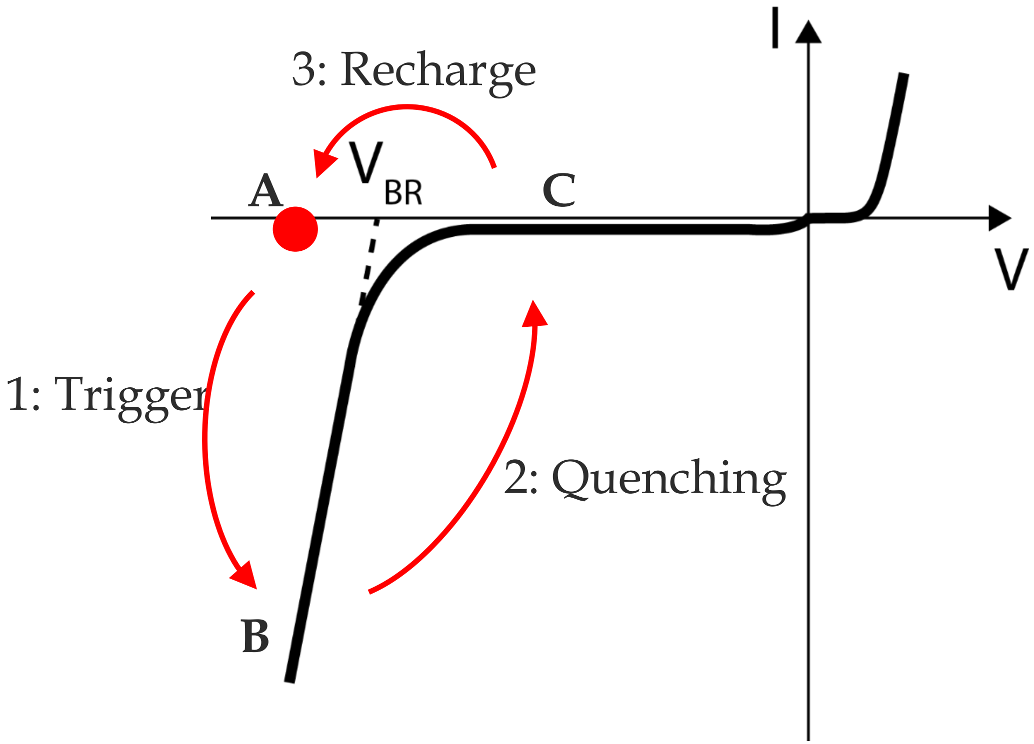


Non linear response

It's a binary detector!

Single Photon Avalanche Diode (SPAD) Operation Cycle





1. Excellent single photon timing resolution
2. Sensitivity – single photon counting
3. Silicon → mass production → low cost

Analog VS Digital Silicon Photomultiplier (SiPM)

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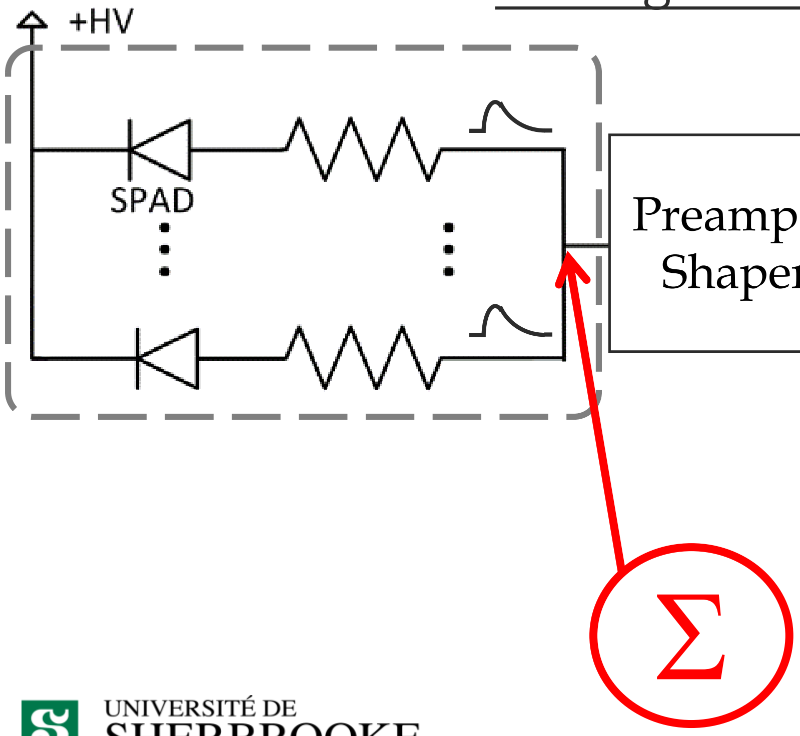
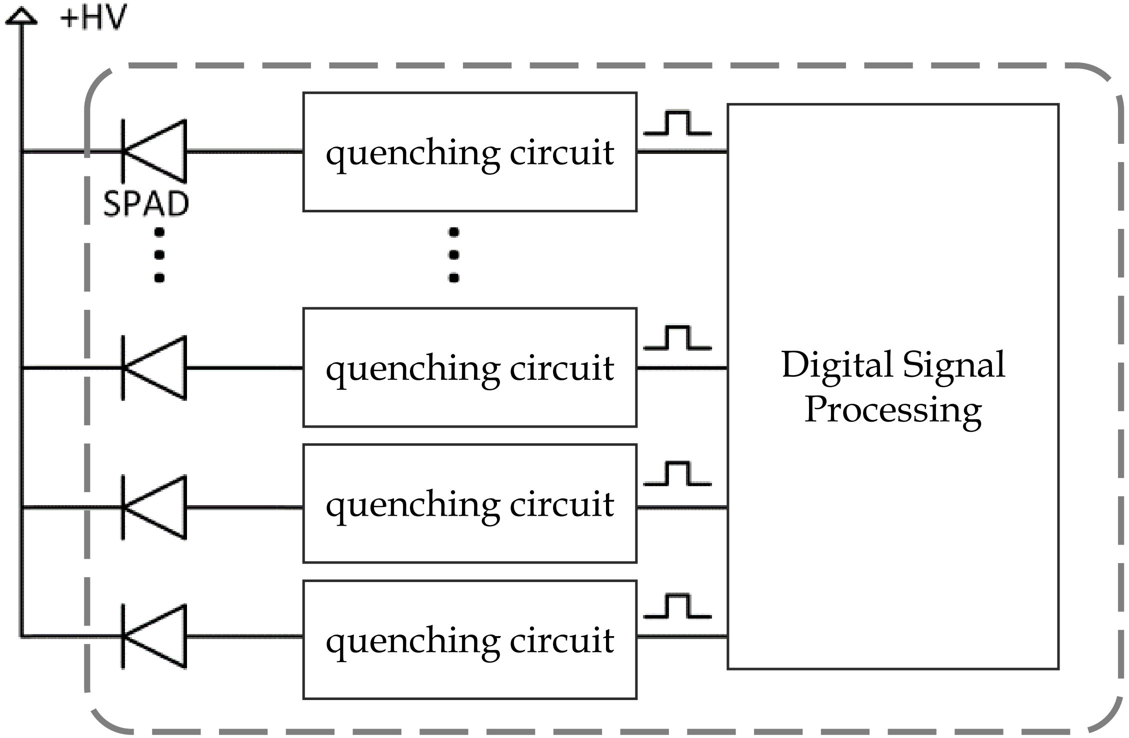
Analog and Digital Silicon PhotoMultiplier (SiPM): The Definition

Single photon avalanche diode (SPAD) is the basic unit cell of **analog and digital SiPM**


Analog SiPM


Digital SiPM

Analog and Digital SiPM

- A SPAD is a **Boolean detector:** **digital information available at the sensor level**

- With an **analog SiPM we sum binary detectors (an array of SPAD) to get a** **linear response**…
  - Then, use a current/transimpedance amplifier + shaper + ADC

To digitize the data… again!

- With a **digital SiPM, each SPAD is coupled one-to-one** with its individual readout circuit.
  - **Photon to bit conversion** at the sensor level
  - Improved noise immunity
  - Output capacitance is not an issue (compared to SiPM)
  - Single photon counting mitigated
  - Control over each SPAD: faulty or radiation damaged = shut off
  - Lower dead time (sense-quench-recharge < 10 ns)
  - Mitigates afterpulsing noise
  - No trigger = Low power consumption

3D Digital SiPM VS 2D Digital SiPM

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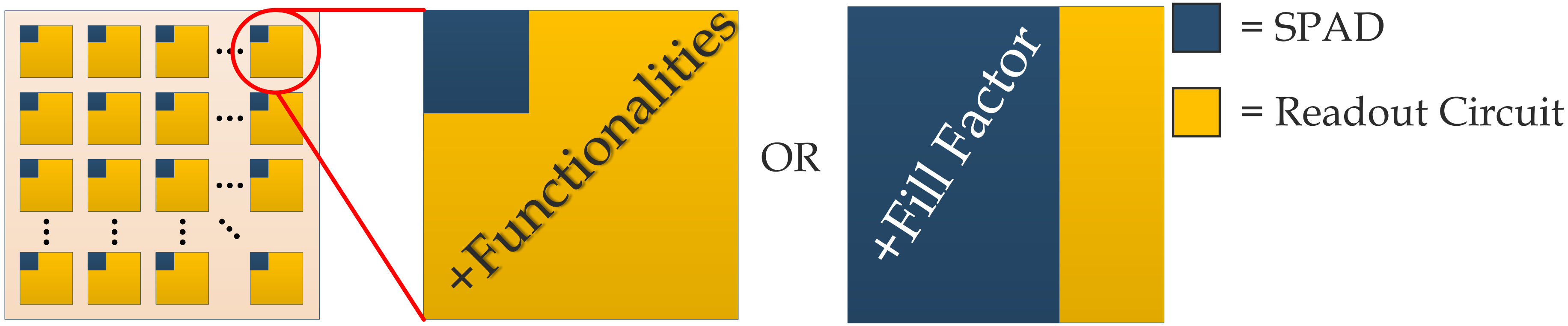
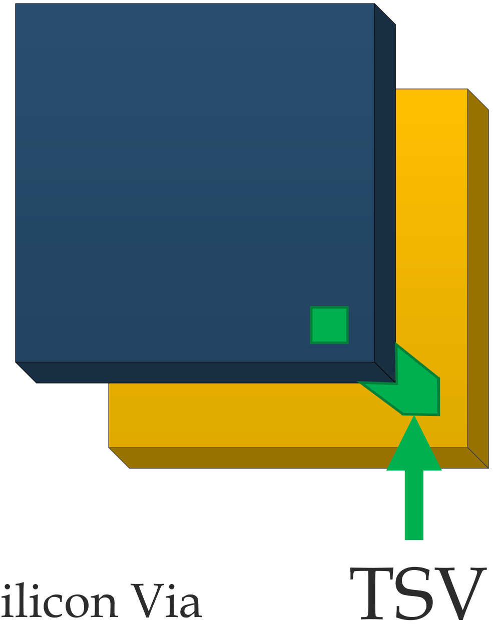
2D Digital SiPM: Trade off and Solution → 3D Digital SiPM



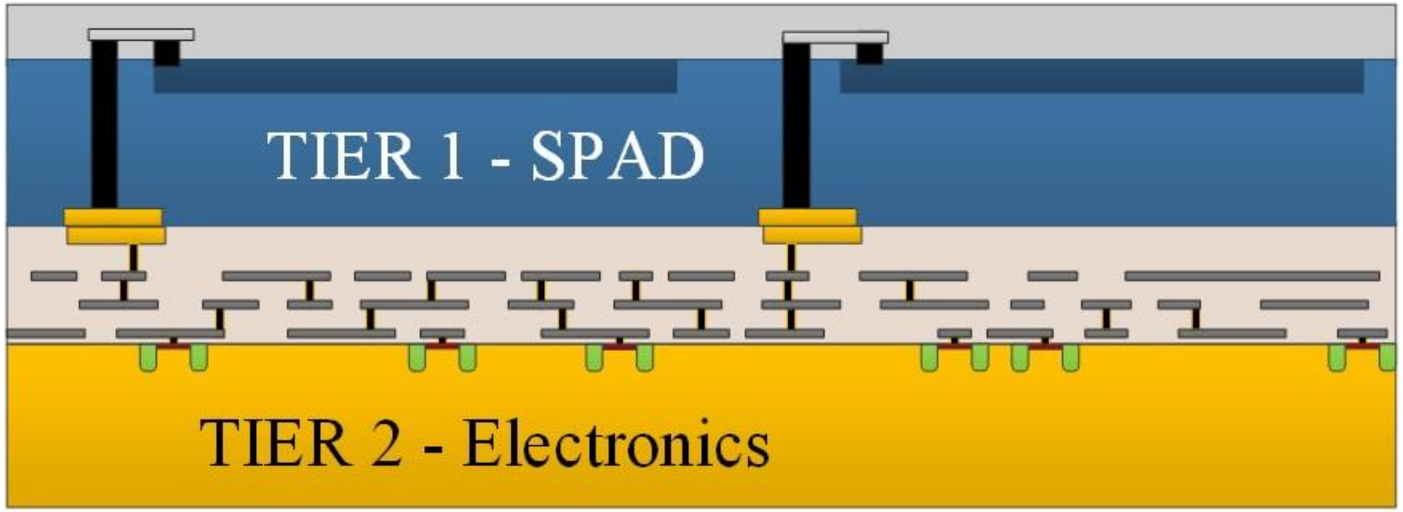
IDEALLY:



- High fill factor for improved photosensitive area
- Freedom for in-pixel electronics functionalities
- Heterogeneous technologies
  - SPAD in optimal technology
    with
  - CMOS readout circuits in optimal process for application specific functionalities

TSV = Through Silicon Via

3D Digital SiPM



3D Digital SiPM (3DdSiPM) for Low Power and Large Area Detectors

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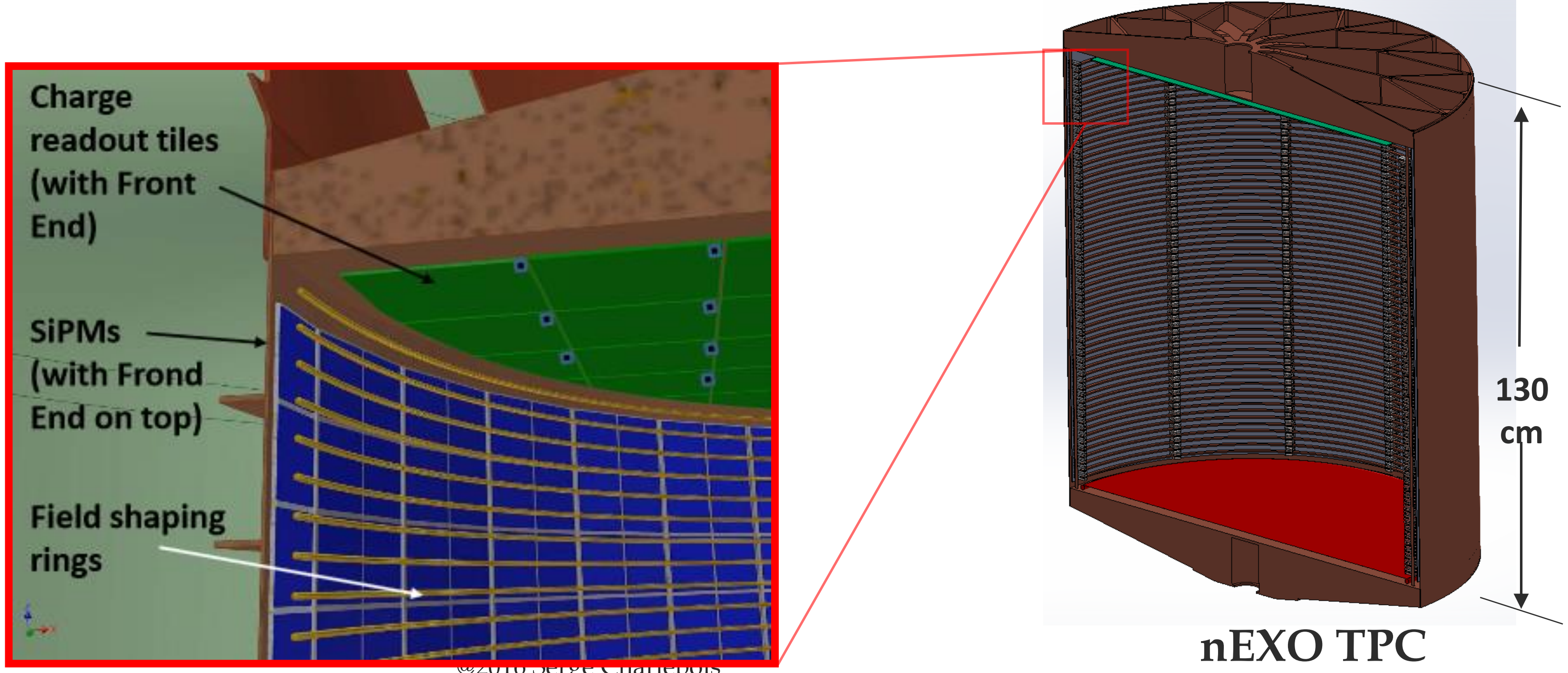
nEXO – Search for 0νββ - Baseline Design

- 5T liquid Xenon, enriched ^{136}Xe
- Charge TPC and scintillation readout

- Analog SiPM on silicon interposer
  - Photosensitive surface: 4 - 5 m^2
  - ~1x1 cm^2 SiPM in tiles ~10x10 cm^2
  - Power budget for scintillation readout: 50 W (100 W with data transmission)



nEXO TPC

Source: nEXO collaboration

Liquid Argon Detector with Pulse Shape Discrimination

CFI Innovation Fund 2017

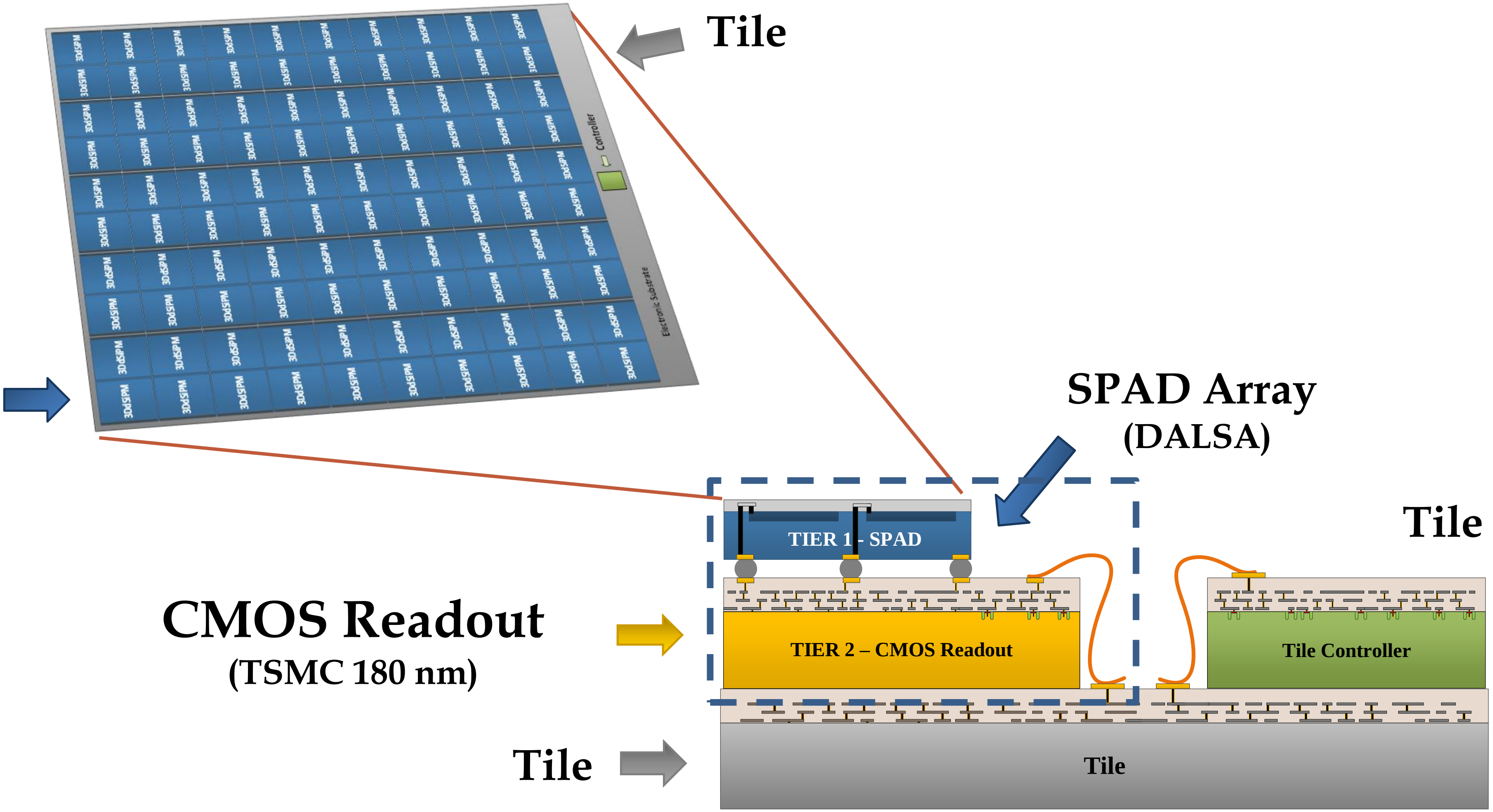
Title: Facility for Development of Cryogenic Detectors and Readout Systems for Subatomic Physics and Particle Astrophysics

Principal investigator: Mark Boulay (Carleton)

Université de Sherbrooke contributions:

- 3D digital SiPM with Embedded Digital Signal Processing for Pulse Shape Discrimination in LAr
- Low Power 3D Digital SiPM for nEXO

The Goal: Tile of 3DdSiPM with a Controller



Tile

3D digital SiPM

SPAD Array
(DALSA)

Tile Controller

CMOS Readout
(TSMC 180 nm)

Tile

Development of the 3DdSiPM Technology:

The SPAD Array and the 3D Vertical Integration Process

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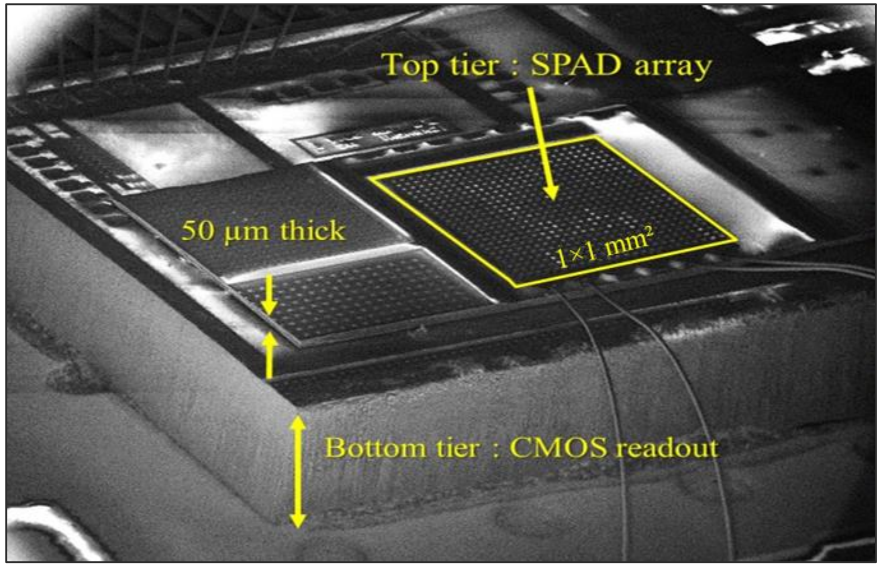
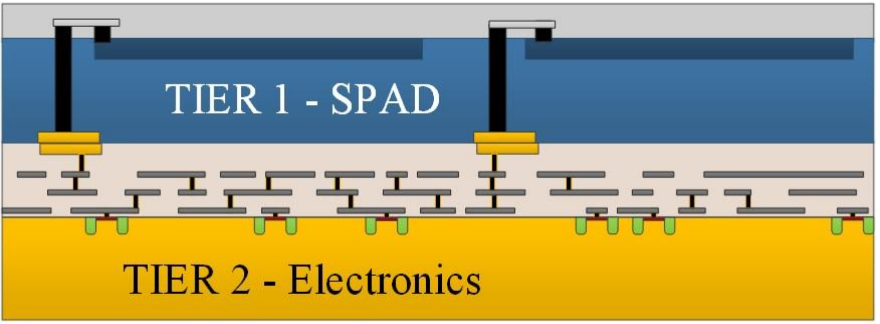
How to Build a Fully Industrial 3D Digital SiPM ?

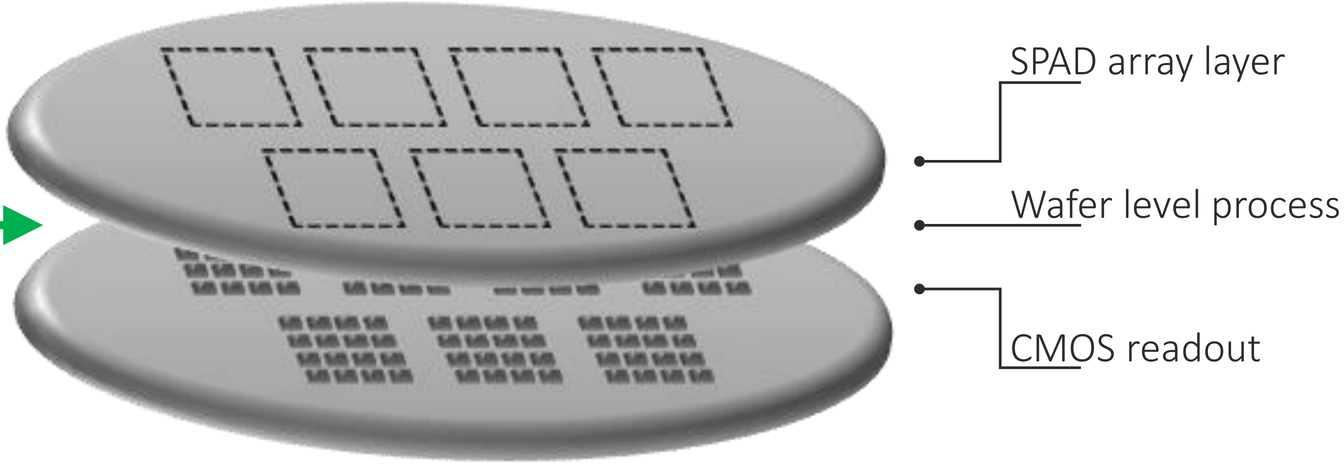
2016: First 3D digital SiPM prototype





Wafer scale / industrial process

3D digital SiPM technology



Main Industrial Collaborator : Teledyne DALSA

High-end CCD process line

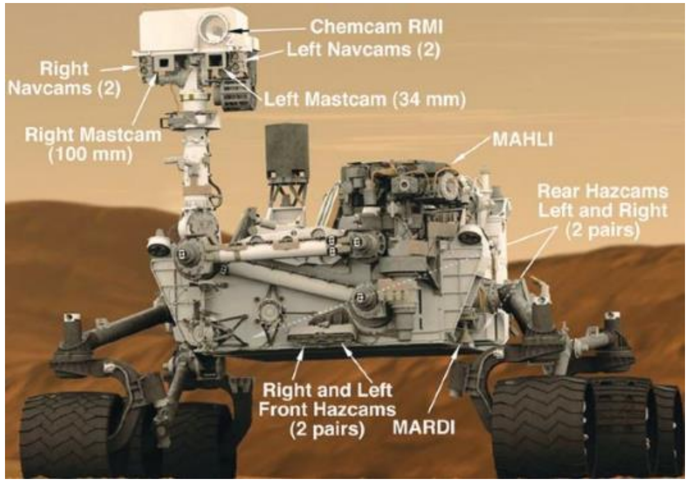
--> excellent for SPAD R&D

- 150 mm process line
- low contaminant / gold free clean rooms

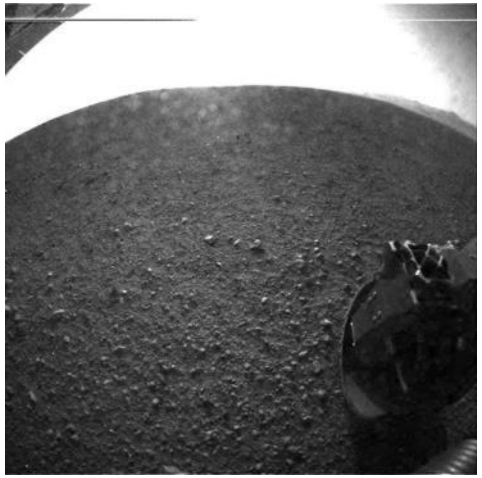
World top 5 Microelectromechanical systems (MEMS) Foundry

--> excellent for wafer level integration

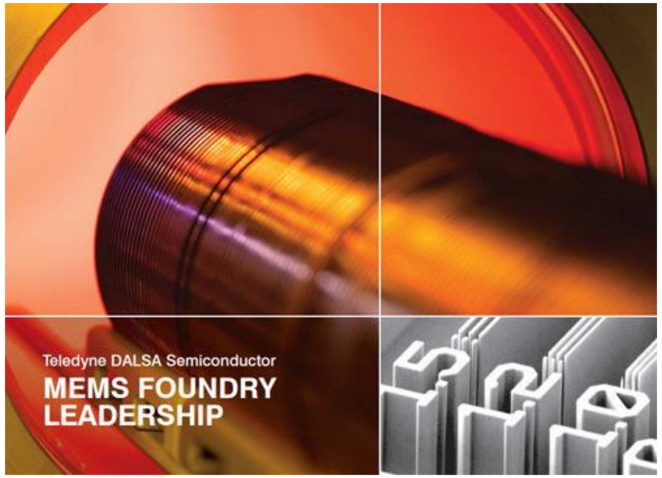
- 150 mm and 200 mm process line
- Wafer thinning, deep etching, bonding, ...



The Eyes of the Mars Curiosity Rover. Tech Briefs (2012)



Life on Mars: Rover landing gives boost to Canadian tech sector. The Globe and Mail (2012)



Courtesy of Teledyne DALSA

MEMS Foundry Rankings (2017 sales in US$M)	
STMicroelectronics	174
Teledyne DALSA	60
Silex Microsystems	50
TSMC	47
X-Fab	42

Status of the MEMS Industry 2018 Market and technology Report Yole Development (2018)

TELEDYNE DALSA
Everywhereyoulook™

Teledyne DALSA Semiconductor Inc. (est. 1980)

~ 500 employees located at Bromont near Montreal, Canada

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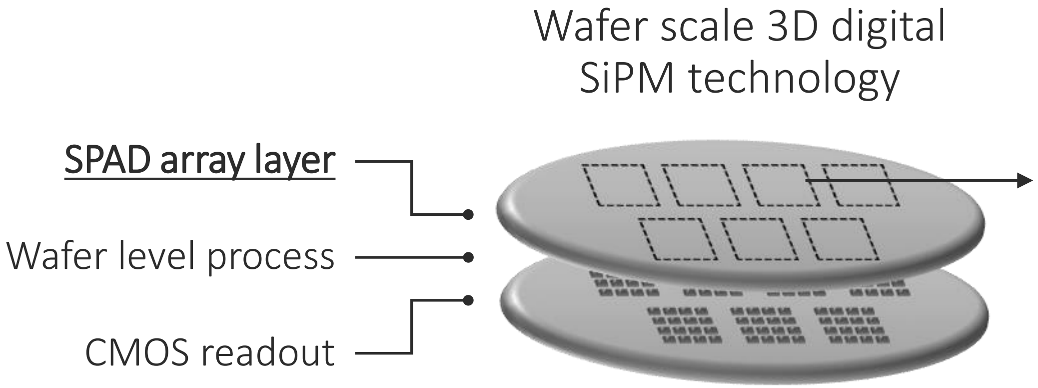
3D digital SiPM technology : SPAD array layer

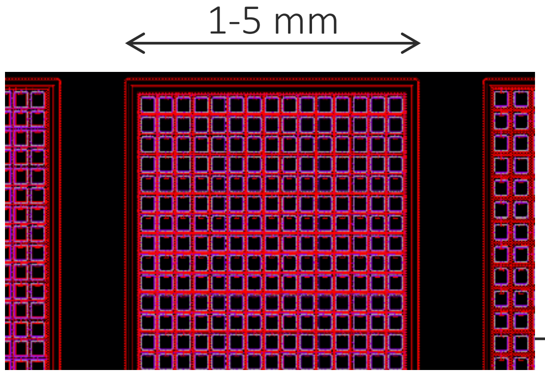
- Top tier : 150 mm wafer (custom process using DALSA CCD production line)
- 1x1 to 5x5 mm^2 SPAD array
- 50-100 um diameter front-side illuminated shallow P+N type SPAD (~0.4 um depth)
- 4 um width / 22 um depth optical/electrical isolation trench (highly doped polysilicon filling)
- 2D process for SPAD development

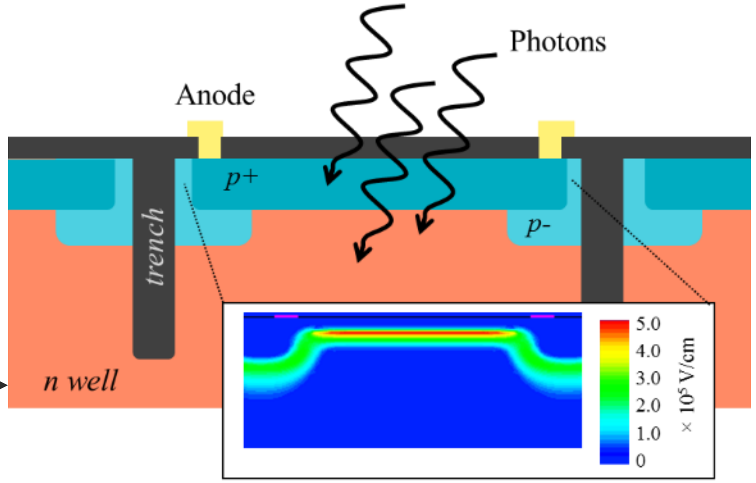

Wafer scale 3D digital SiPM technology

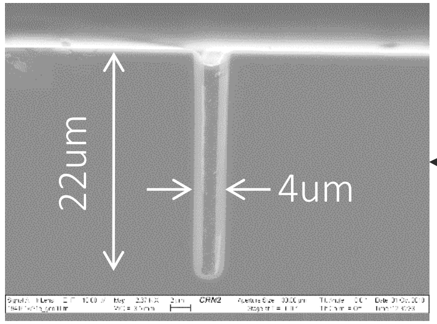
SPAD array layer

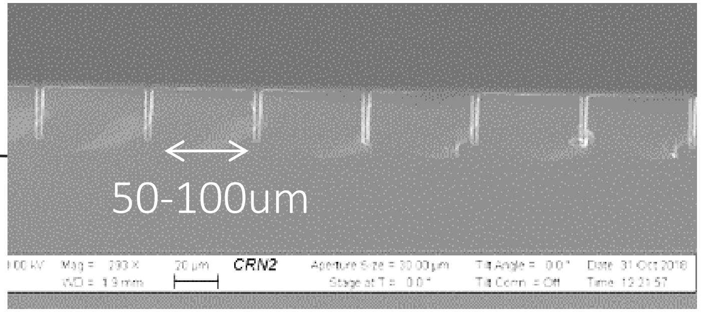
Wafer level process

CMOS readout

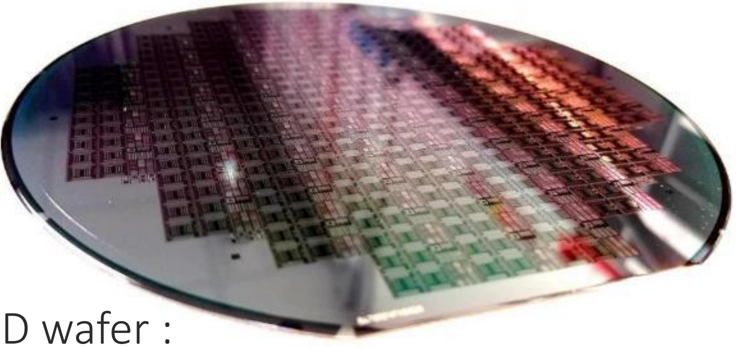






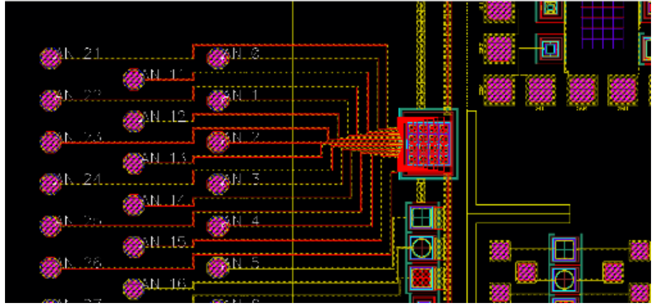


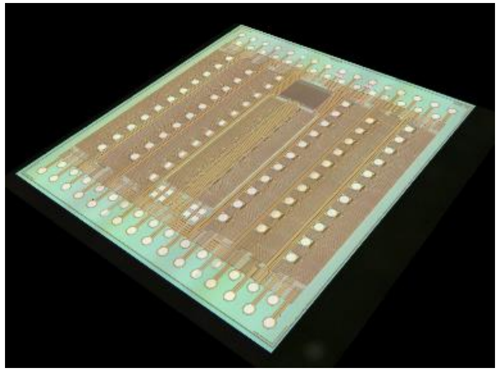
SPAD development plateform



2D SPAD wafer :

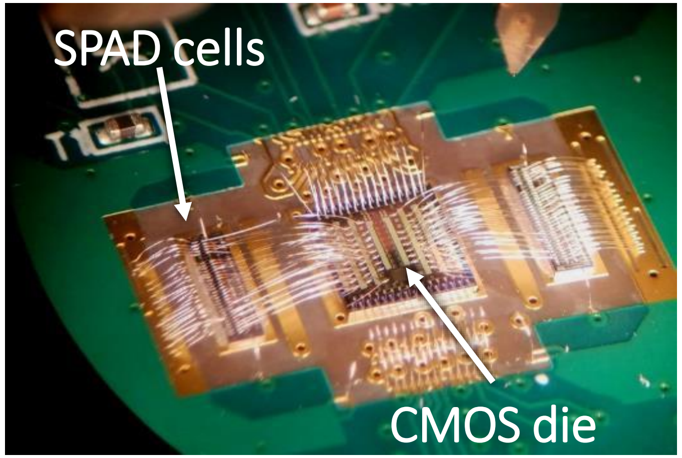
- Single cell with variants
  - SPAD size and shape
  - process variation
- Small array (4 x 4 cells)
  - cell size and pitch
  - w/ or w/out trench



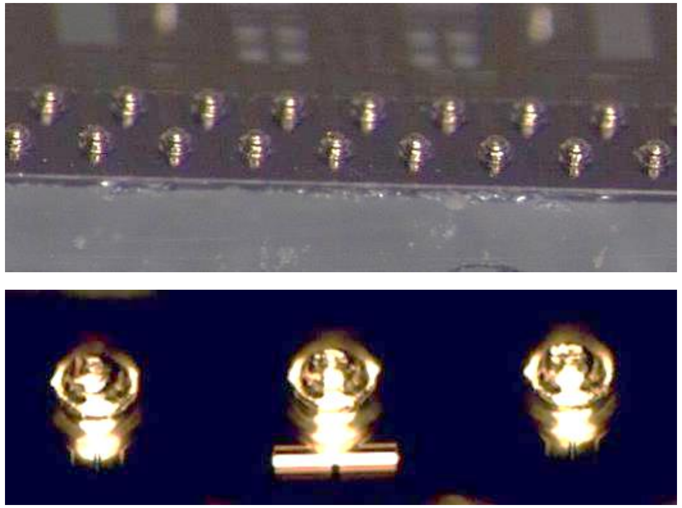


CMOS ASIC for SPAD probing

- TSMC CMOS 180 nm
- 64 quenching circuits
  - anode/cathode
  - up to 10 V excess voltage
  - variable input threshold
  - variable holdoff
- 4 outputs (MUX)



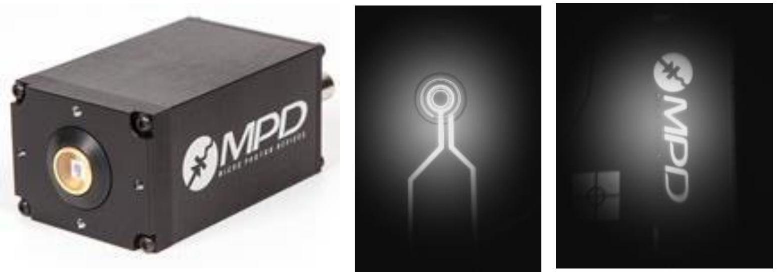
side-by-side wirebonding



flipchip packaging

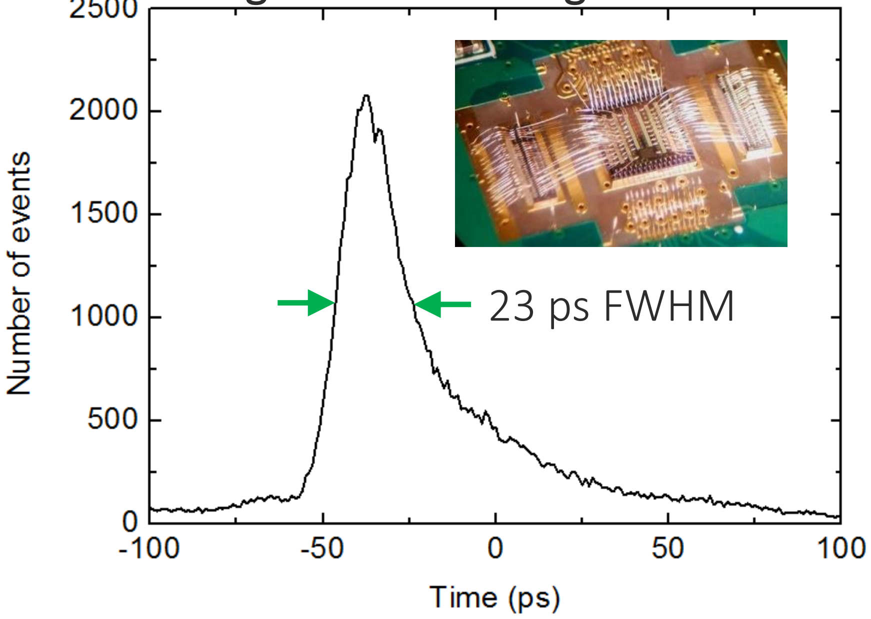
2D SPAD First Batch : Measurement Results

	2D SPAD	MPD PD5CT
Size (um)	36 um (square)	50 um (circle)
Breakdown / Overvoltage (V)	22.1 / 4	28.7 / 5
Dead time	100 ns - 10 us	300 ns
Single Photon Timing Resolution (ps FWHM)	23 @ 410 nm	27 @ 820 nm
Photon Detection Efficiency (%)	52% peak at 500 nm >30% at 390-600 nm	47% peak at 550 nm >30% at 450-700 nm



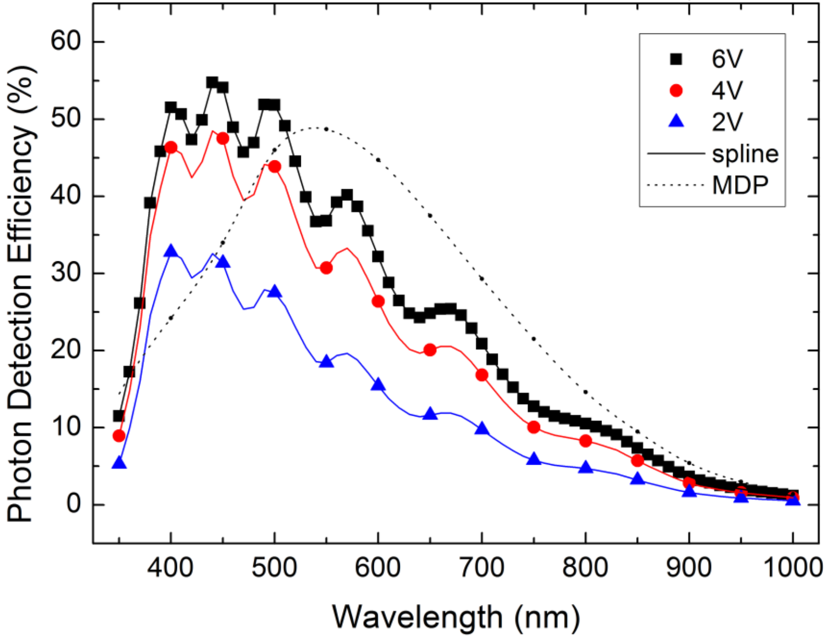
High-rate photon counting and picosecond timing with silicon-SPAD based compact detector modules A. Giudice (Journal of Modern Optics 2007)

Single Photon Timing Resolution



23 ps FWHM

Photon Detection Efficiency



400-500 nm range :

- fast scintillators for PET scanners

VUV range (< 200nm):

- liquid Xe : 178 nm
- liquid Ar : 128 nm

VUV postprocessing for noble liquid experiments

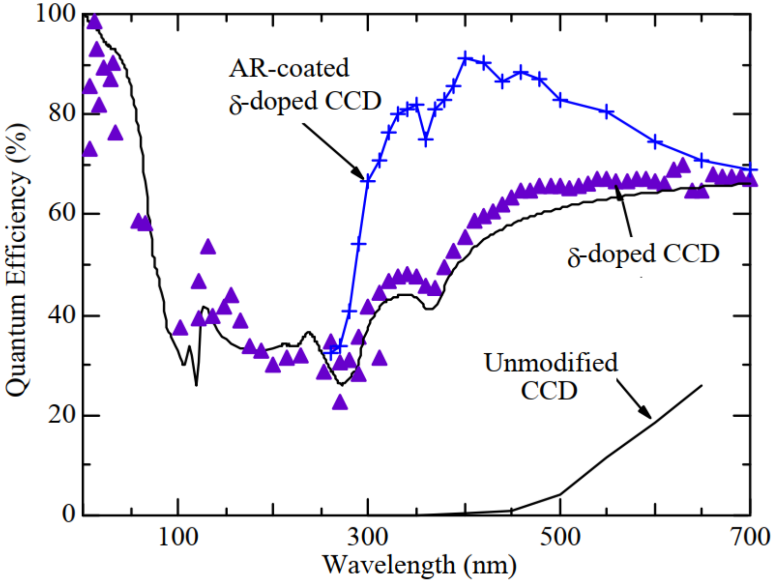
- Delta-doping is used on CCDs to enhance the deep UV response
- Surface energy band engineering (ultra thin surface doping)
- UV-generated electrons drift towards the SPAD junction
- Simulation on SPAD demonstrates quantum efficiency improvement
- Will be use in addition to anti-reflective coating

Goals:

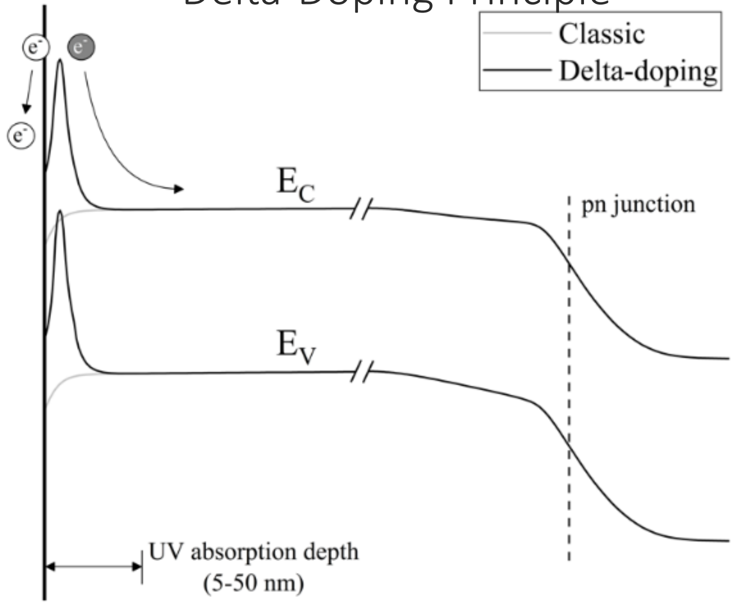
> 35% PDE at 175 nm (LXe)

> 15% PDE at 125 nm (LAr)

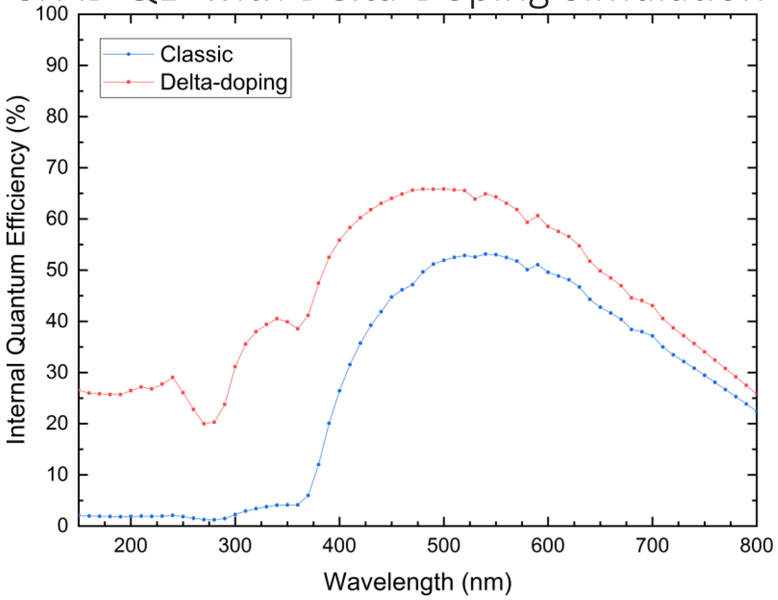
CCD Quantum Efficiency



Delta-Doping Principle



SPAD QE with Delta-Doping Simulation



Delta-doped back-illuminated CMOS imaging arrays: progress and prospects.
M.E. Hoenk (In Infrared Systems and Photoelectronic Technology IV 2009)

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Arthur B. McDonald
Canadian Astroparticle Physics Research Institute

Development of the 3DdSiPM Technology:

Microelectronic Readout Integrated Circuit for Low Power 3DdSiPM and Large Area Detectors

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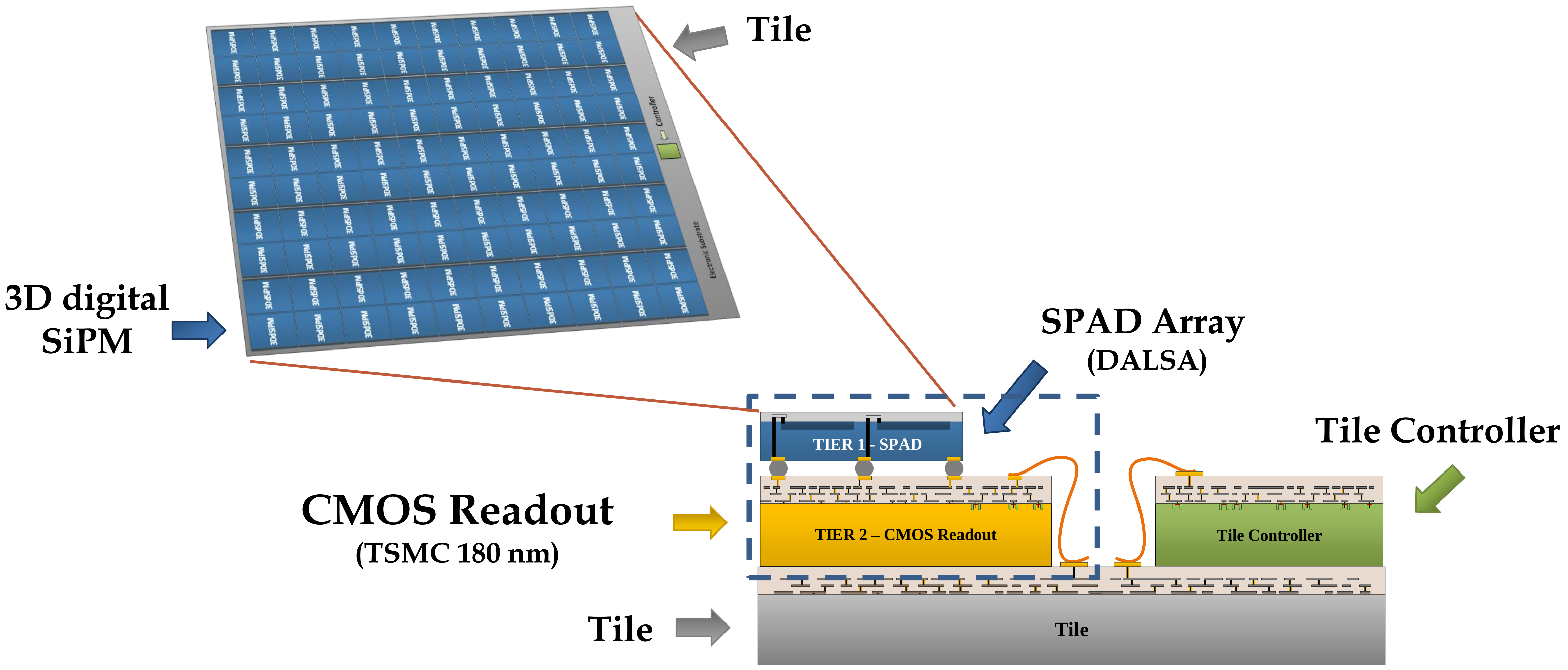
3DdSiPM on a Tile with a Controller



Tile

3D digital SiPM

SPAD Array
(DALSA)

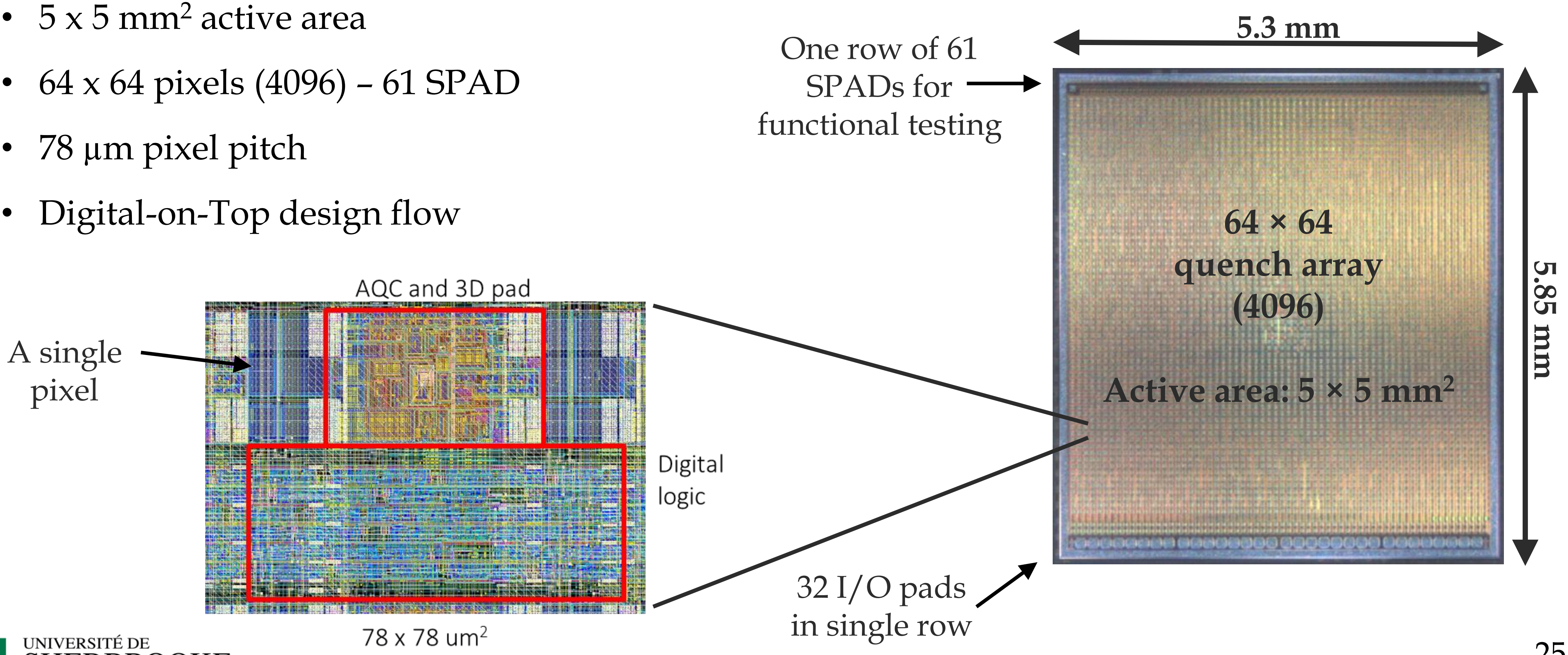
Tile Controller

CMOS Readout
(TSMC 180 nm)

Tile

CMOS Readout for 3DdSiPM – Overview

- TSMC 180 nm BCD process
- 5 x 5 mm^2 active area
- 64 x 64 pixels (4096) – 61 SPAD
- 78 µm pixel pitch
- Digital-on-Top design flow



5.3 mm

One row of 61 SPADs for functional testing

64 × 64 quench array (4096)

Active area: 5 × 5 mm^2

5.85 mm

32 I/O pads in single row

A single pixel

AQC and 3D pad

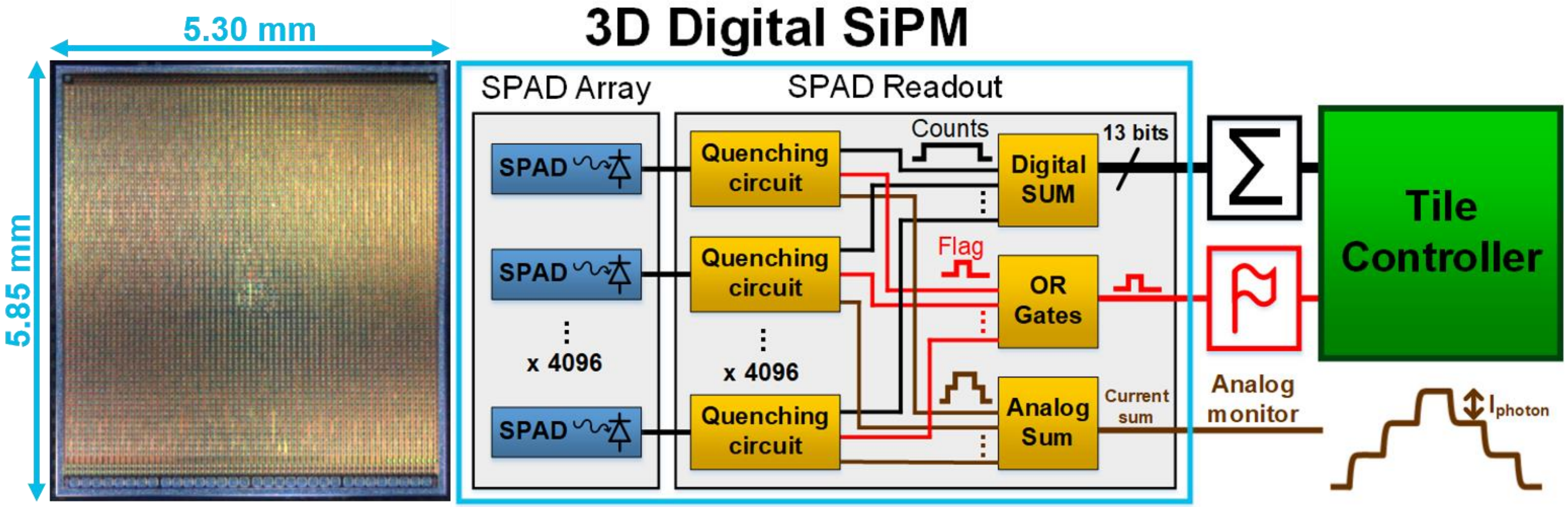
Digital logic

78 x 78 um^2

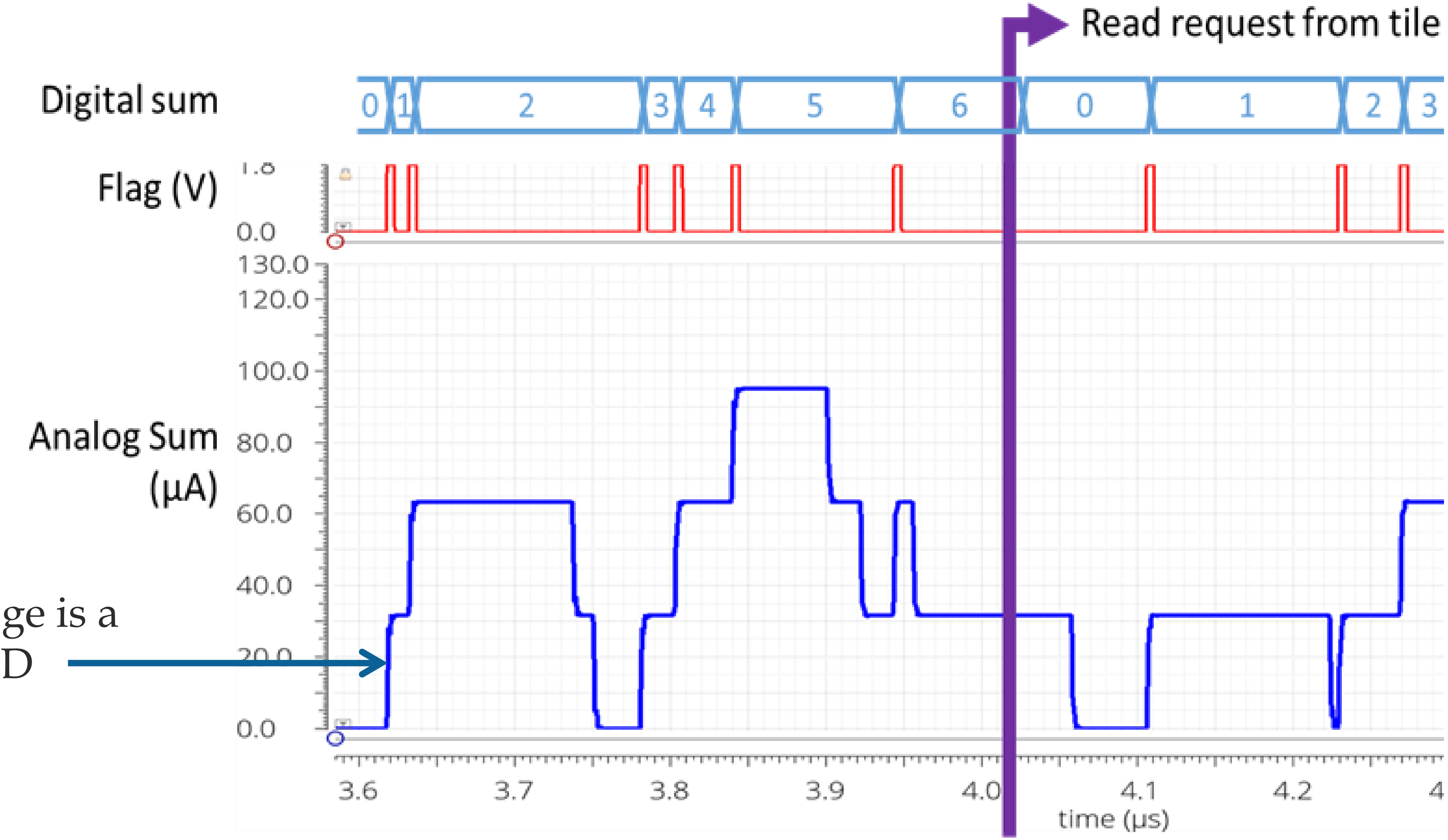
CMOS Readout for 3DdSiPM – Low Power Architecture

- nEXO operation mode: **INTEGRATION**
  - Event driven: each 3DdSiPM signals the tile controller when a SPAD triggers
  - **Asynchronous (no event no clock – low power)**
  - Integration time from 10 ns to 1 µs (350 ns)
  - Transmission of total counts (over integration time) when requested by the tile controller
  - Analog monitor for demonstration

- LAr operation mode: **CONTINUOUS SAMPLING**
  - Synchronous operation by a clock
  - Flags the controller to signal counts
  - Low flag jitter (<500 ps) to allow time-of-flight
  - 128 FIFO depth for transmission on request
  - Sampling bins: short (10 ns) and long frames (1 µs) to allow PSD (Pulse Shape Discrimination)



Simulation of the 3 Outputs from the ASIC



Each rising edge is a triggered SPAD

tommy.rossignol@usherbrooke.ca

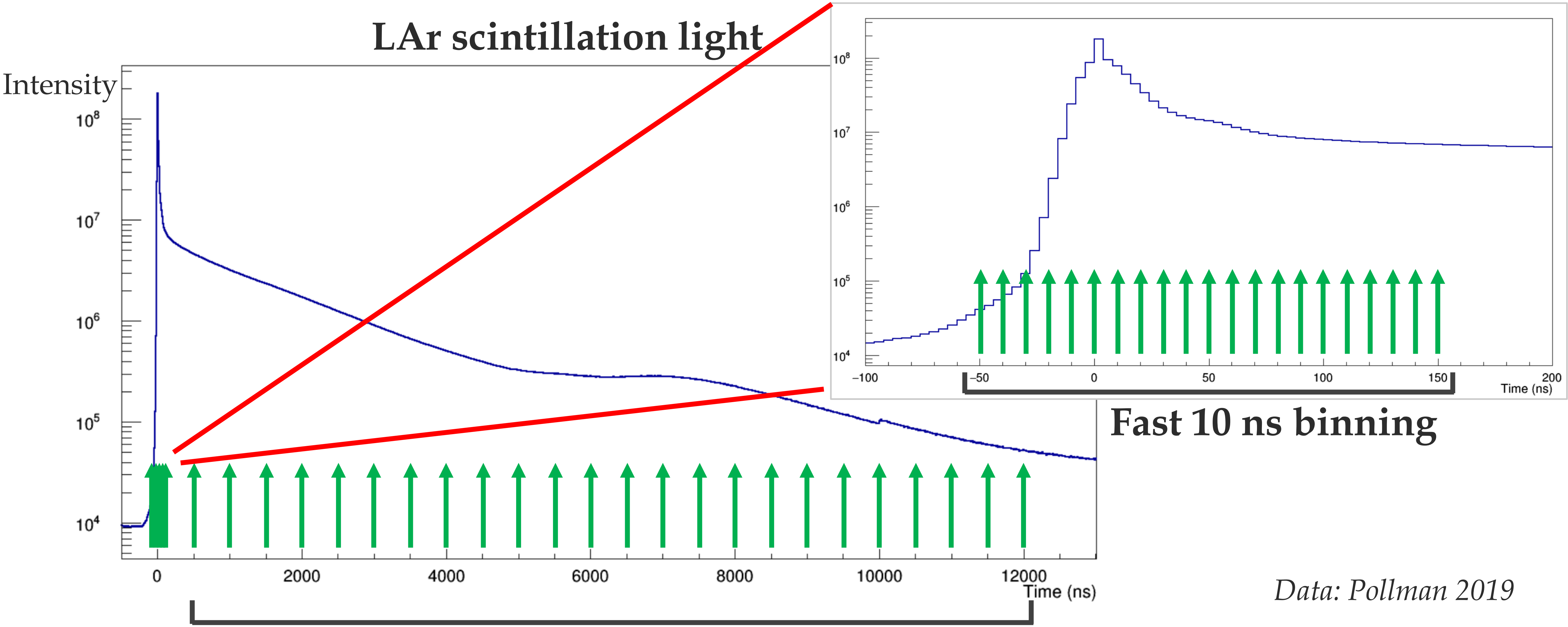
Coincidence / Dark Count Filter

- Single **flag** on a tile in a **coincidence window** : **event rejected** (dark count)

- Multiple **flags** on a tile in a **coincidence window** : **start acquisition** and read out after **acquisition time**

- **Coincidence window duration**, **acquisition time** and **flag threshold** managed by tile controller (programable)
- Possibility to keep all **flags** (threshold of zero)
- No readout on dark count to limit power consumption

Time Binning for Pulse Shape Discrimination in LAr



LAr scintillation light

Fast 10 ns binning

Slow 500 ns binning

Data: Pollman 2019

Microelectronic Readout Integrated Circuit for Low Power 3DdSiPM and Large Area Detectors

Measurements and Results

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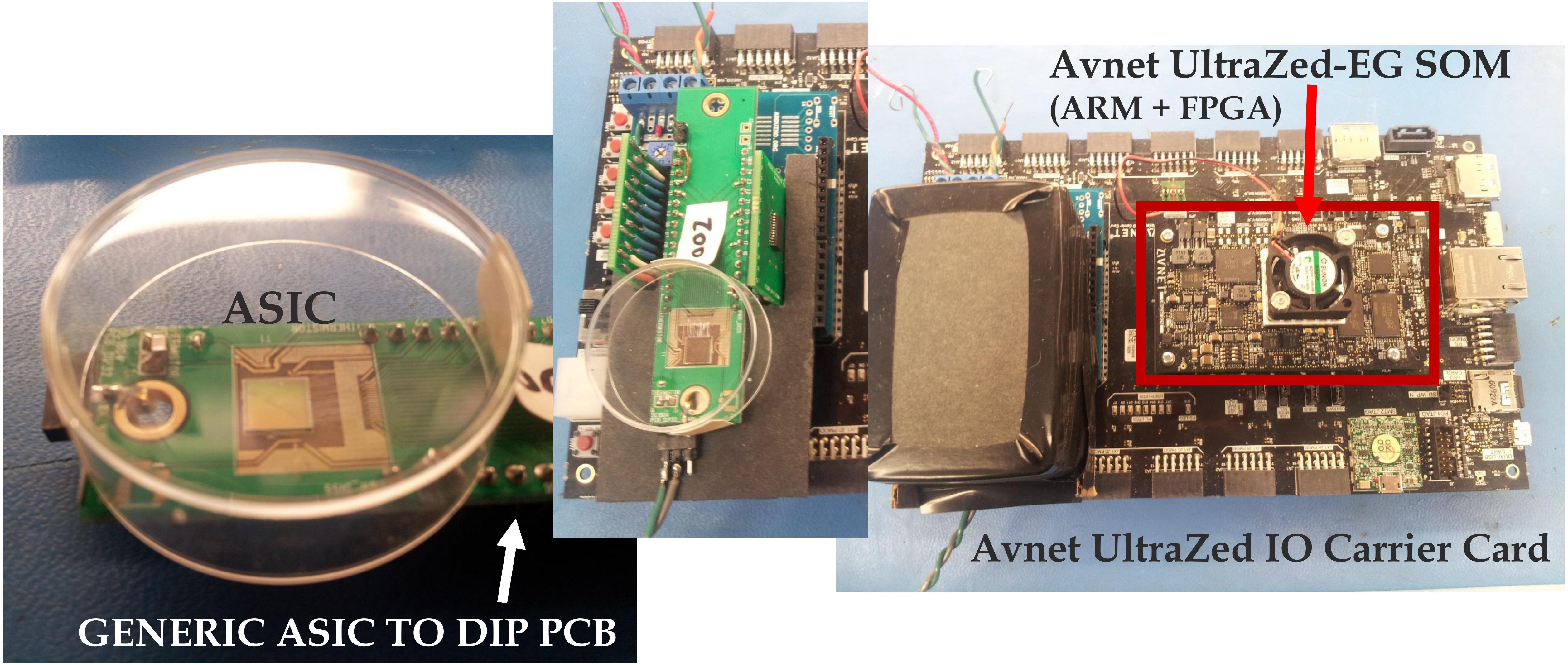
« Apollo 13 » Setup – Functionnality Tests



ASIC

GENERIC ASIC TO DIP PCB

Avnet UltraZed-EG SOM
(ARM + FPGA)

Avnet UltraZed IO Carrier Card

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« Apollo 13 » Setup – Functionnality Tests

- Poor PCB signal integrity : new PCB this week!
- 61 SPAD on the ASIC
- 90 % of the digital functionalities **tested** and **validated**
    - Flag, digital sum, FIFO, data transmission, ASIC configuration

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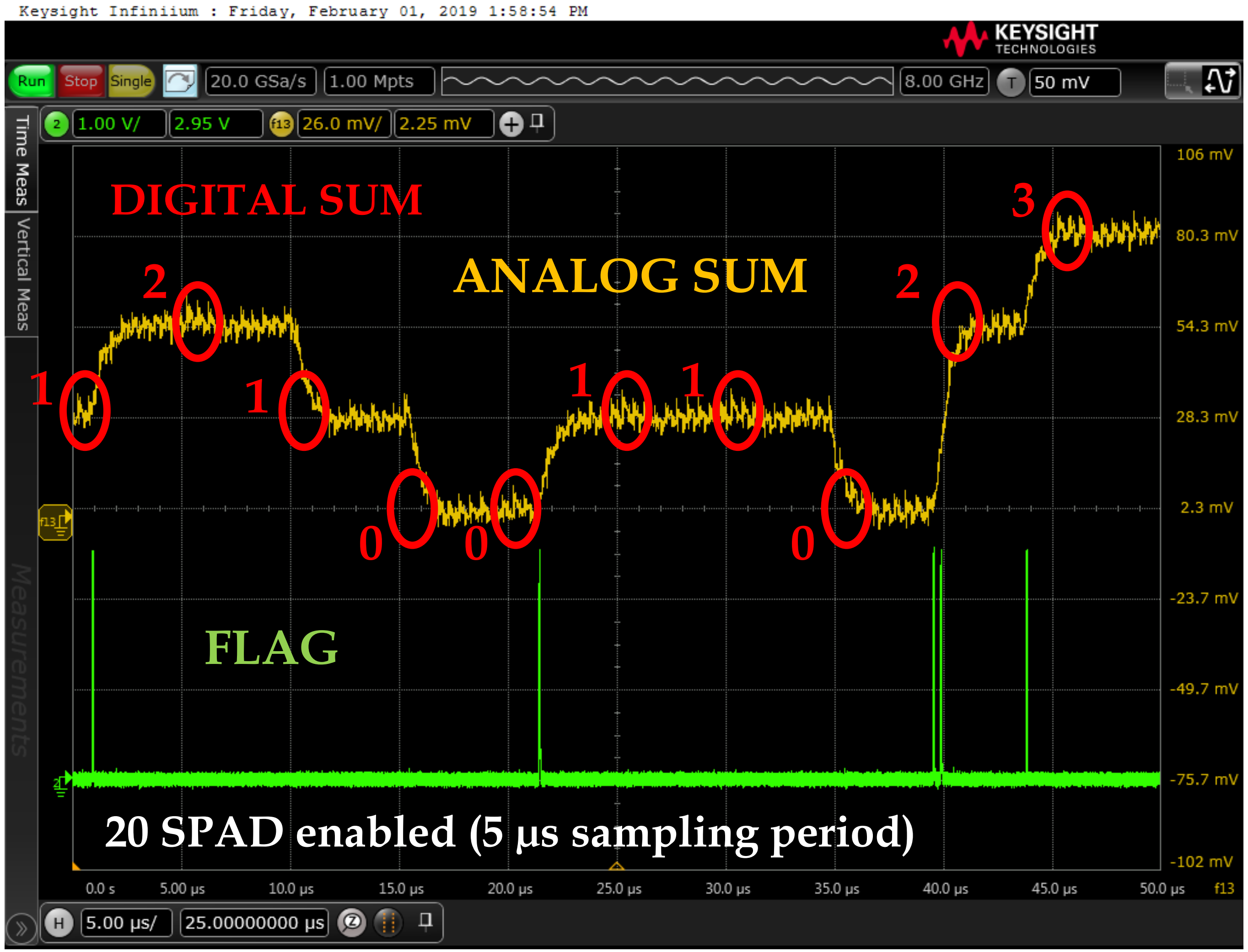
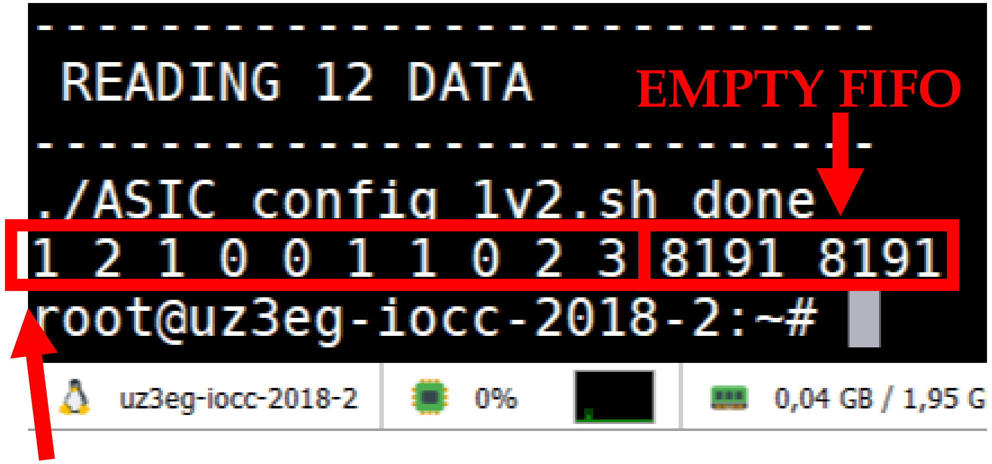
MEASURED - Integration Mode



20 SPAD enabled (5 µs sampling period)

- ADC like acquisition
- Number of pixels triggered (in hold off) at the moment of the acquisition
- Each circle represents the result from the digital register



```
------------------------------
 READING 12 DATA
------------------------------
./ASIC_config_1v2.sh done
1 2 1 0 0 1 1 0 2 3 8191 8191
root@uz3eg-iocc-2018-2:~#
```

EMPTY FIFO

DIGITAL SUM FROM ASIC

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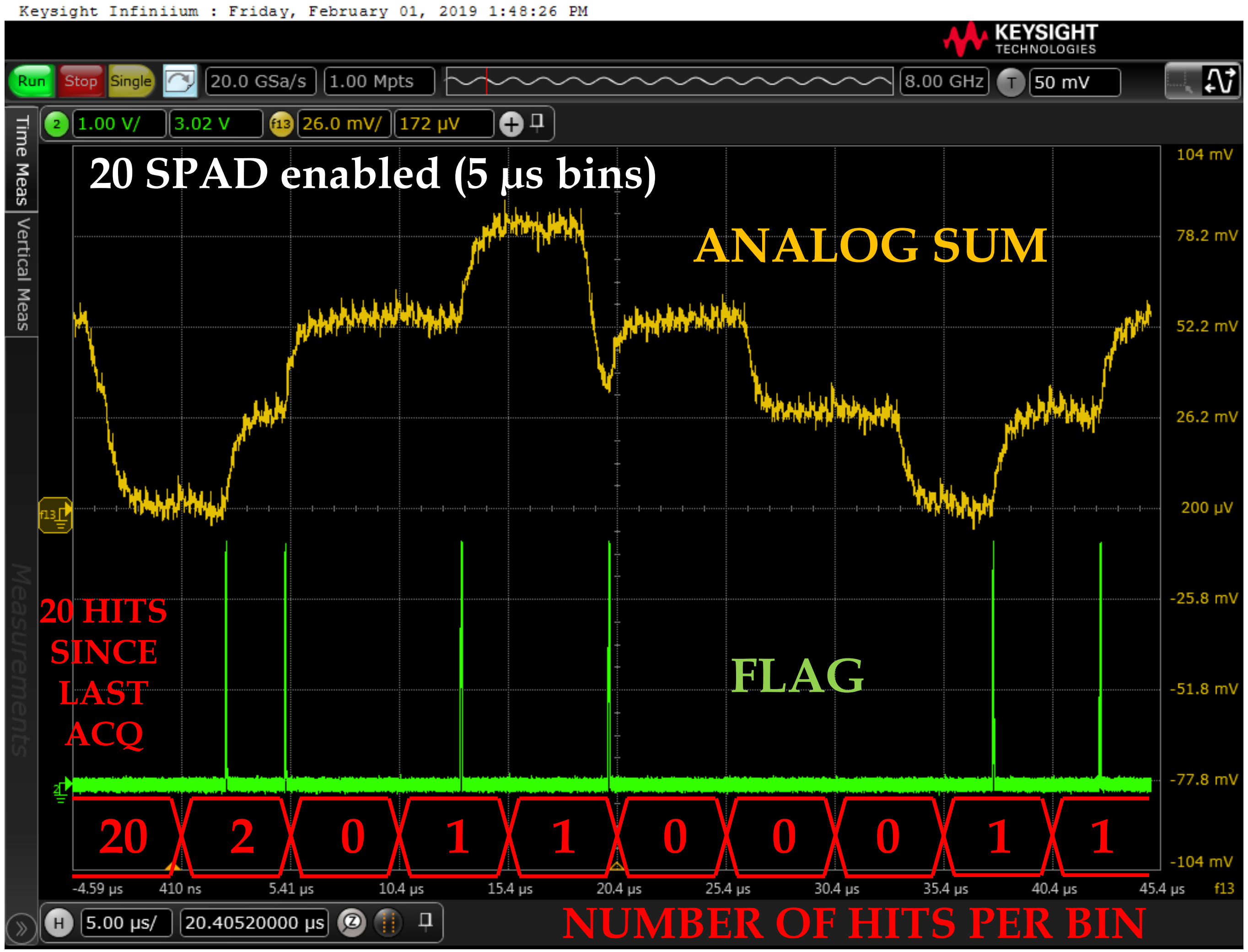
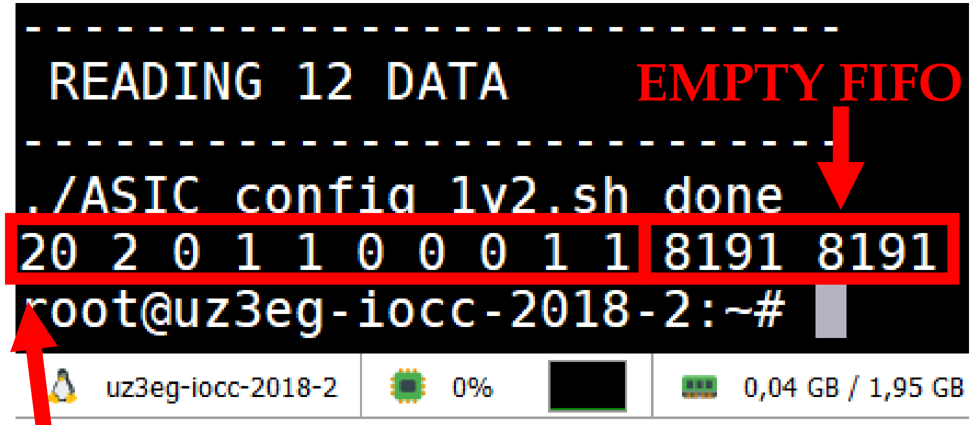
MEASURED – Binning Mode



- Time binning acquisition
- Number of pixels triggered in each time bin
- Each number represents the result from the digital register



```
-----------------------------
 READING 12 DATA
-----------------------------
./ASIC config 1v2.sh done
20 2 0 1 1 0 0 0 1 1 8191 8191
root@uz3eg-iocc-2018-2:~#
```

DIGITAL SUM FROM ASIC

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Conclusion

- No fundamental limitation to build 3D digital SiPM, but it is a great engineering challenge.
- First 3D Digital SiPM expected in 2020.
- SPAD array, 3D integration and readout electronics developed and optimized in parallel.
  - Microelectronics readout soon ready for wafer level production.
  - SPAD R&D as fast as we can within Teledyne-DALSA.
  - Issue with 3D bonding: bad luck. Problem is now fixed.
- We are recruiting! Ph.D. and postdoc.
- In parallel with particle physics instrumentation, electronic readout for:
  - Positron Emission Tomography (PET) aiming at sub-10 ps FWHM coincidence timing resolution.
  - Photon gating Computed Tomography (CT) scanner.
  - Quantum key distribution.

A team's work

Université de Sherbrooke

- **Serge Charlebois**
- **Réjean Fontaine**
- **Roger Lecomte**
- **Henri Dautet**
- Julien Sylvestre
- David Danovitch
- Caroline Paulin
- Étienne Paradis
- Étienne Grondin
- Konin Koua

- Nicolas Roy
- Frédéric Nolet
- Samuel Parent
- Audrey Corbeil Therrien
- Benoit-Louis Bérubé
- Marc-André Tétrault
- Frédéric Vachon
- Tommy Rossignol
- Gabriel St-Hilaire
- Jacob Deschamps
- Xavier Bernard
- Thomas Dequivre
- William Lemaire

- Luc Maurais
- Maxime Côté
- Vincent Philippe Rhéaume
- Étienne Desaulniers Lamy
- Alexandre Boisvert
- Michel Labrecque-Dias
- Pascal Gendron
- Arnaud Samson
- Jonathan Bouchard
- Frédérik Dubois
- Marc-Olivier Mercier
- Frédéric Bourque

Collaborators

- Fabrice Retiere
- Paul Lecoq
- nEXO Collaboration
- nEXO Canada
- Simon Viel

Teledyne-DALSA Semiconducteur Inc

- Claude Jean (CEO)
- Stephane Martel
- Robert Groulx

Arthur B. McDonald
Canadian Astroparticle Physics Research Institute

NSERC
CRSNG

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sur la nature
et les technologies
Québec

RESMIQ
Regroupement Stratégique
en Microsystèmes du Québec

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MICROSYSTEMS

3IT

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FUND

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