HMPID Trigger during Run3

HMPID Plenary Meeting 14/12/2018

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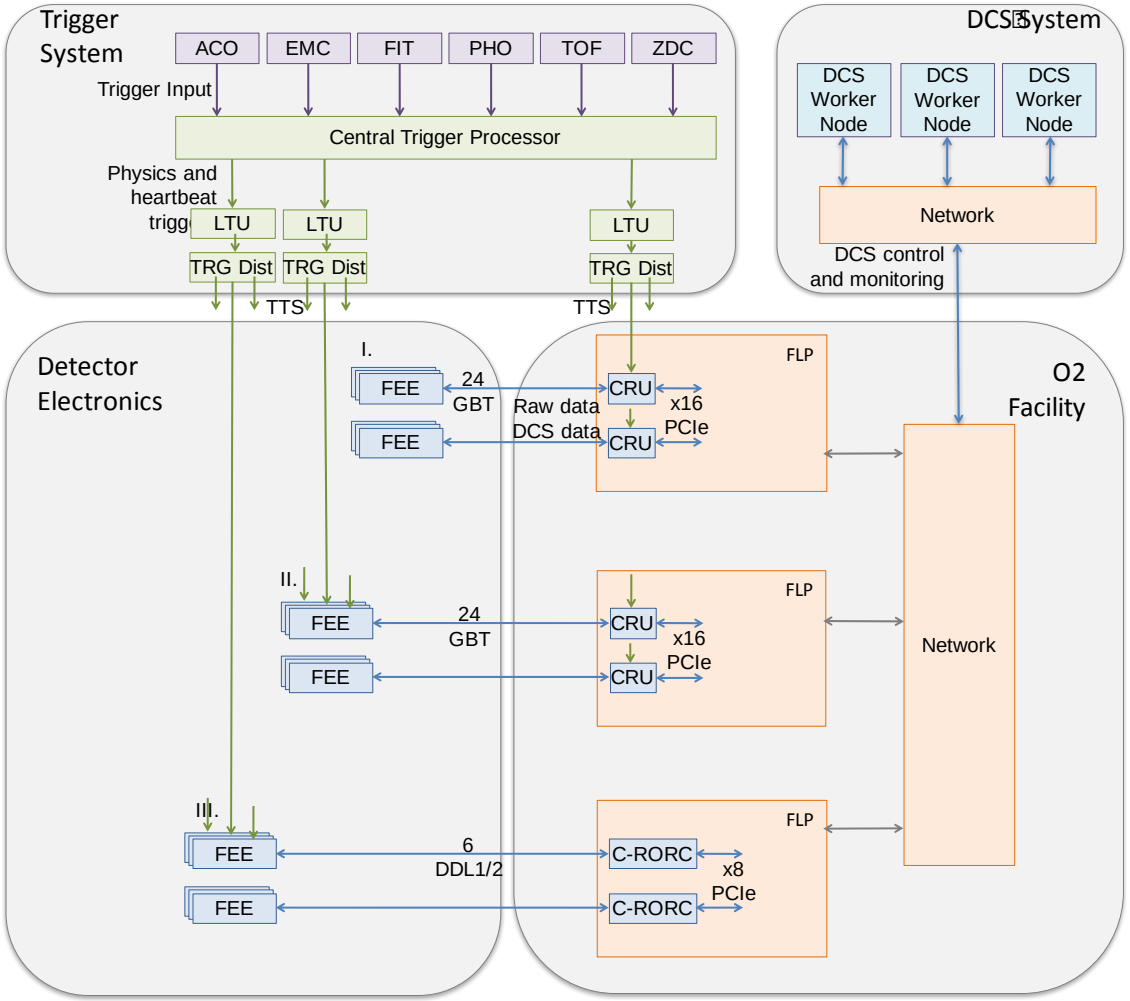
Triggering in Run3



- CTP will produce trigger signals
  - LM, L0, L1 with several latencies
- In addition CTP will produce the HB trigger and other software triggers.
- All trigger types are sent via LTU and TTS

HMPID in Run3

- **HMPID Requirements:**
  - L0 signal at ~1.2 us after an event when charge on the pads is at its peak
  - Message to be able to assemble header for data transfer
- Run3 triggering for detectors with TTC System
  - One synchronous trigger via channel A, sent at LM, L0 or L1 time
  - An asynchronous message in channel B, containing the trigger data sent from CTP at L1 time
- HMPID will also receive an LM trigger via LVDS cables

HMPID in Run3

- **Why LM?**
  - L0 signal arrives at CTP at 1200 us
  - It arrives at our detector (over TTC) at ~1.7 us, which would be too late for us
  - Solution is to use LM which arrives at the detector at ~835 ns

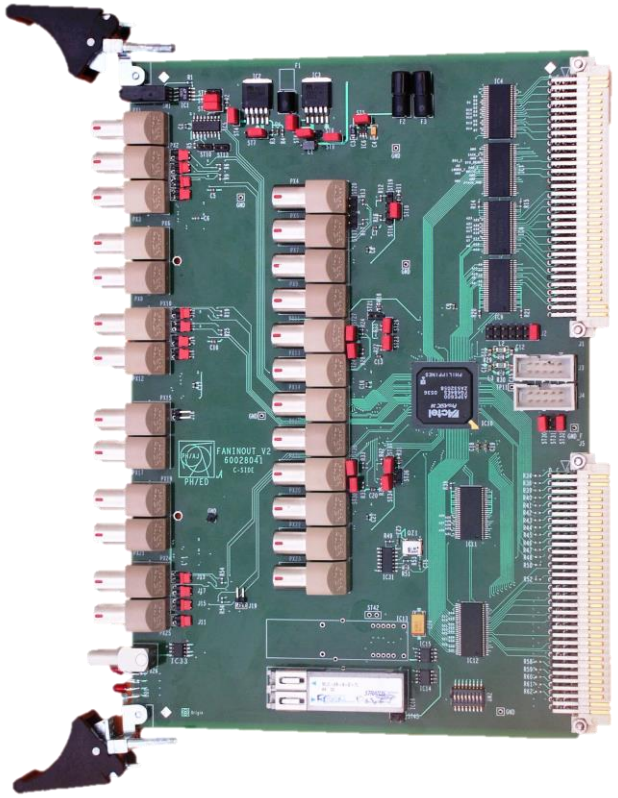
Time	Total Latency (ns)	Description
425 ns	425 ns	LM input to CTP board
100 ns	525 ns	CTP Processing Time
125 ns	650 ns	CTP-LTU Fan-Out Time
25 ns	675 ns	LTU Processing Time
160 ns	835 ns	Propagation Time from LTU to HMPID

Table: Calculating the propagation time of LM via LVDS

HMPID in Run3

- Upgrades to HMPID are twofold:
  1. New Fan-In/Fan-Out module for precise control on the delay, distribution of LM and fan-in of BUSY
  2. Upgrades of Firmware to handle trigger message

Fan-In/Fan-Out Module



- **Current Module:**
  - **Delay Range:** 2.5 us
  - **Delay Resolution:** 25 ns
- **Improved Module**
  - **Delay Range:** 525 ns
  - **Delay Resolution:** 1 ns

Design and Implementation

- Tapped Shift Register Based Architecture with a multiplexer.
- Implementation in Xilinx Virtex 5 FPGA

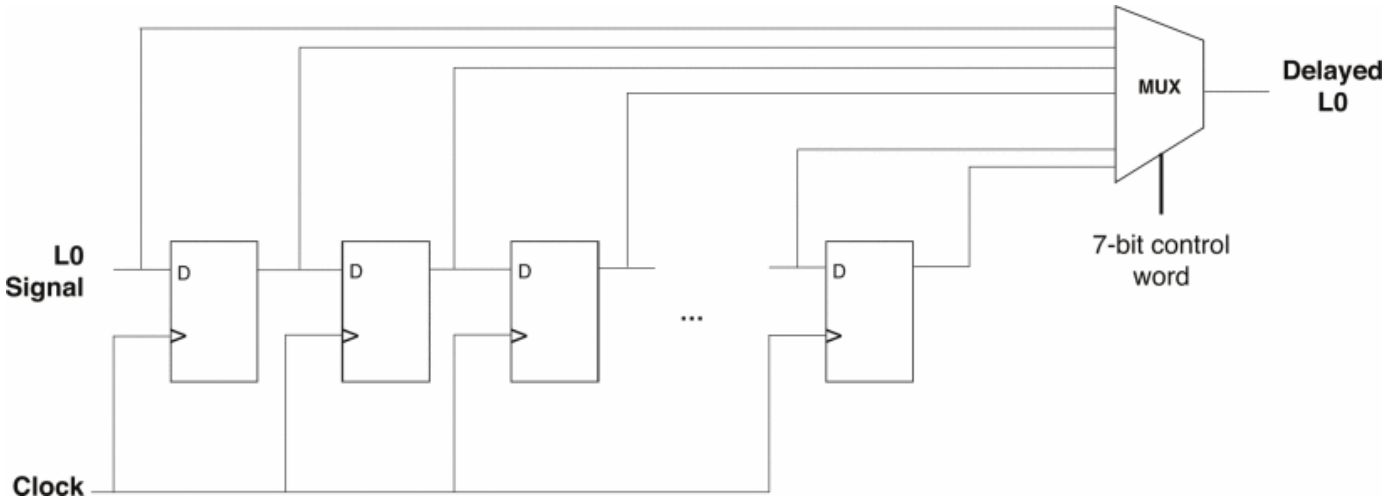
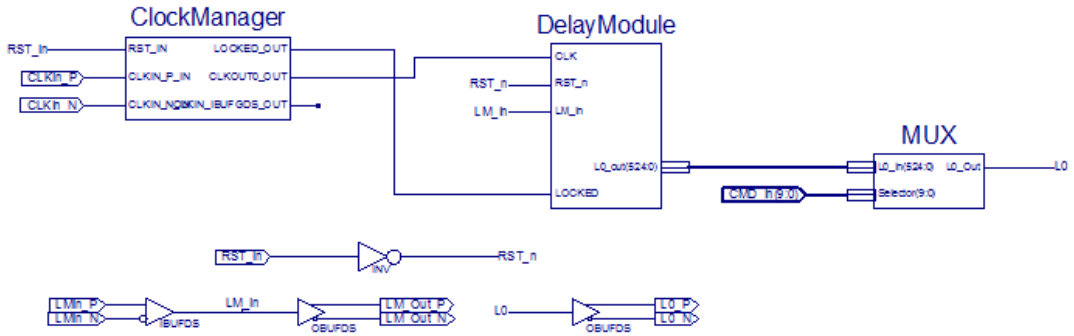
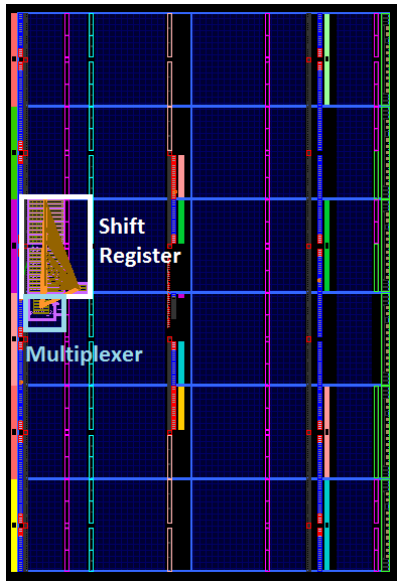


Figure: Implementation of Digital Delay Line

Design and Implementation

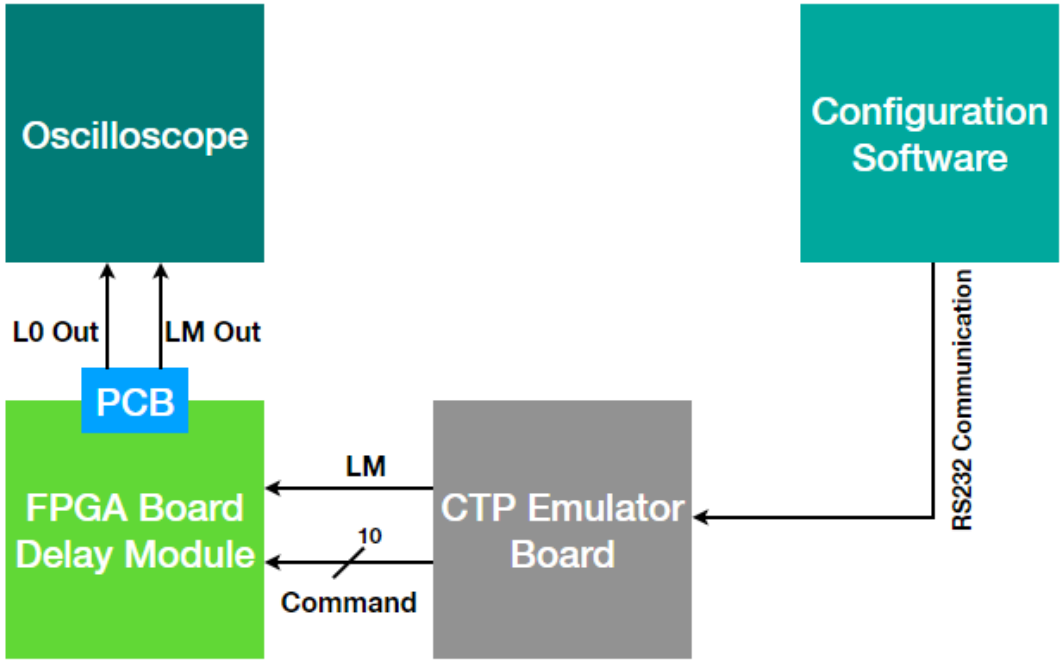


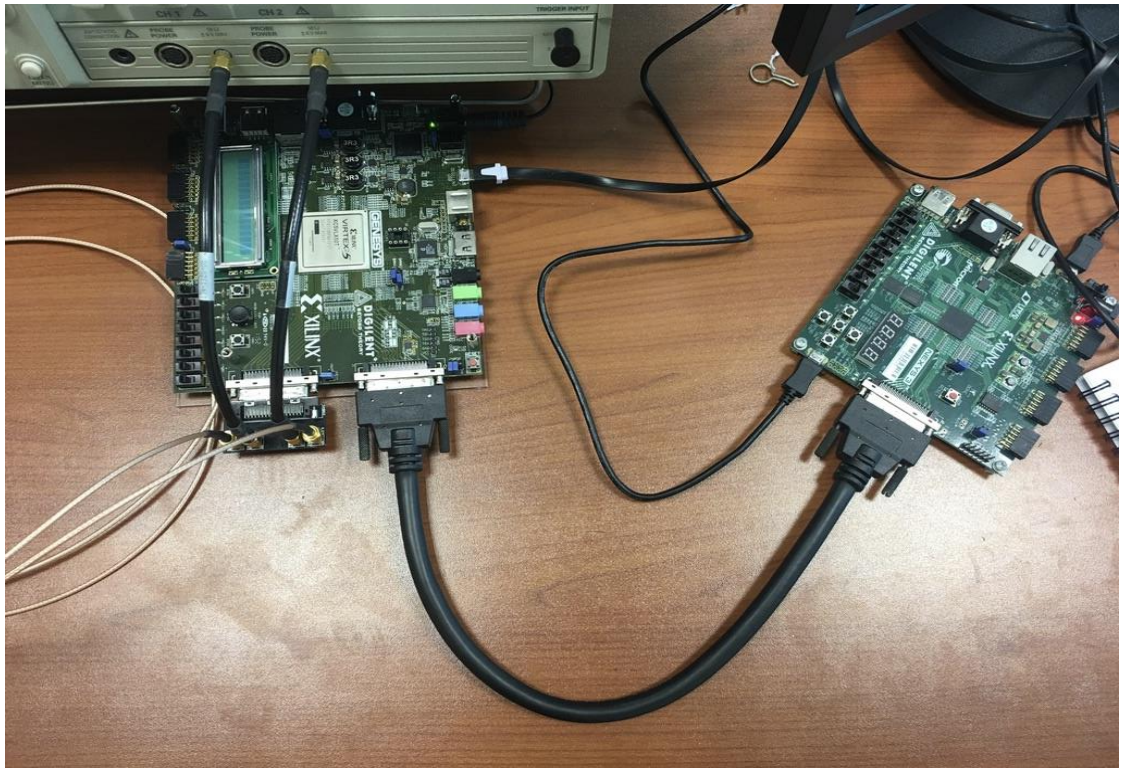


- ClockManager - 1 GHz Clock Generator
- Delay Module – Shift Register
- MUX – Multiplexer

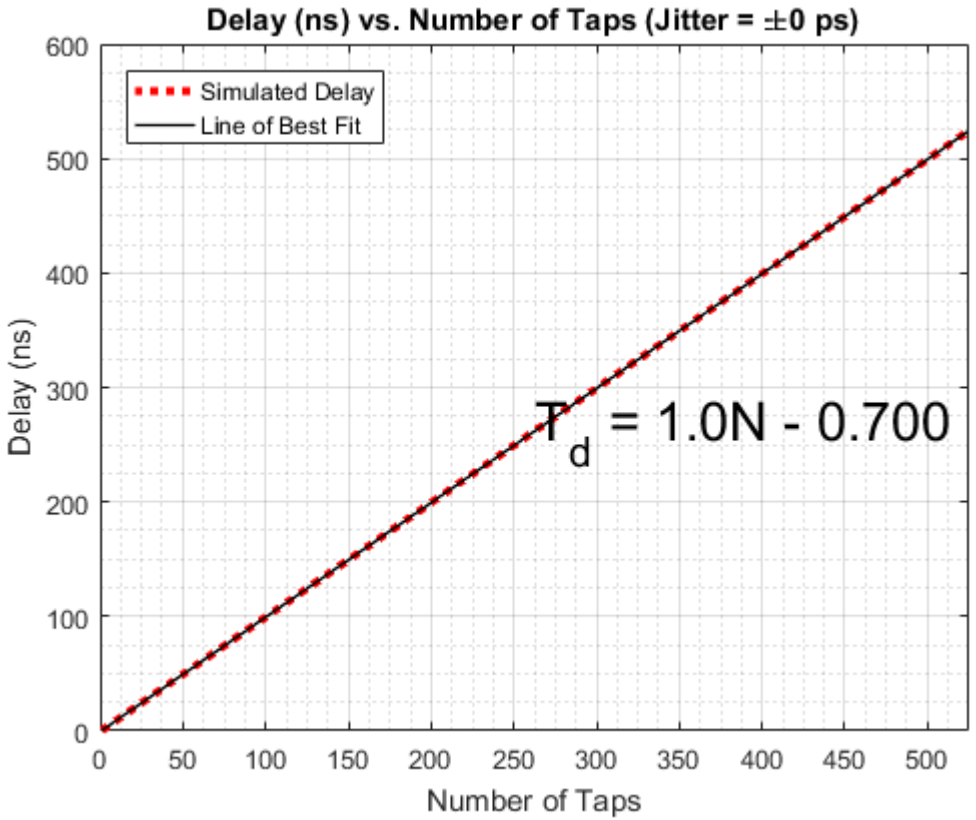
- Floorplanning to constrain occupied area by the Shift Register

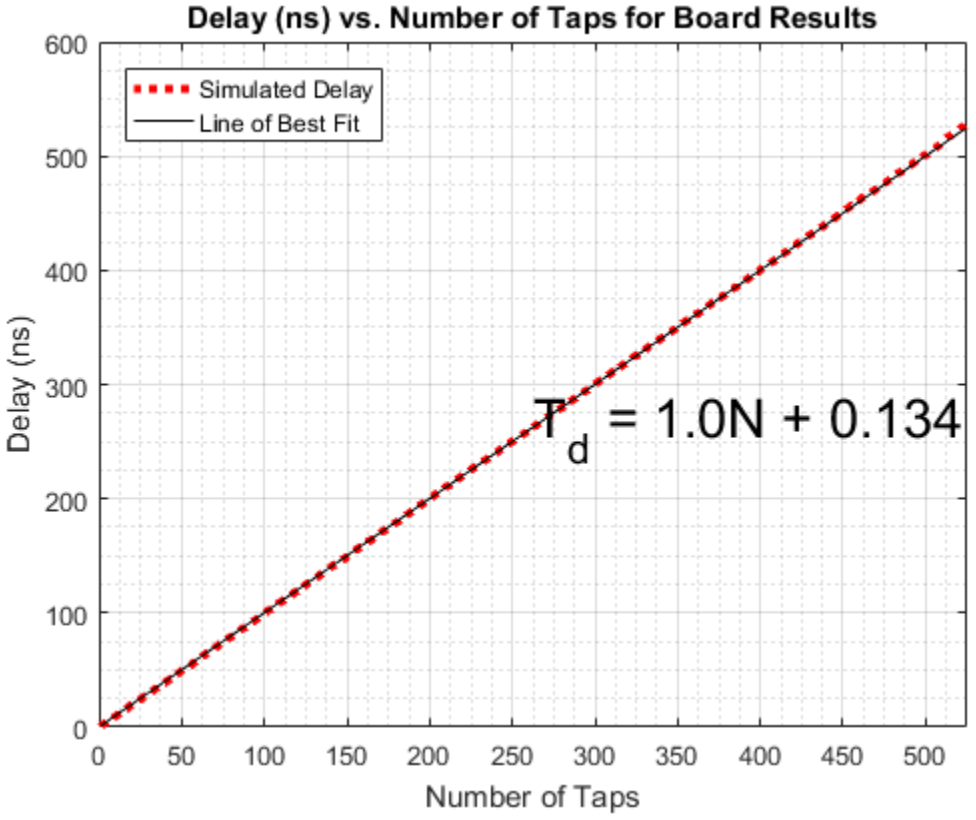
Testing


Oscilloscope
Configuration Software
L0 Out
LM Out
PCB
FPGA Board Delay Module
LM
10
Command
CTP Emulator Board
RS232 Communication



Results

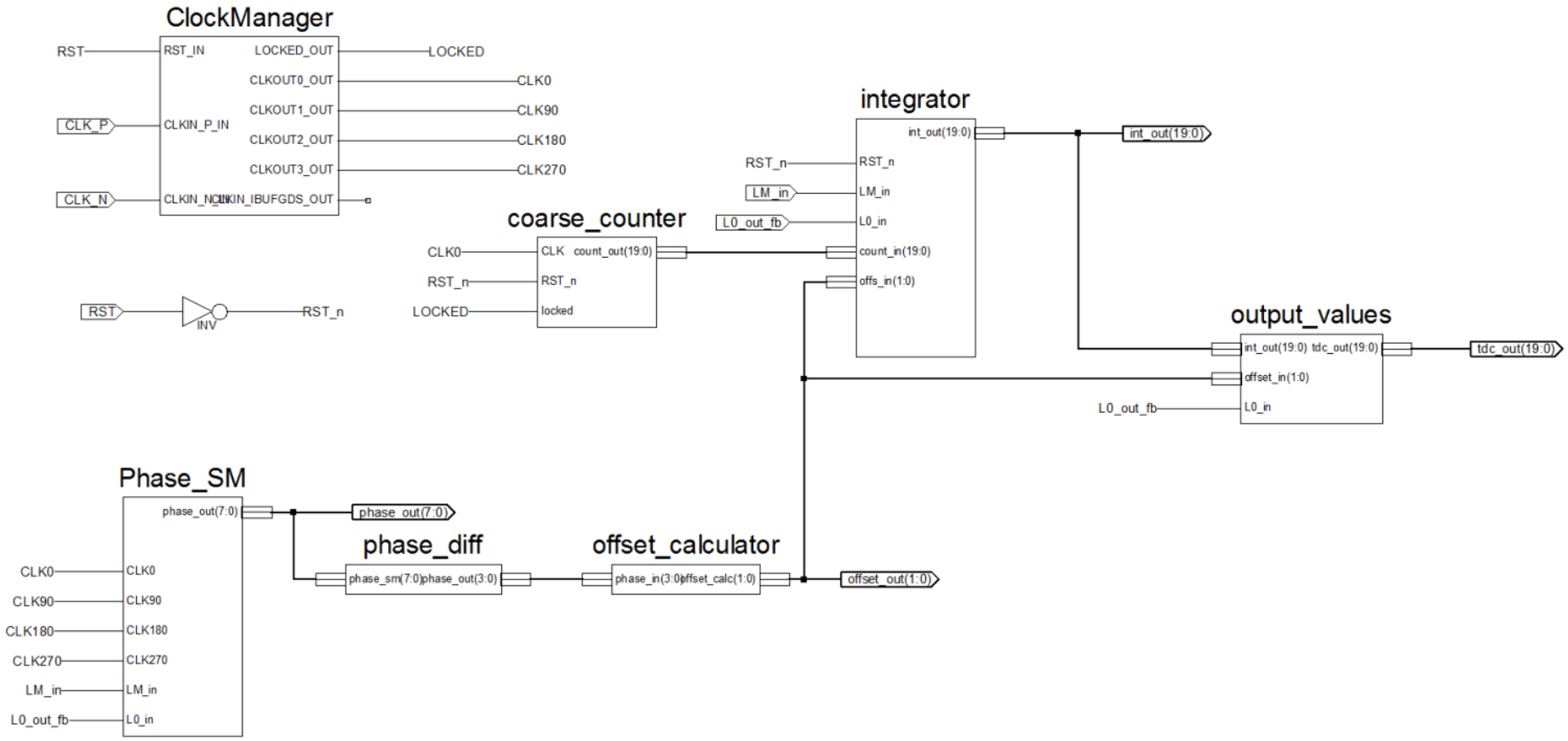

Delay (ns) vs. Number of Taps (Jitter = ±0 ps)
Simulated Delay
Line of Best Fit
T_d = 1.0N - 0.700
Delay (ns)
Number of Taps
0
100
200
300
400
500
600
0
50
100
150
200
250
300
350
400
450
500


Delay (ns) vs. Number of Taps for Board Results
Simulated Delay
Line of Best Fit
T_d = 1.0N + 0.134
Delay (ns)
Number of Taps
0
100
200
300
400
500
600
0
50
100
150
200
250
300
350
400
450
500

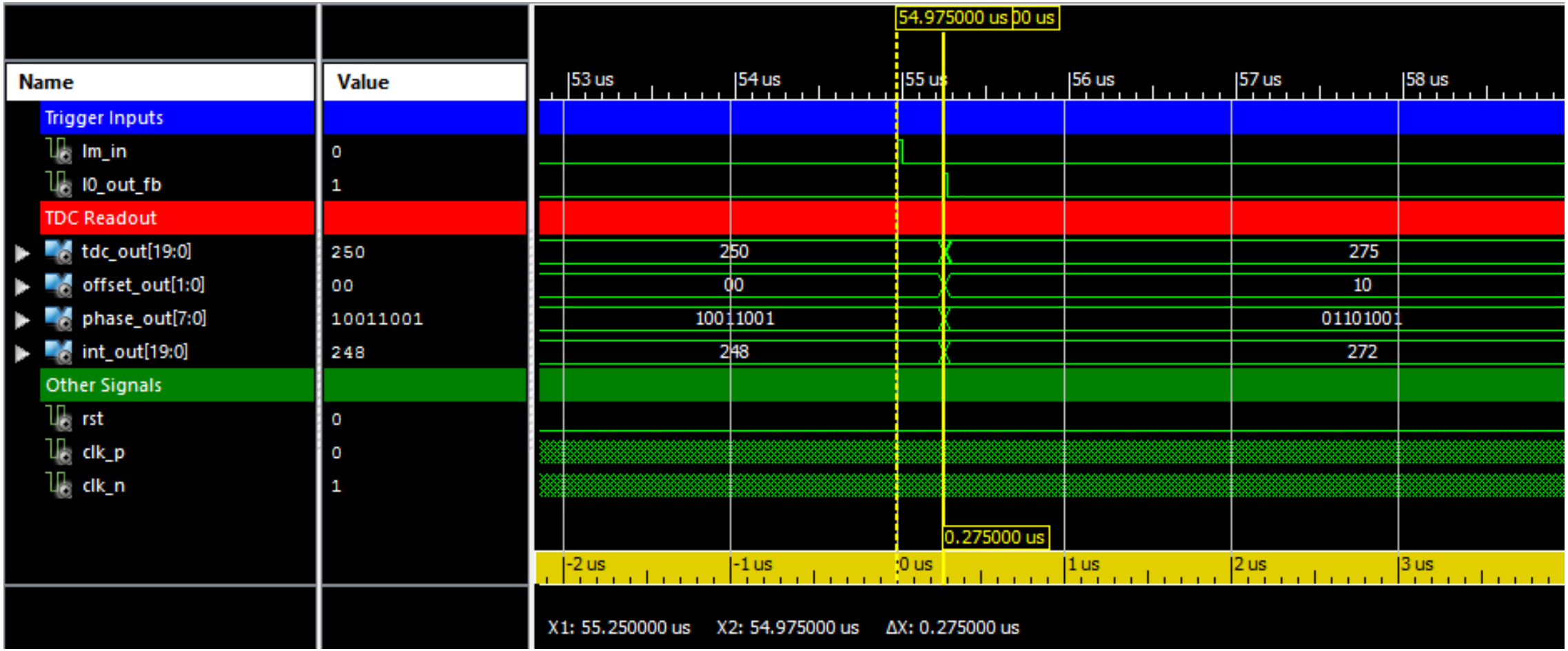
Monitoring Module

- Problem with this delay line is that there is an unpredictable offset.
  - Stems from the accumulation of jitter along the line
- One Solution is to use a control loop to monitor the delay and correct the multiplexer code, if the delay is more than +/- 1 ns

Monitoring Module



Monitoring Module - Results



Firmware Upgrades

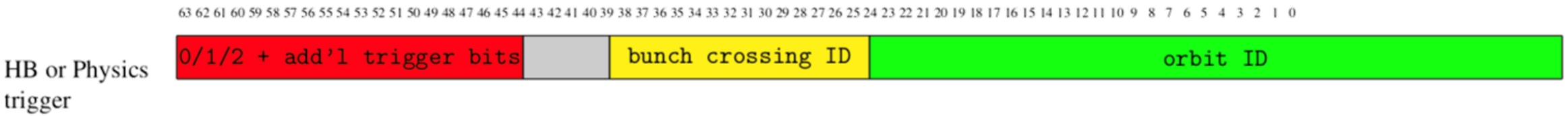
- Tests in Bld 581 on present Firmware were performed by Raul and myself
- Problem with v27 VHDL conversion of header module
  - Solved by changing header block to AHDL
  - No more corrupted header received
- Problem with errors in hardware?
  - Yes and No. Most probably what is resulting in errors from TB is the fact that we are running firmware from P2

- New Firmware so far:
  - Changed from unreliable reset module clock to one generated by PLL
  - Started new TTC module

New TTC Module Run3

- Writing of new TTC module for Run3 underway
- Data Format for Run3

Data	Word Number	Payload	Content
[0..15]	x	TType[0..15]	Trigger Type
[0..11]	x	BCID[0..11]	BCID
[0..15]	x	Orbit[0..15]	Orbit Low
[0..15]	x	Orbit[16..31]	Orbit High



New TTC Module for Run3

- Handles L0, L1 sequence
- Handles HB Trigger even when BUSY
- Header Builder by filling in respective values of the CDH

- No way of testing this so far as I cannot build a fake trigger message using the CTP Emulator.

Plans for 2019

- **January 2019**
  - We should have the new lab completed with Run3 LTU and C-RORC.
    - In this way we can test the various functionalities of the new firmware.
  - Tests at P2 of porting to VHDL (Run2 environment)
- **Final Design and Prototype of Fan-In/Fan-Out Module**
- **Final Prototype of Run3 Firmware**