Fabrication of active-edge detectors without support wafer using a unique "perforated edge" approach

O. Koybasi[1], A. Kok[1], A. Summanwar[1],
Marco Povoli[1], L. Breivik[1].

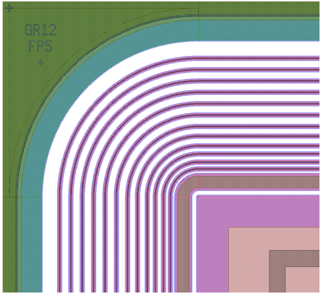
[1] SINTEF MiNaLab,Gaustadalleen 23 C, 0373, Oslo, Norway

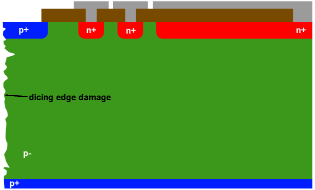
TREDI 2019 - 14th Trento Workshop on Advanced Silicon Radiation Detectors
Trento, Italy, February 25-27, 2019

Outline

1. Background
2. Achieving the active-edge without a support wafer
   - Development at SINTEF MiNaLab
   - Fabrication
   - Electrical characterisation
     - Dicing tests
     - Capacitance measurements
3. Future development
4. Conclusions

Edge-termination structures



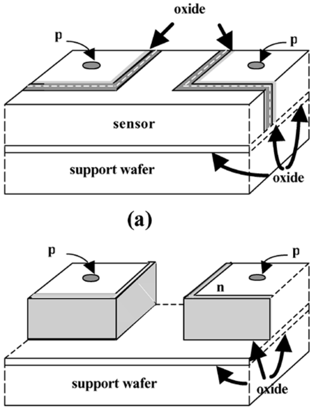


- The edge termination of radiation detectors is important
- Gradually dropping the potential and help increasing breakdown voltage
- Prevents current injection from the dicing region
- Some standard solutions include:
  - Combination of grounded and floating guard-rings[1]
  - Current terminating structures[2]
- Dead region around the sensors amounts to about 1-1.5mm
- Seamless tiling of multiple detectors to cover large areas is difficult

[1] L. Evensen, et al., NIMA 337 (1993), 44-52
[2] E. Noschis, et al., NIMA 574 (2007), 420-424

Active-Edge

Origin and development



[S. I. Parker, et. al., IEEE TNS, VOL. 53, NO. 3, JUNE 2006]
[C.J. Kenney, et al., NIMA 565 (2006), 272-277]

ADVANTAGES

- Reduction in the extension of the dead edge area
- Efficient tiling of sensors for seamless area coverage
- Complete isolation from the dicing lanes

DISADVANTAGES

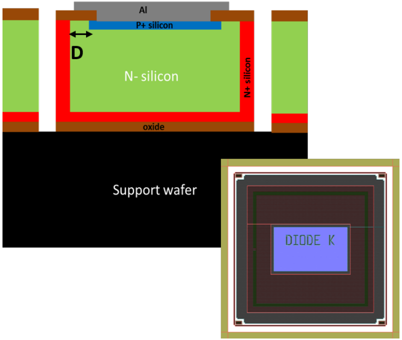
- Complicated fabrication process
- More expensive approach
- Necessary to use a support wafer during processing

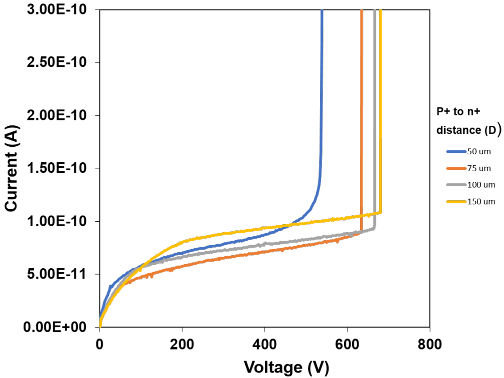
Active-edge at SINTEF MiNaLab

With support wafer

- Initial approach with support wafers
- Excellent electrical results
- Similar to planar IV
- Leakage current as low as $\sim$0.3 nA/cm^2

Without in-house bump-bonding and wafer grinding facilities, extremely difficult to address the issues with support wafer removal!





Achieving the active-edge without a support wafer

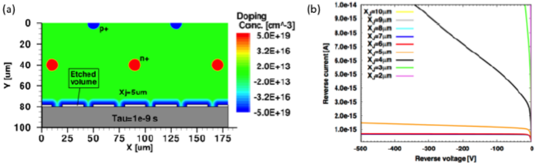
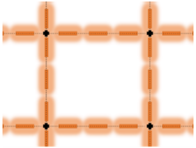
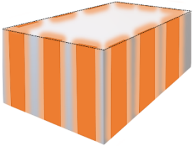


Figure 2. (a) Simulation domain, and (b) simulated current-voltage curves for different lateral diffusion length (x_j) in double-side 3D sensor with active edge by ohmic wall.

[G.-F. Dall Betta, 2012 JINST 7 C10006]

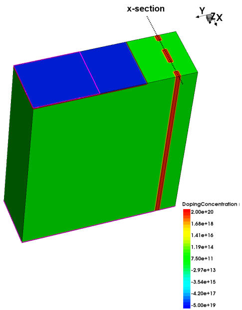


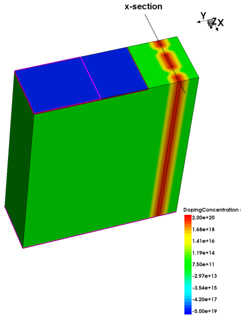


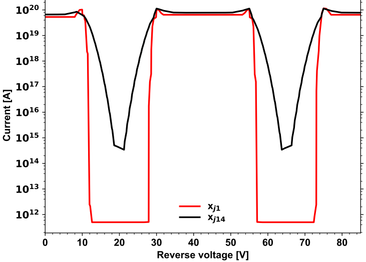
- The idea was proposed and investigated through numerical simulations
- Simulation results indicated that this approach could deliver an active-edge termination without etching a full trench
- Necessary to demonstrate fabrication feasibility and mechanical integrity of the wafer
- Perform the tuning of the trench aspect ratio to achieve the desired depth

Development at SINTEF MiNaLab

Numerical simulations (1)

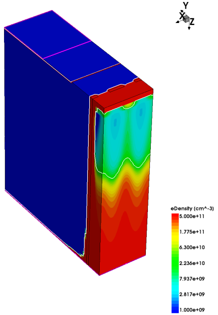


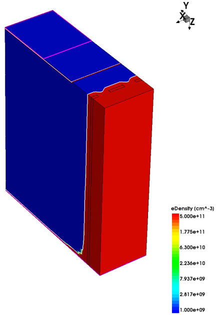


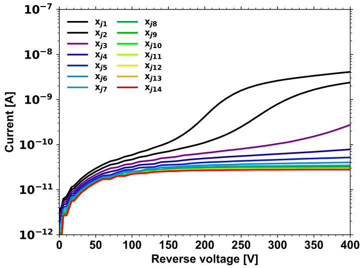


- Through numerical simulation investigate the dopant depths required to achieve isolation from the dicing edge
- At the edge, the lifetimes are reduced to 1ns to simulated a highly damaged cut region
- The I-V curve is simulated for different dopant depths

Numerical simulations (2)

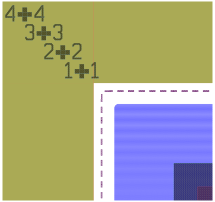


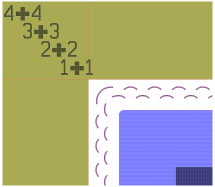


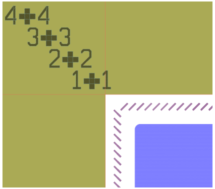


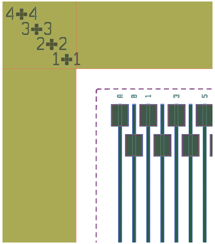
- For a shallow dopant depth there is no ”active-edge” formation and the depletion region can reach the dicing region
- With deeper doping profiles, it is possible to achieve a full active-edge
- The dopant depth depends on the distance between the trenches
- The distance between trenches depends on the requirements for the mechanical strength of the wafer

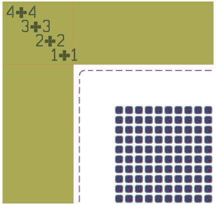
Layout design





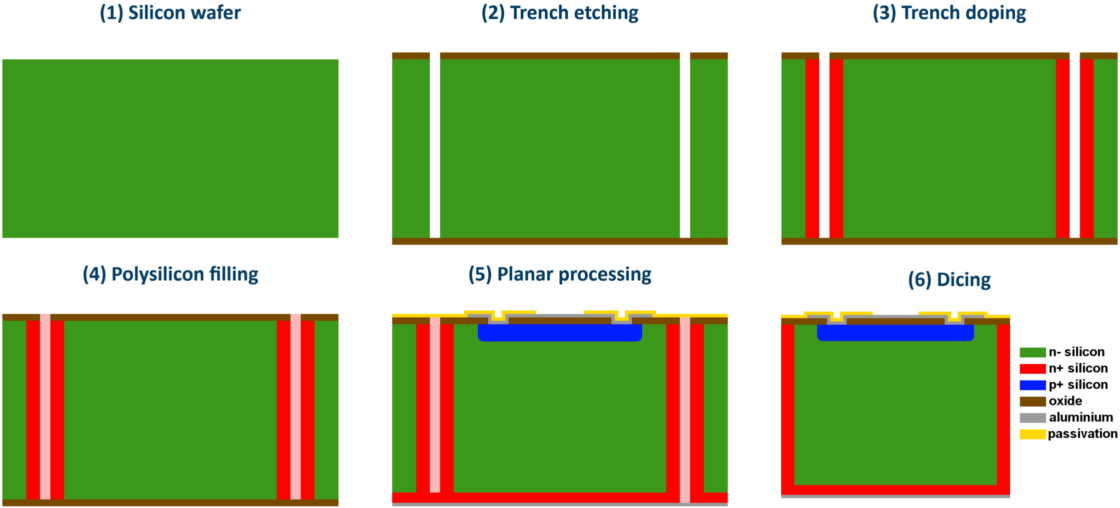




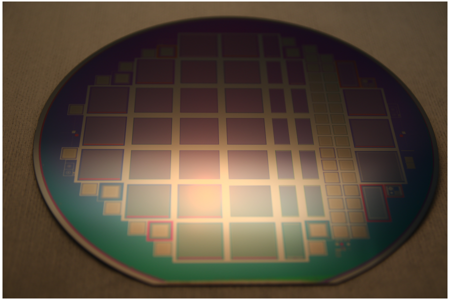


- Diodes with different trench configuration ($5 \times 5 mm^2$)
- Strip detectors with $75 \mu m$ pitch
- Medipix sensors
- Test structures for process monitoring
- Dicing marks at different distances from the trench

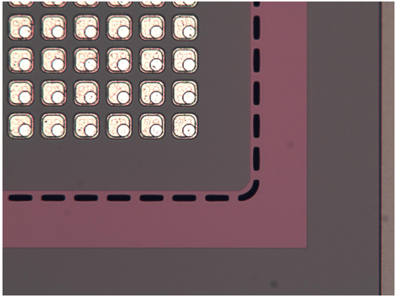
Fabrication (1)



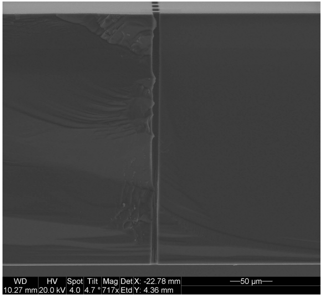
Fabrication (2)



- Picture of a full wafer



- Corner of a Medipix sensor

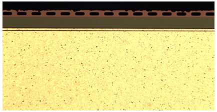


- SEM picture

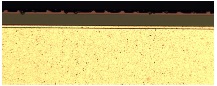
Electrical characterisation (1)

Dicing tests

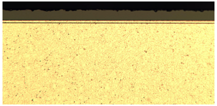
Dicing at X = 10μm (outside)

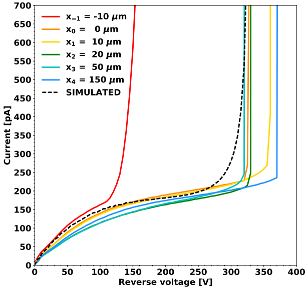


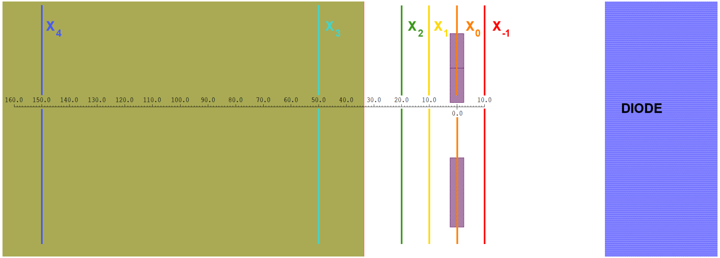
Dicing at X = 0μm (in the trench)



Dicing at X = -10μm (inside)

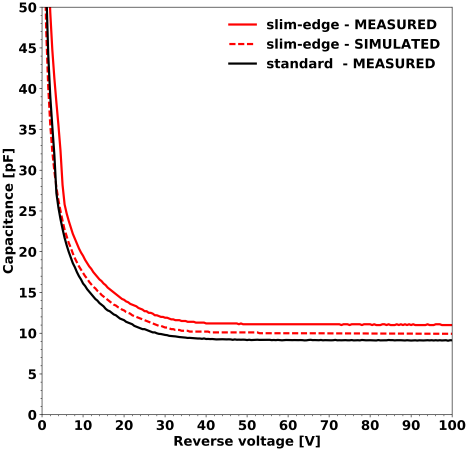


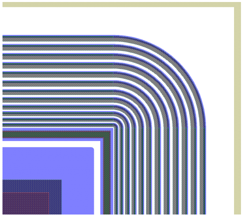


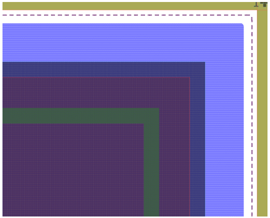


- Test carried out on diodes
- The diodes are etched at different distances from the trench and the I-V is measured again
- No increase in current is observed even when dicing inside the segmented trench
- To see current increase we must dice 10μm inside the active area

Electrical characterisation (2)



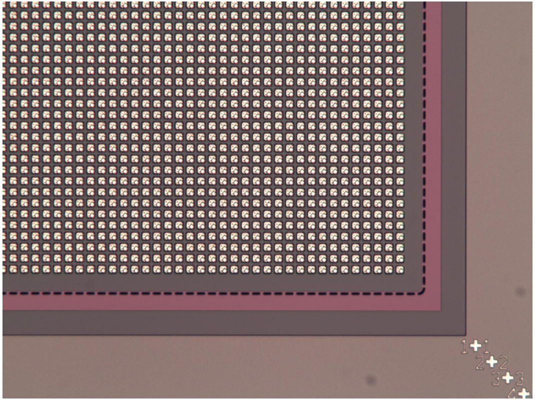




- The short edge termination gives an increase in capacitance as expected
- The increase amounts to about 10%
- Good agreement with numerical simulations

Final considerations and future development

- This technology was developed on N-type substrates but can be transferred to P-type as well
- It is only considered production level for 300μm thick substrates
- For thicker substrates the aspect ratio of the trenches needs to be adjusted and the quality of the photo lithography following the trench etching needs to be assessed
- It might be necessary to move away from resist spinning if the trenches become too wide
- These aspects will be evaluated and developed in the near future



Conclusions

- We have succesfully developed a fabrication procedure to produce active-edge devices without using a support wafer
- The electrical characterisation returned excellent results and the devices work as expected and in agreement with numerical simulations
- Further development is necessary for thicker substrates (>300μm)
- This technology can also be applied to our N-on-P process

SINTEF

Technology for a better society