Measurement of effective space charge concentration vs. neutron fluence in p-type substrates from LFoundry

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RD50

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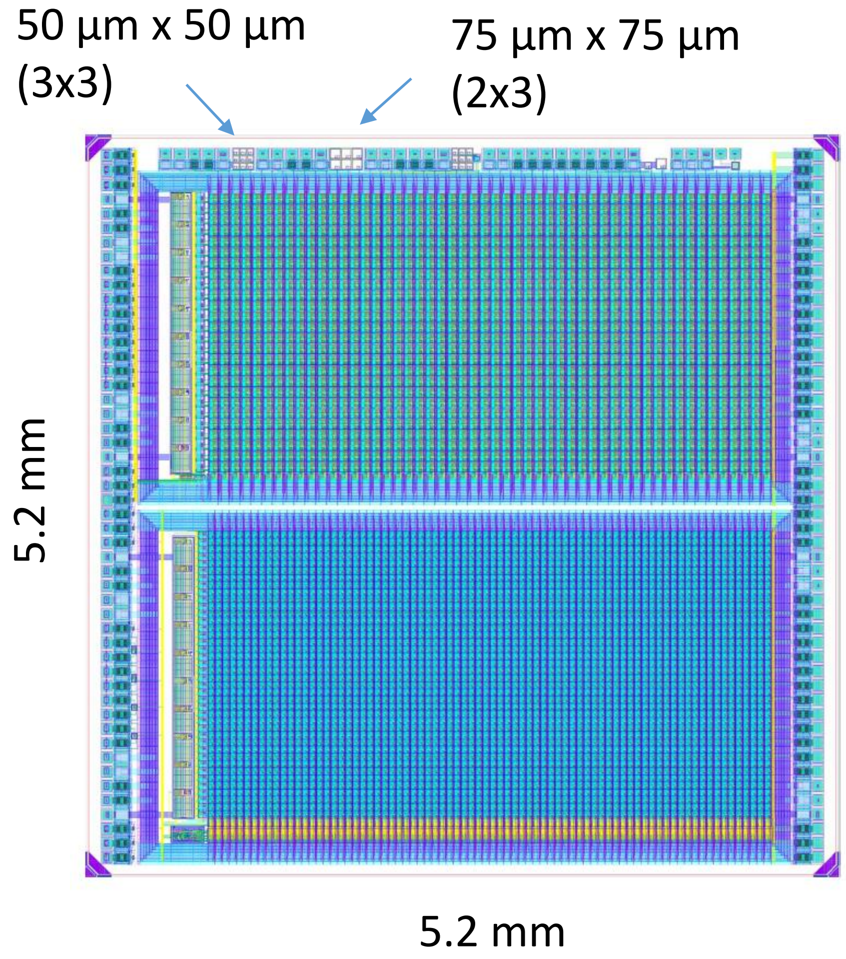
Introduction

- RD50 submitted CMOS pixel detector prototype chip *RD50-MPW1* in 150 nm LFoundry process
- chips were produced on p-type wafers in 2 different initial resistivities:
  ~ 500 Ωcm and ~1.9 kΩcm
- chips were irradiated in reactor in Ljubljana to several different fluences ranging from
  1e13 n/cm² to 2e15 n/cm²
- depletion depth at different bias voltages was measured with E-TCT
- N_{eff} estimated from depletion depth and studied as a function of neutron fluence

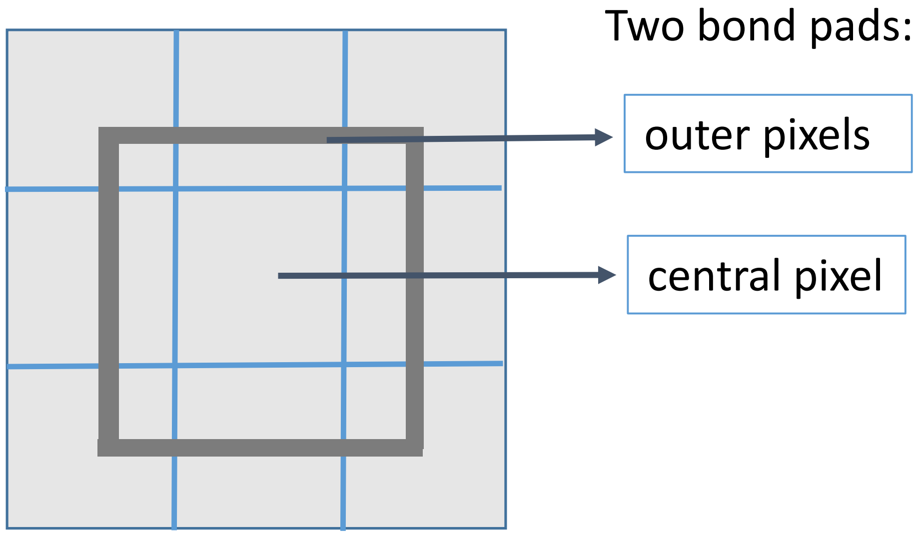
RD50-MPW1 CMOS chip

Passive pixel arrays for E-TCT



Measurements made with:

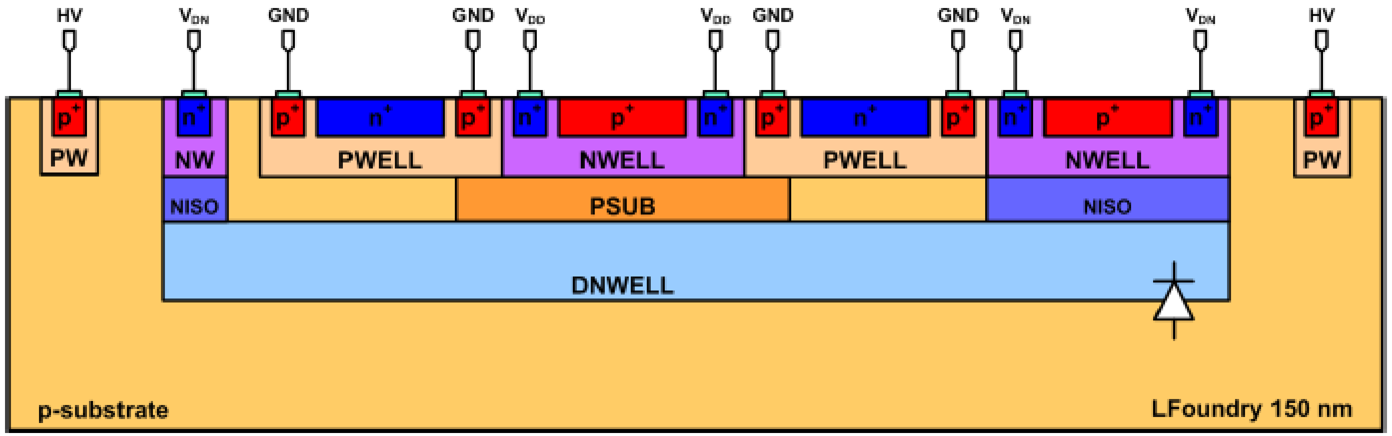
- 3x3 pixel array of 50 µm x 50 µm pixels
- central pixel to read out
- Outer pixels connected together



<u>RD50 CMOS chip</u>

Scheme of a pixel

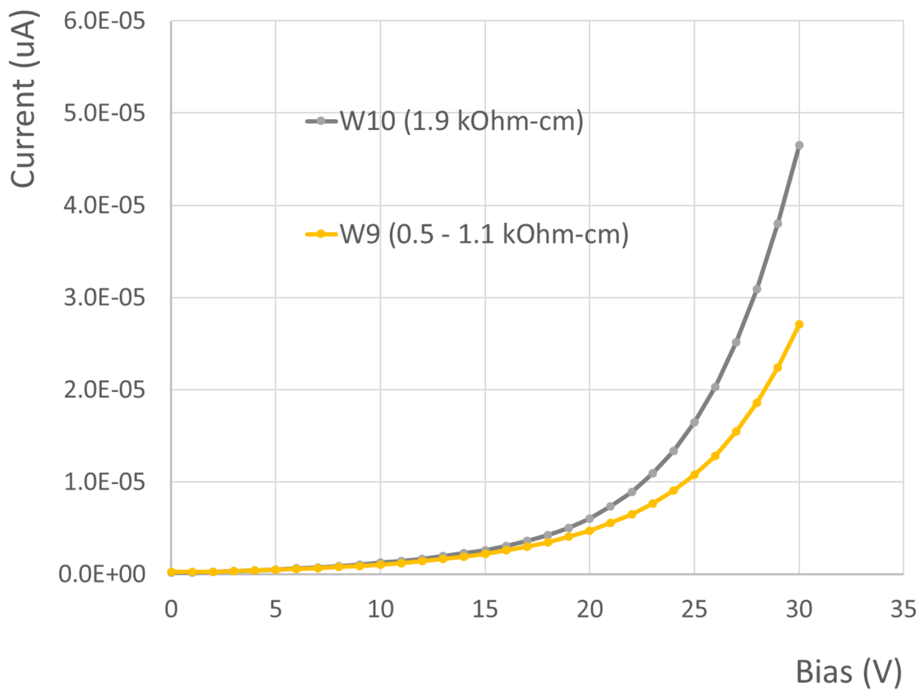
- Passive pixel: same scheme as active pixel except there is no transistors in the wells
- DNWELL connected to bias voltage and to the amplifier via bias-T
- P-substrate connected to ground

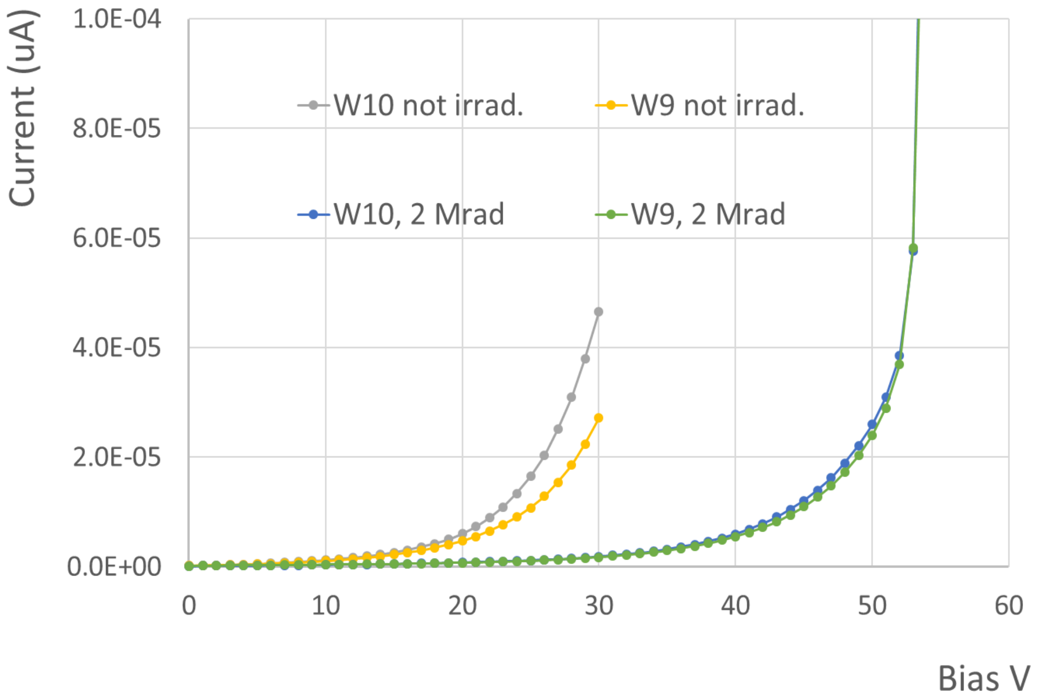


Chips are not thinned, back plane not processed, substrate biased through the implants on top

Detector current before irradiation

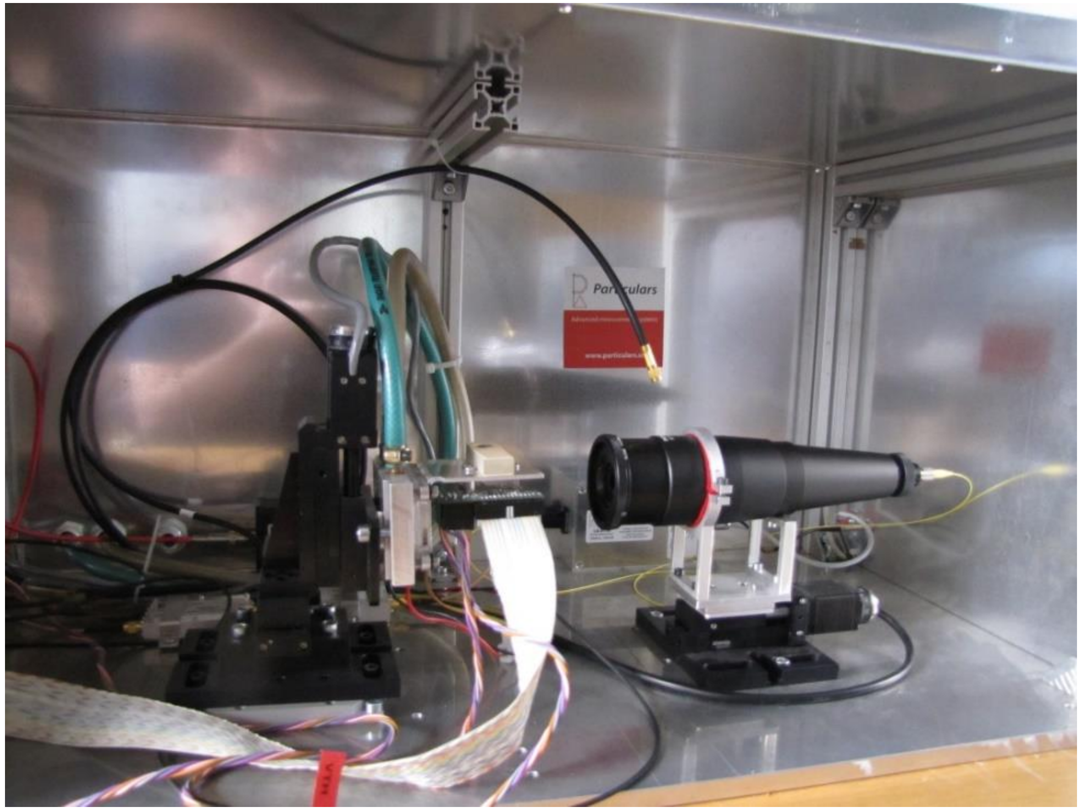
Current measured on outer 8 pixels of 3x3 pixel array (50x50 um² pixel)





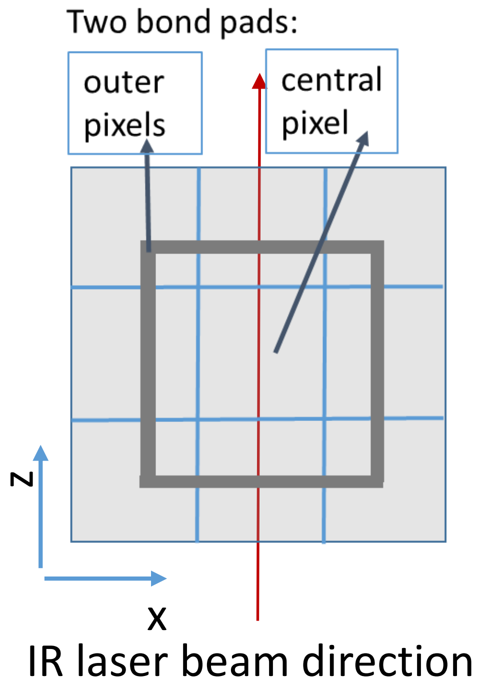
- high current before irradiation, several reasons for this, more detail:
  ➔ talk by Matthew Lewis Franks later today
- chips were exposed to 2 Mrad TID from background radiation in the reactor
  ➔ at zero reactor power there is no neutrons, only photons
  ➔ leakage current smaller after 2 Mrad TID irradiation

Edge TCT setup

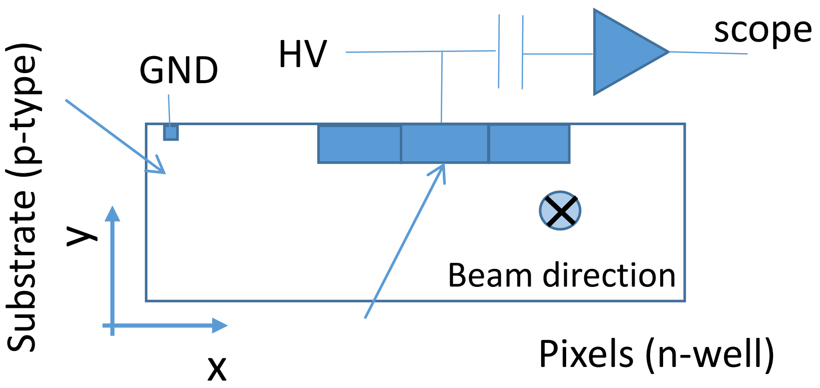


(more details: www.particulars.si)

Top view:

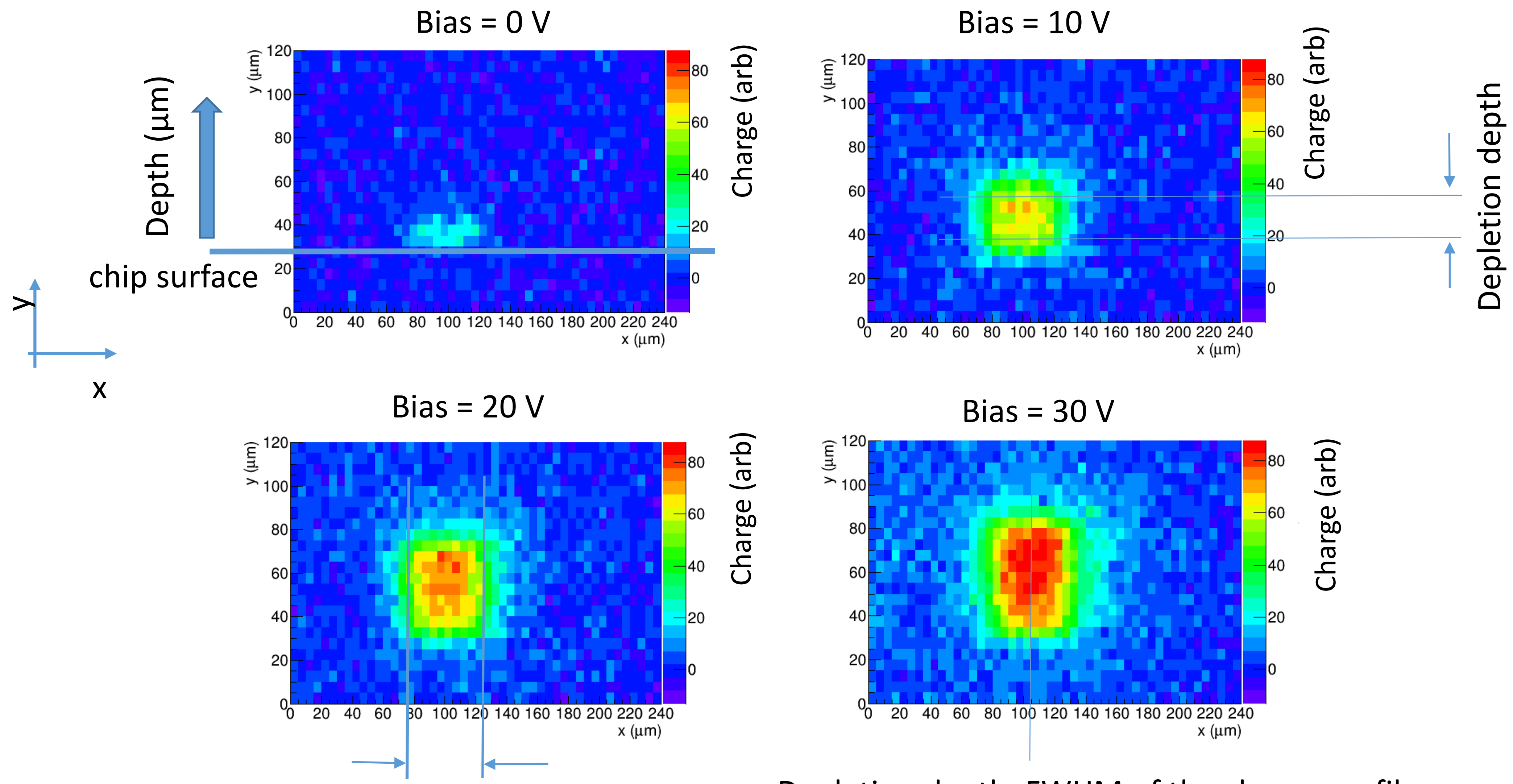


Side view:



Before irradiation

Central pixel connected to readout amplifier

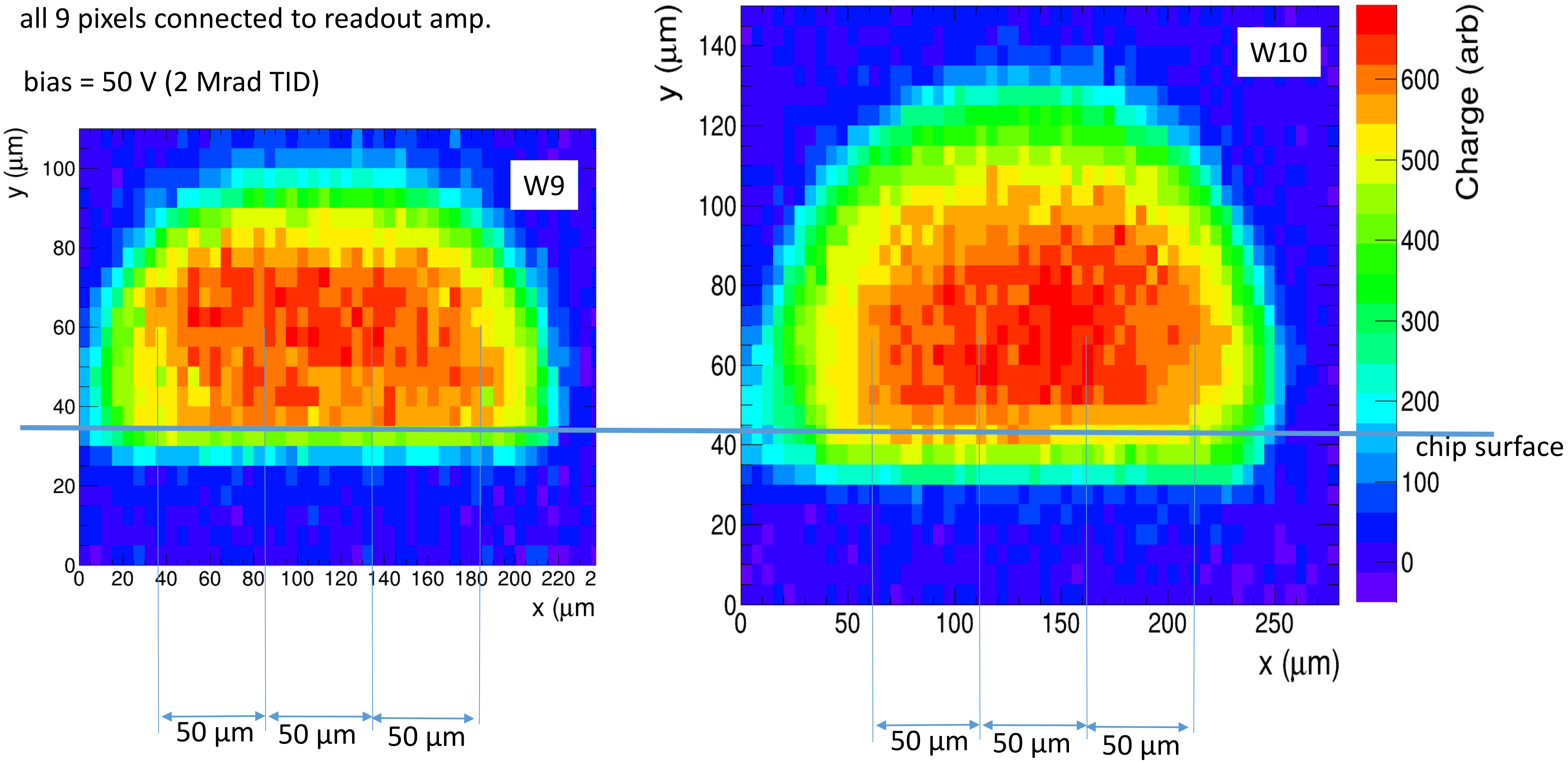


Pixel width 50 µm

Depletion depth: FWHM of the charge profile across the centre of the pixel

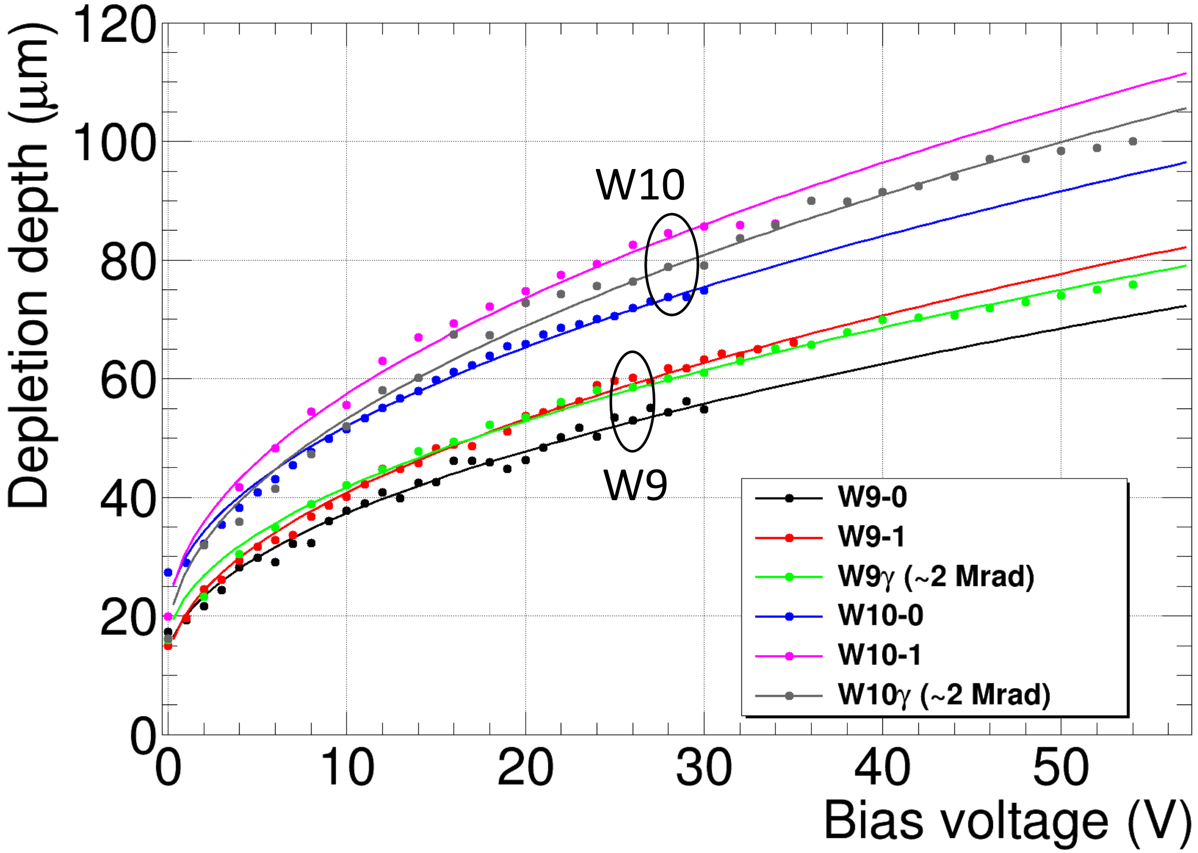
Charge collection profile

- all 9 pixels connected to readout amp.
- bias = 50 V (2 Mrad TID)



Before irradiation

- charge collection profile measured across the middle of central pixel
- depletion depth: FWHM of charge profile



Fit: $$d = d_0 + \sqrt{\frac{2\varepsilon\varepsilon_0}{e_0 N_{eff}} \cdot V_{sub}}$$ ➔ extract N_{eff}

parameter d_0: built in voltage, finite laser beam width…

W9:

N_{eff} = (1.8 ± 0.3)· 10^{13} cm^{-3}

Resistivity: 720 Ωcm ± 150 Ωcm

W10:

N_{eff} = (1.0 ± 0.2)· 10^{13} cm^{-3}

Resistivity: 1.3 kΩcm ± 0.15 kΩcm

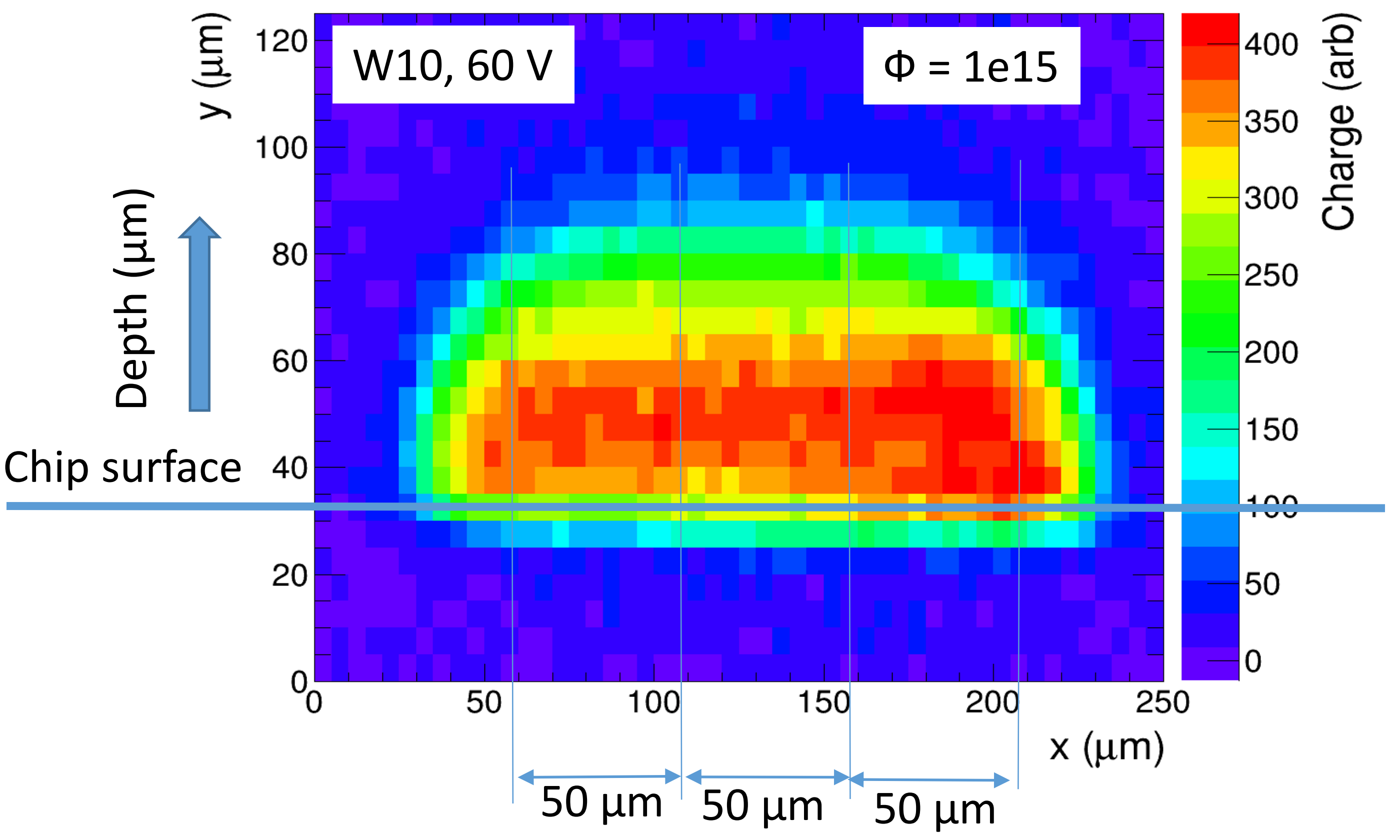
➔ somewhat lower than nominal 1.9 kΩcm

No observable effect of 2 Mrad TID on N_{eff}

Chips irradiated in reactor in Ljubljana

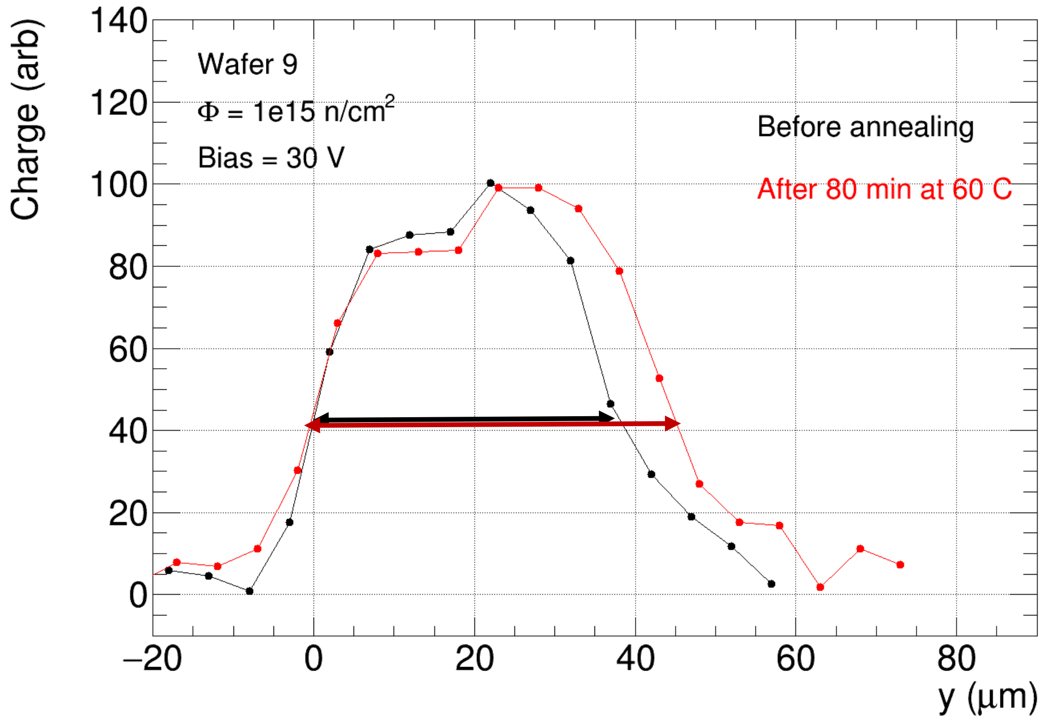
- fluences: 1e13, 2e13, 5e13, 1e14, 2e14, 5e14, 1e15, 2e15,
- each fluence separate chip

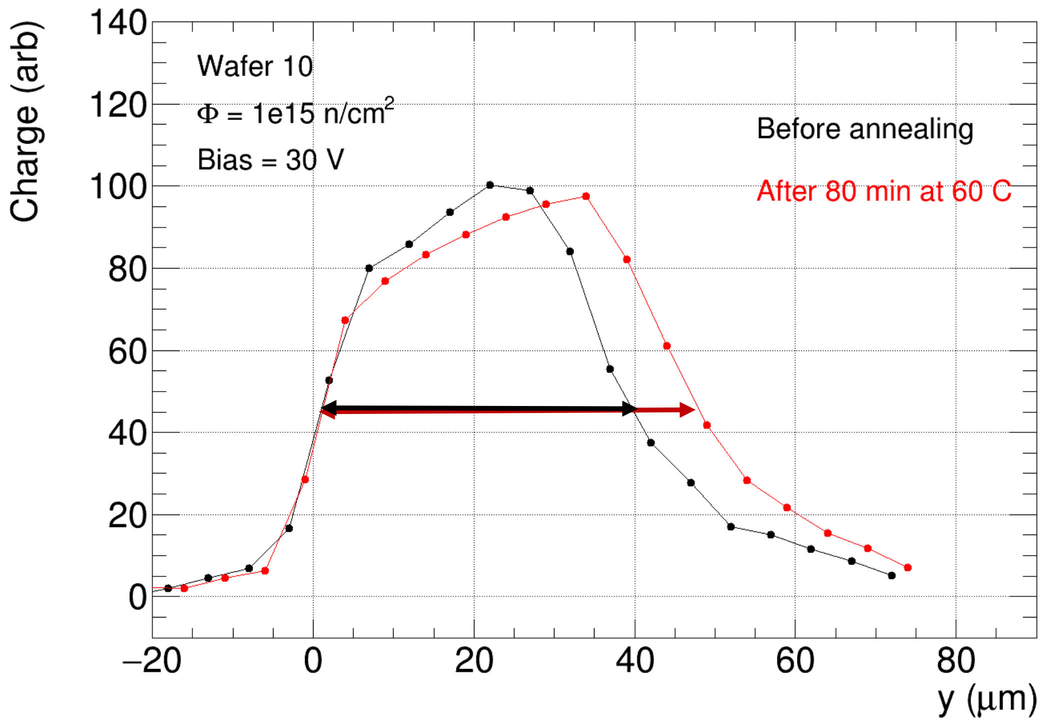
➔ no efficiency gaps between pixels



Annealing

➔ depletion depth increases by up to ~ 20 % after annealing for 80 minutes at 60 C

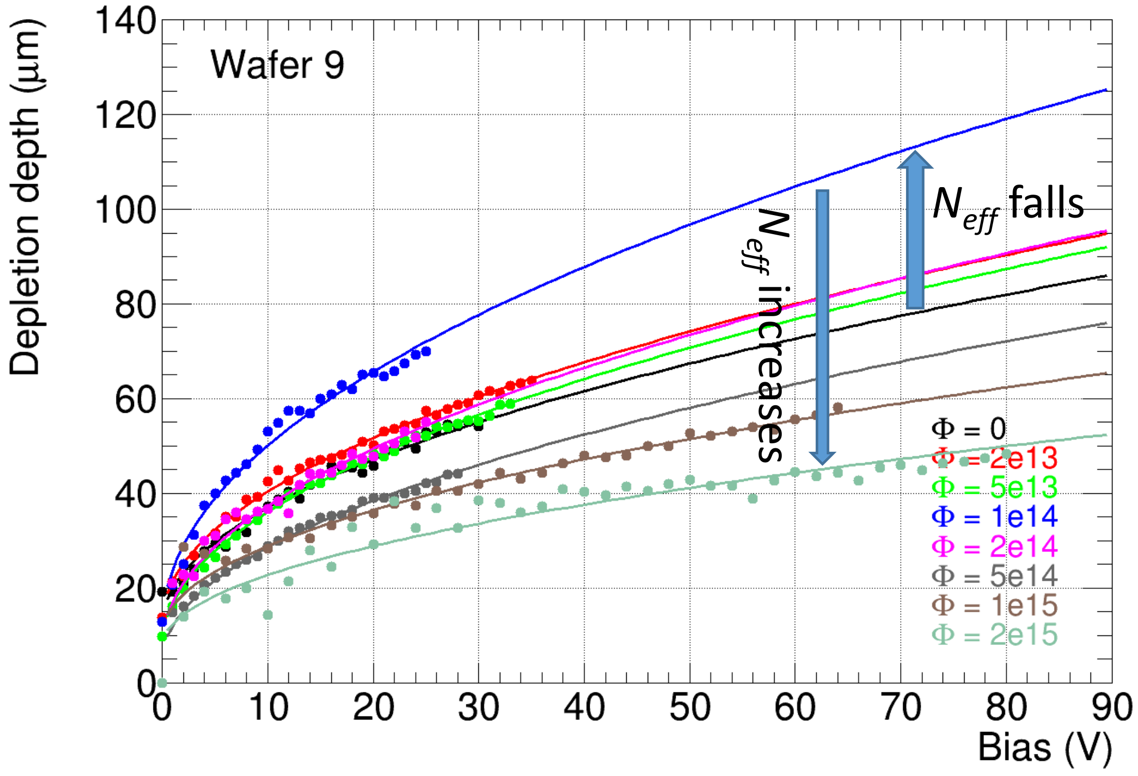




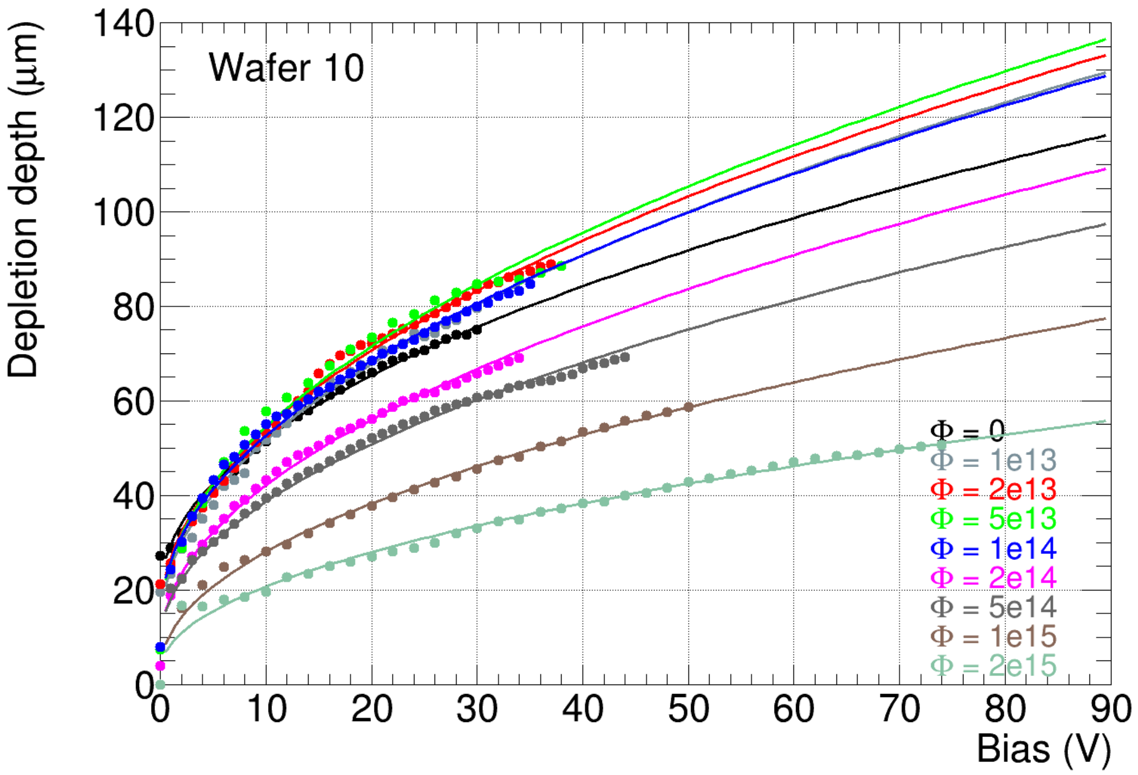
After irradiation with neutrons

- depletion depth vs. bias voltage
- measured after annealing for 80 min at 60°C

W9 (lower resistivity)



W10 (higher resistivity)

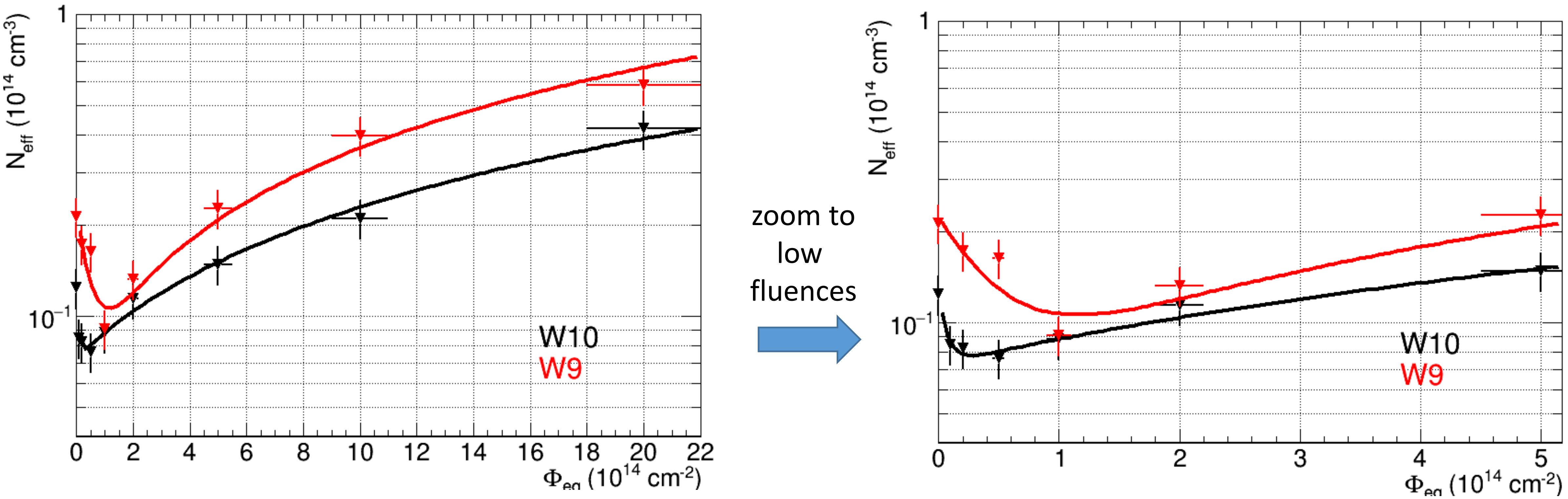


- depletion depth changes with irradiation
- acceptor removal effects

N_{eff} vs. fluence

Fit: $$N_{\mathrm{eff}} = N_{\mathrm{eff0}} - N_{\mathrm{c}} \cdot (1 - \exp(-c \cdot \Phi_{\mathrm{eq}})) + g_{\mathrm{C}} \cdot \Phi_{\mathrm{eq}}$$

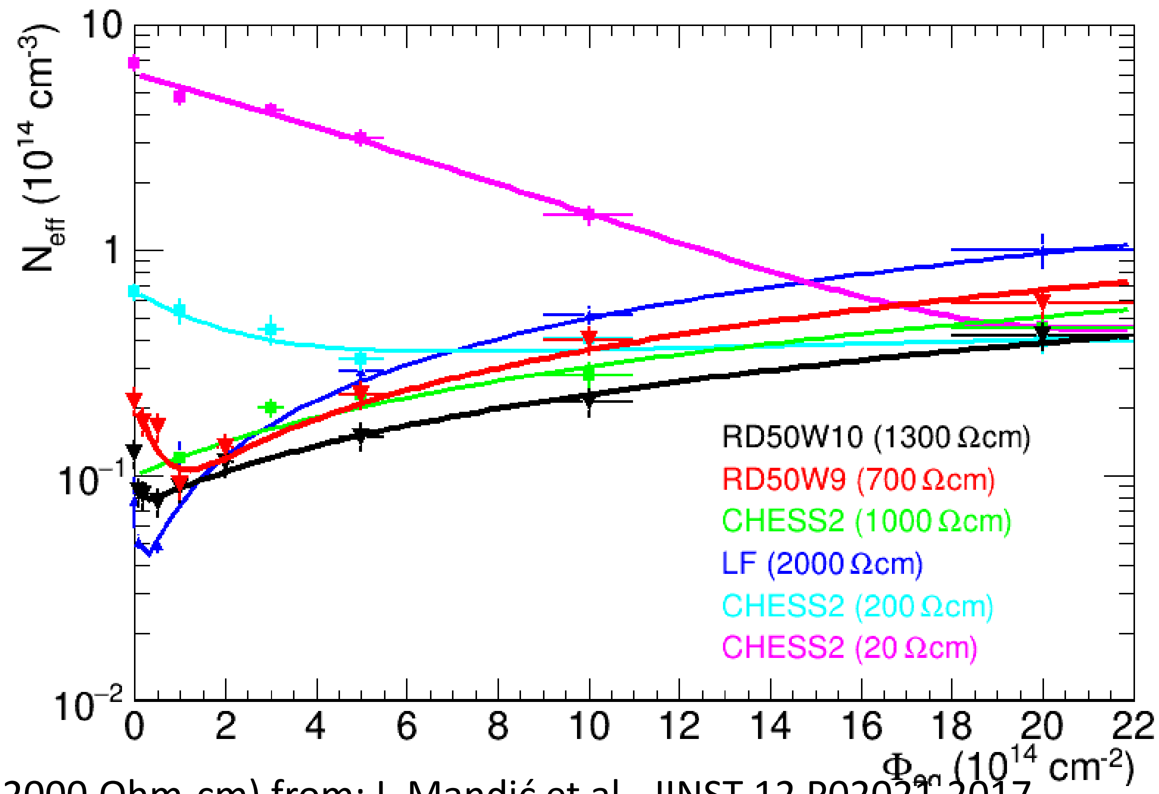
	N_{eff0}	N_c/N_{eff0}	c	g_c
W9	2.2e13 cm^{-3}	0.75	2.1e-14 cm^2	0.031 cm^{-1}
W10	1.2e13 cm^{-3}	0.41	14 e-14 cm^2	0.016 cm^{-1}



Compare with other measurements

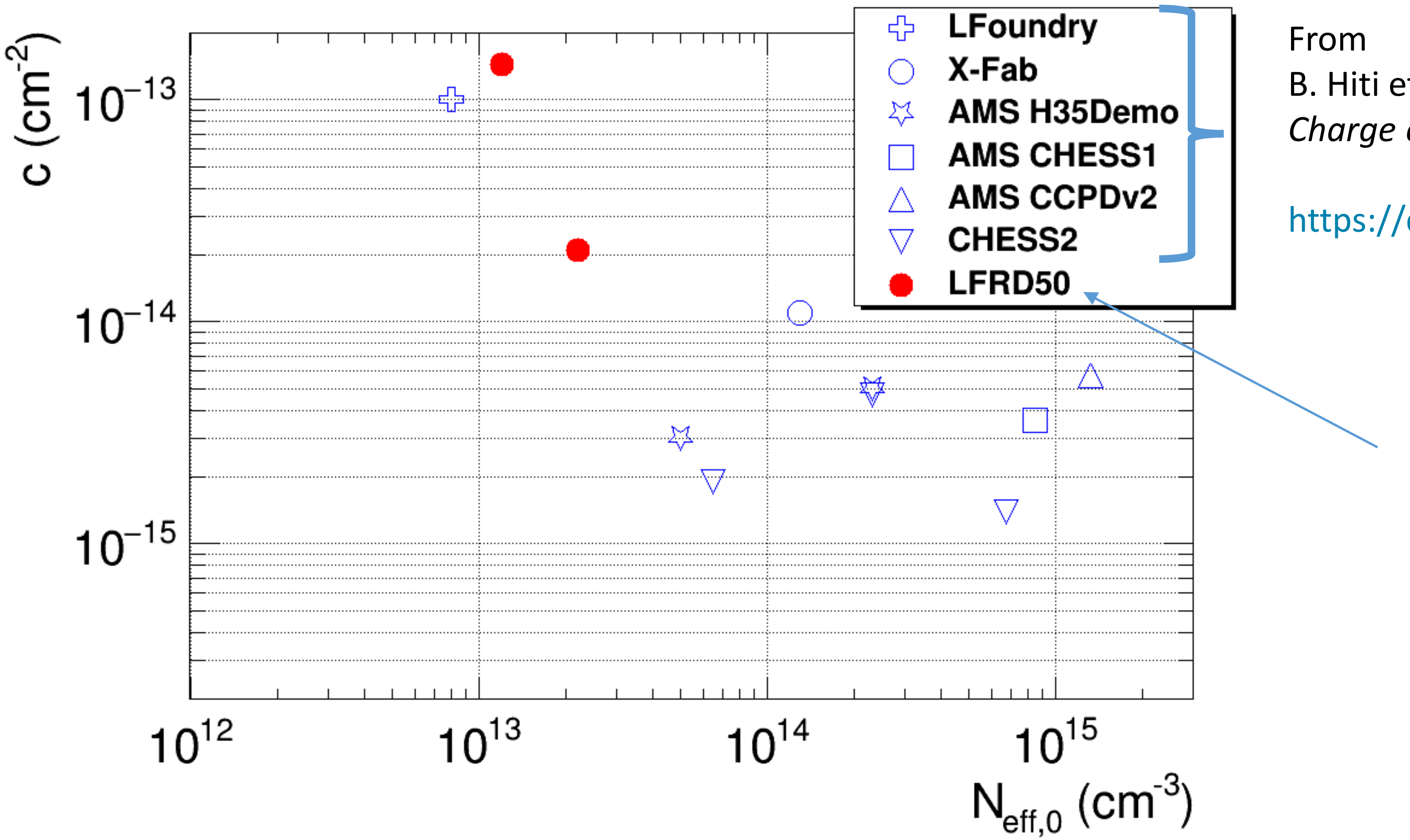
- this measurement consistent with other substrates with similar initial resistivity

- low resistivity 20 Ωcm (CHESS2, AMS): improves with fluence in this fluence range but large initial N_{eff}
- resistivity ~ 200 Ωcm, (CHESS2, AMS): smallest change of N_{eff} in this fluence range



- LF (2000 Ohm-cm) from: I. Mandić et al., JINST 12 P02021 2017
- CHESS2 from: B. Hiti et al, (NIMA) https://doi.org/10.1016/j.nima.2018.07.022

Compare removal parameter ***c*** with other CMOS substrates

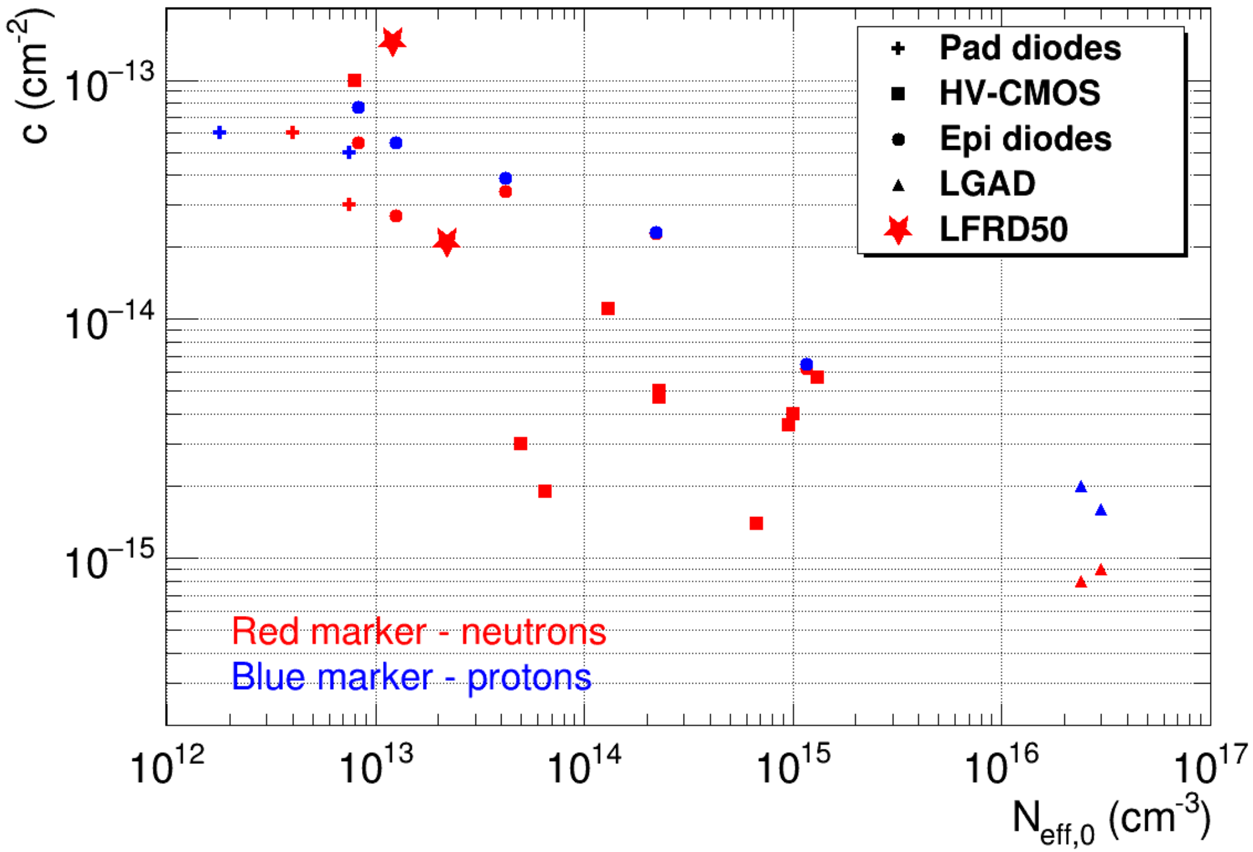


From
B. Hiti et al.,
Charge collection in irradiated HV-CMOS detectors

https://doi.org/10.1016/j.nima.2018.07.022

Summary for CMOS, diodes, LGAD

- LRRD50 fit into the summary plot:
  ➔ *c* drops with increasing N_{eff0}
  ➔ *c* higher after proton irradiation



Epi diodes:
- P. Dias de Almeida, 32nd RD50 Workshop, 2018
- https://indico.cern.ch/event/719814/contributions/3022586/
- K. Kaska
  http://repositum.tuwien.ac.at/obvutwhs/content/titleinfo/1633435

LGAD:
- G. Kramberger, JINST Vol. 10 (2015) P07006

Pad diodes:
- G. Kramberger, 26th RD50 workshop, Santander, 2015
  https://indico.cern.ch/event/381195/contributions/905665/

CMOS:
- A. Affolder et al., JINST 11 P04007 2016
- I. Mandić et al., JINST 12 P02021 2017
- E. Cavallaro et al., JINST 12 C01074 2017
- B. Hiti et al., JINST 12 P10020 2017
- B. Hiti et al, (NIMA) https://doi.org/10.1016/j.nima.2018.07.022

See also:
- M. Moll, IEEE TNS 65 (2018) p.1561
  https://doi.org/10.1109/TNS.2018.2819506
- G. Kramberger, HSTD11, Okinawa, 2017
  https://indico.cern.ch/event/577879/
- Y. Gurimskaya, 33rd RD50 workshop
  https://indico.cern.ch/event/754063/contributions/3222777/

Summary

- measurements with irradiated pixel detector structures on *RD50-MPW1* chip by LFoundry, two initial resistivites

- TID irradiation by background radiation in the reactor (no neutrons)
  ➔ smaller leakage current measured after 2 Mrad TID
    - may help to identify the source of the excessive detector current measured before irradiation

  ➔ no effect of 2 Mrad TID on depletion depth

- neutron irradiation
  ➔ uniform charge collection efficiency across pixel structure → no efficiency gaps observed
  ➔ depletion depth increases (~ 10 %) after annealing for 80 minutes at 60°C

  ➔ N_{eff} measured with E-TCT and studied as the function of fluence
    ➔ acceptor removal parameter ***c*** extracted
      - results consistent with previous measurement
        ➔acceptor removal constant higher for substrates with lower initial resistivity

Depletion depth vs. fluence

- depletion depth at 100 V

  ➔ calculated from function fitted to depletion vs. bias (see slide 12):