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# Measurement of effective space charge concentration vs. neutron fluence in p-type substrates from LFoundry

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RD50 submitted a pixel detector prototype ASIC in 150 nm CMOS technology at LFoundry. The chip contains passive pixel arrays near the edge of the chip suitable for E-TCT measurements. The chips were manufactured on p-type silicon with two different initial resistivities. Chips were irradiated with neutrons in the Triga reactor in Ljubljana to several fluences up to maximal fluence of 2e15 n/cm2. Evolution of effective space charge concentration with neutron fluence was measured with E-TCT for the two different initial resistivities. Acceptor removal parameters were estimated and compared with other measurements.

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