

Design of fast depleted CMOS pixels for particle detection within the CERN-RD50 collaboration

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The industrial standard High Voltage CMOS (HV-CMOS) technology is a promising candidate for future particle physics experiments. The CERN-RD50 collaboration develops depleted CMOS sensors to improve their features so that they meet the requirements of future particle physics experiments. In this work we propose the design of a new prototype chip based on LFoundry 0.15um technology, which focuses on minimising the leakage current, increasing the break down voltage and improving the pixel speed. The chip consists of several test structures and an 8 x 8 matrix of 60 um x 60 um pixels with analog readout. The aim of this matrix is to improve the processing speed of depleted CMOS sensors while keeping the noise low. Two flavours of pixels have been designed: the continuous pixel and switched pixel. With carefully designing the amplifier and minimising the parasitic capacitance, the continuous pixel can deal with a maximum particle rate of 20M events/sec and the switched pixel is able to deal with as high as 50M events/sec, when the equivalent noise charge (ENC) is kept less than 100 e⁻.

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