Results and perspectives from RD53 on the Next Generation Readout Chips for HL-LHC silicon pixel detector phase 2 upgrades

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On behalf of RD53 Collaboration

TREDI 2019 - Trento 25 Feb 2019

Outline

This talk will cover:

- Introduction
- RD53 evolution towards final chip
- Analog Front End : results / performance

This talk will not cover:

- Test beam results (more talk during the conference)
- Detailed radiation hardness results
- Details of Serial Powering testing of RD53A &/or system aspects

*Many results shown here rely on the work done by several people in RD53 but a **special thanks** goes to young students, that are working with lot of enthusiasm and energy: you will find their names along the presentation when referring to their work !*

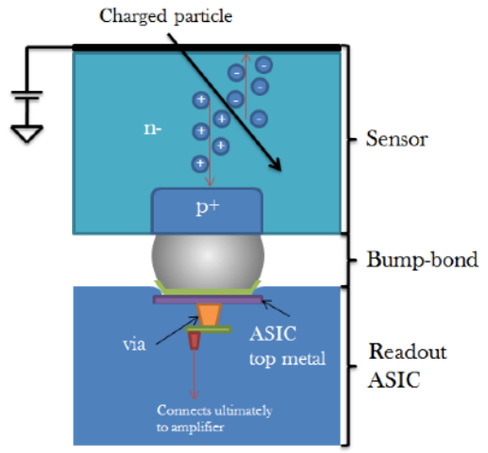
Pixel Detector at HL_LHC

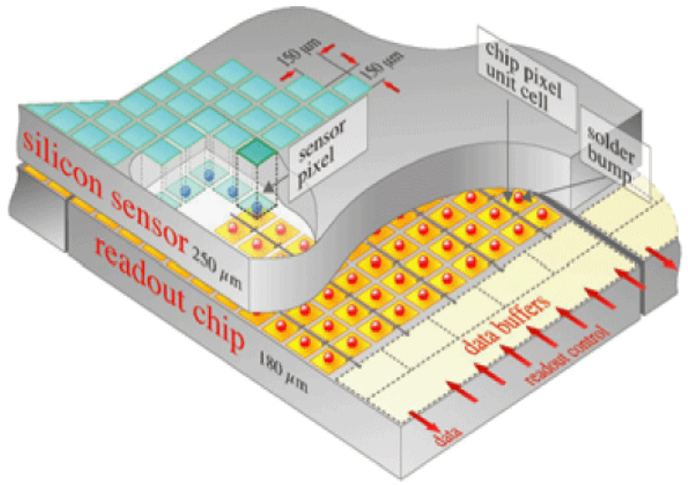
Requirements from HL_LHC experiments

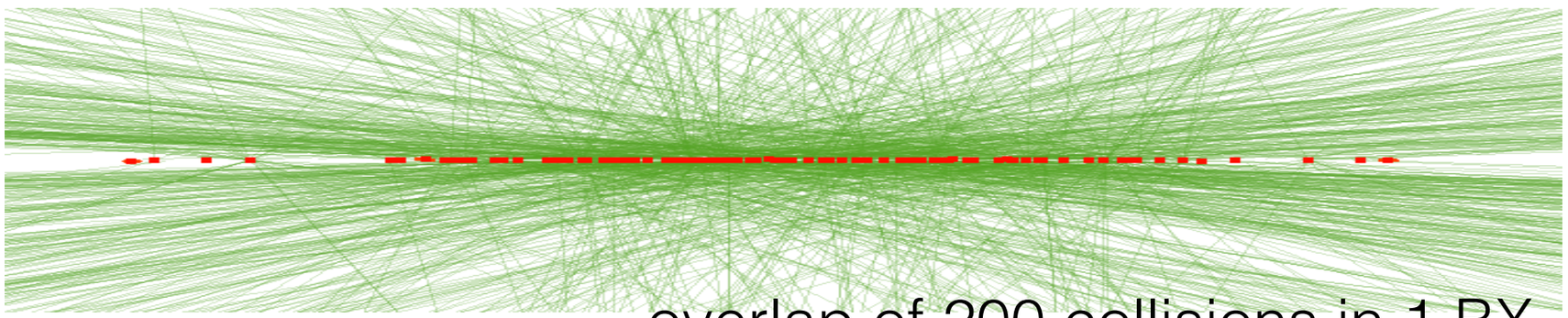
Small pixels: 50x50um$^{2.}$
Large chips : 2cm x 2cm (~0.5 billion transistors)
Pixel Hit rates: up to 3 GHz/cm^2 (200 P.U.)
Radiation : 1Grad, 10^{16} n/cm^2 (unprecedented)

Trigger: up to 1MHz with 12.8us latency
(~100x buffering and readout)
Low power - Low mass systems

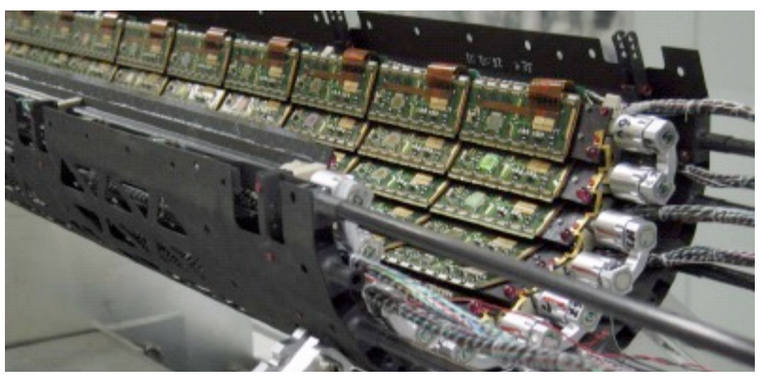
Data readout : up to 4-8 Gbs/s
TRIGGER Latency up to 12.8us (x3) ==> deeper storage buffer







overlap of 200 collisions in 1 BX



RD53 timeline

A. Development of Building blocks: IP-Block; Analog Very Front Ends

B. Development of Digital Architecture

C. Verification environment

D. Complex Chip Integration : modern tools to secure a successful ASIC submission

E. Radiation characterization: try mitigation strategy

Small DEMONSTRATORs : 64x64 pixel matrix
- FE65P2
- CHIPIX65-FE0

RD53A large scale prototype
400x192 pixel matrix

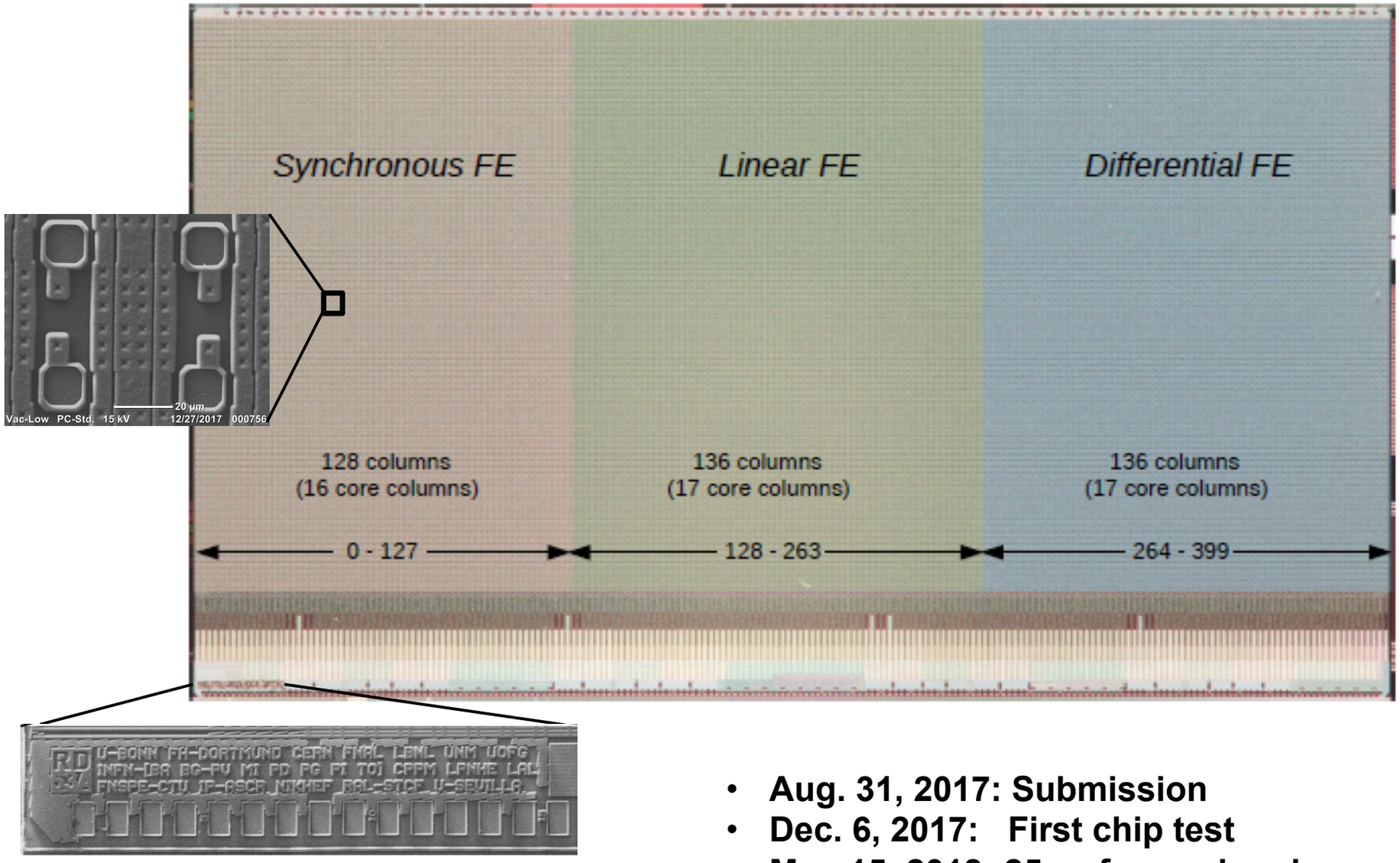
RD53B
~400x400 pixel matrix

ATLAS pixel chip

CMS pixel chip

2013 2014 2015 2016 2017 2018 2019 Time

RD53A



- **Aug. 31, 2017: Submission**
- **Dec. 6, 2017: First chip test**
- **Mar. 15, 2018: 25 wafers ordered**
- **Apr. 13, 2018: First bump-bonded chip test**
- **Aug. 1, 2018: Other 25 wafers ordered**

RD53A core design team

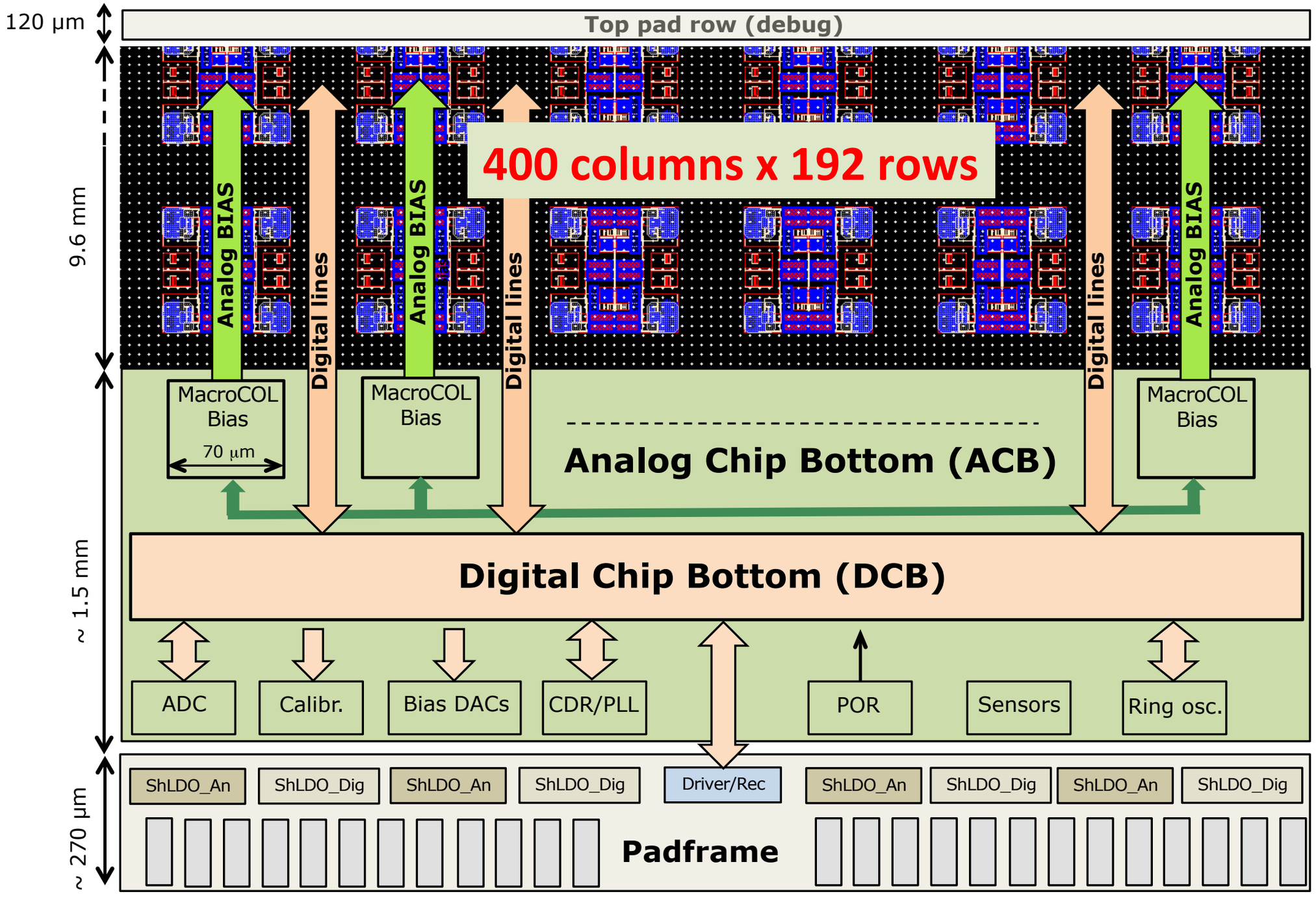
Flavio Loddo (Bari)
Tomasz Hemperek (Bonn)
Roberto Beccherle (INFN PI)
Elia Conti (CERN)
Francesco Crescioli (Paris)
Francesco De Canio (INFN BG-PV)
Leyre Flores (Glasgow)
Luigi Gaioni (INFN BG-PV)
Dario Gnani (LBNL)
Hans Krueger (Bonn)
Sara Marconi (CERN / INFN PG)
Mohsine Menouni (CPPM)
Sandeep Miryala (FNAL)
Ennio Monteil (INFN TO)
Luca Pacher (INFN TO)
Andrea Paternò (INFN TO)

2 x 1,15 cm²

~200M transistors

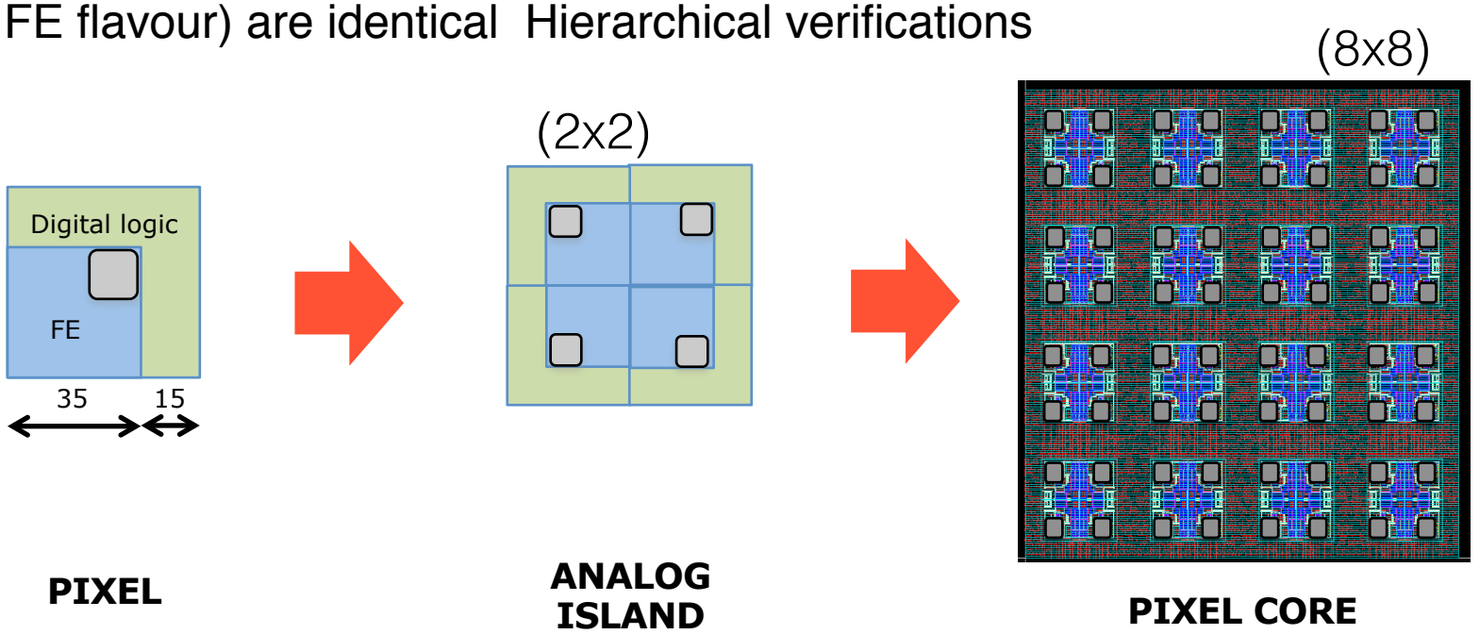
Chip doc on CDS: http://cds.cern.ch/record/2287593

RD53A Functional floorplan



Pixel Matrix

- The pixel matrix is built up of **8 x 8 Pixel Cores**
  - **16 analog islands (2x2 quads)** embedded in a flat digital synthesized sea
  - 50% of area to Analog, 50% to digital
- A Pixel Core can be simulated at transistor level with analog simulator
- All Cores (for each FE flavour) are identical Hierarchical verifications



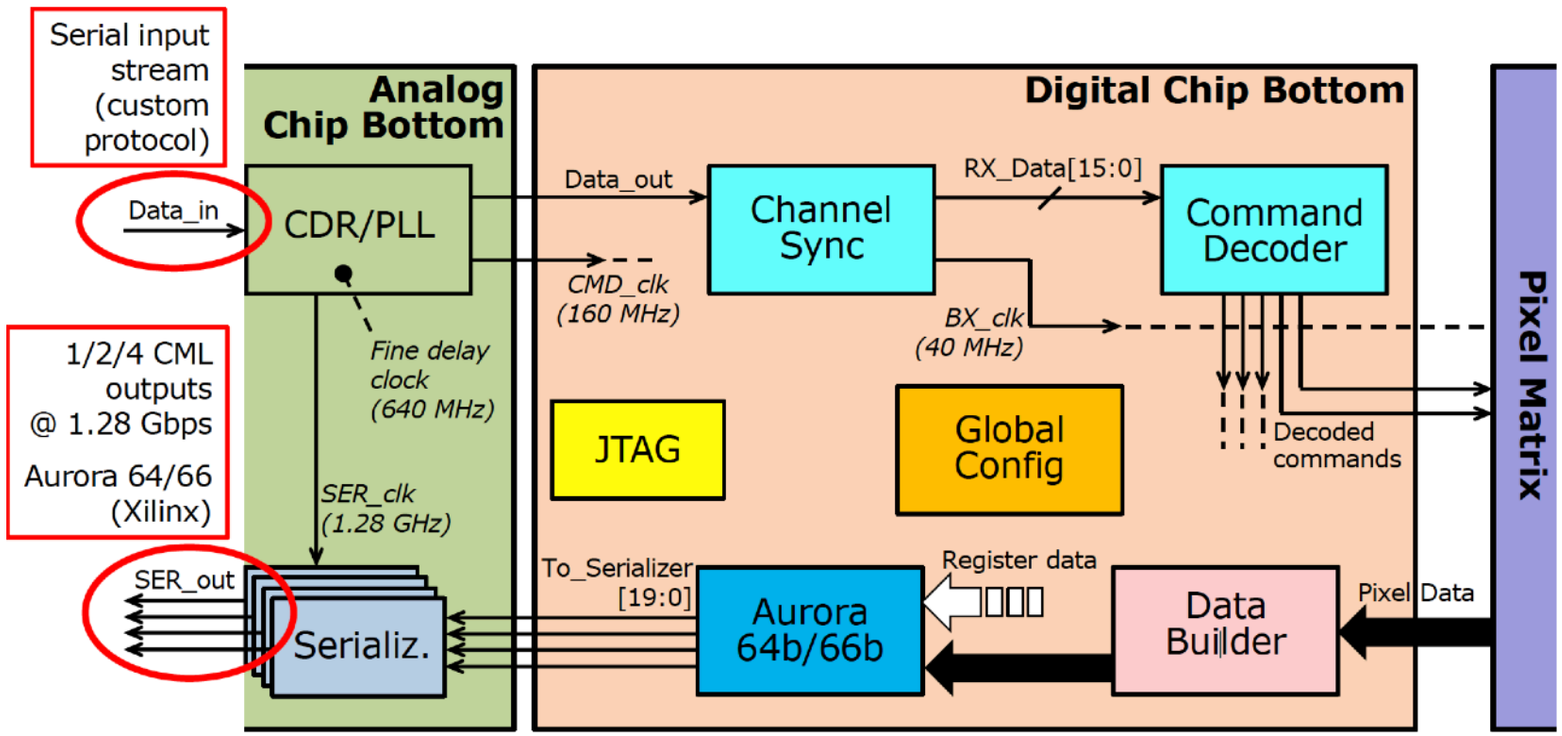
- All the digital logic for signal digitisation, storage, trigger-matching and readout is shared among several pixel, called Pixel Regions. **Two different Pixel region architectures** have been implemented

Distributed Buffering architecture (DBA)
- with (1x4) regions and distributed ToT storage
- implemented for two Analog FE (Lin, Diff)

Centralized Buffering architecture (CBA)
- with (4x8) regions and centralised ToT storage
- implemented for one Analog FE (Sync)

both allow to run at high rate (3 GHz/cm2), high trigger rate (1MHz) long latencies (12.8 us) with <1% inefficiency

Digital Bottom and I/O



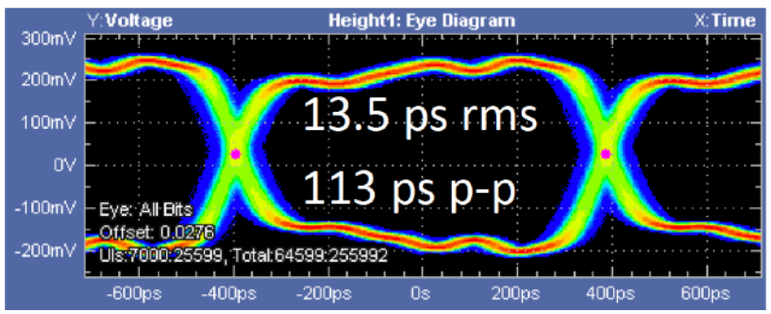
- CDR/PLL: single input: commands, clock, trigger@160 MHz
- serial output with 4-lines, each@1,28 Gbs, using Aurora 64b/66b protocol

ALL works fine, chip works also after irradiation (500 Mrad) results

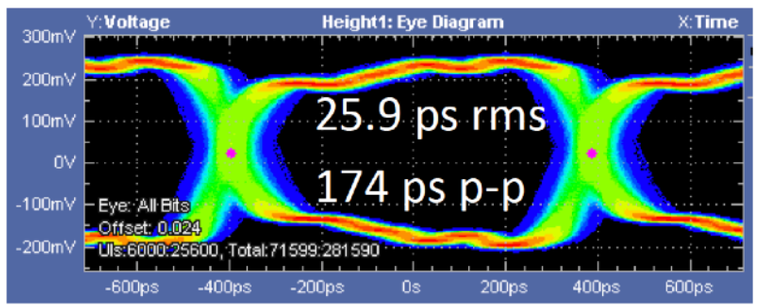
Issue / Improvements discovered:

- CDR/PLL full reliability is fundamental. Lock stability needs further improvement for larger range of input voltage, temperature and after irradiation.
- For Output the PLL clock is influenced by chip activity. Problem understood and proved
- new prototype submitted in August

No CLK to matrix, all columns off



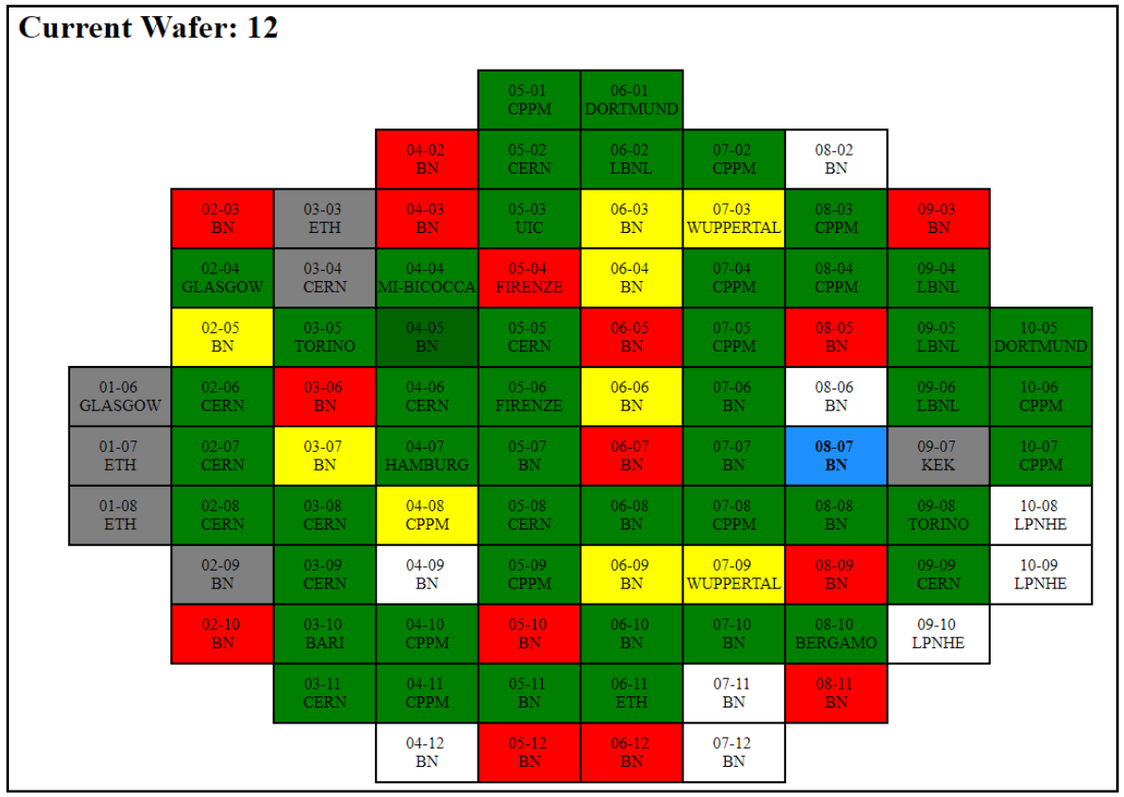
CLK send to matrix, all columns on



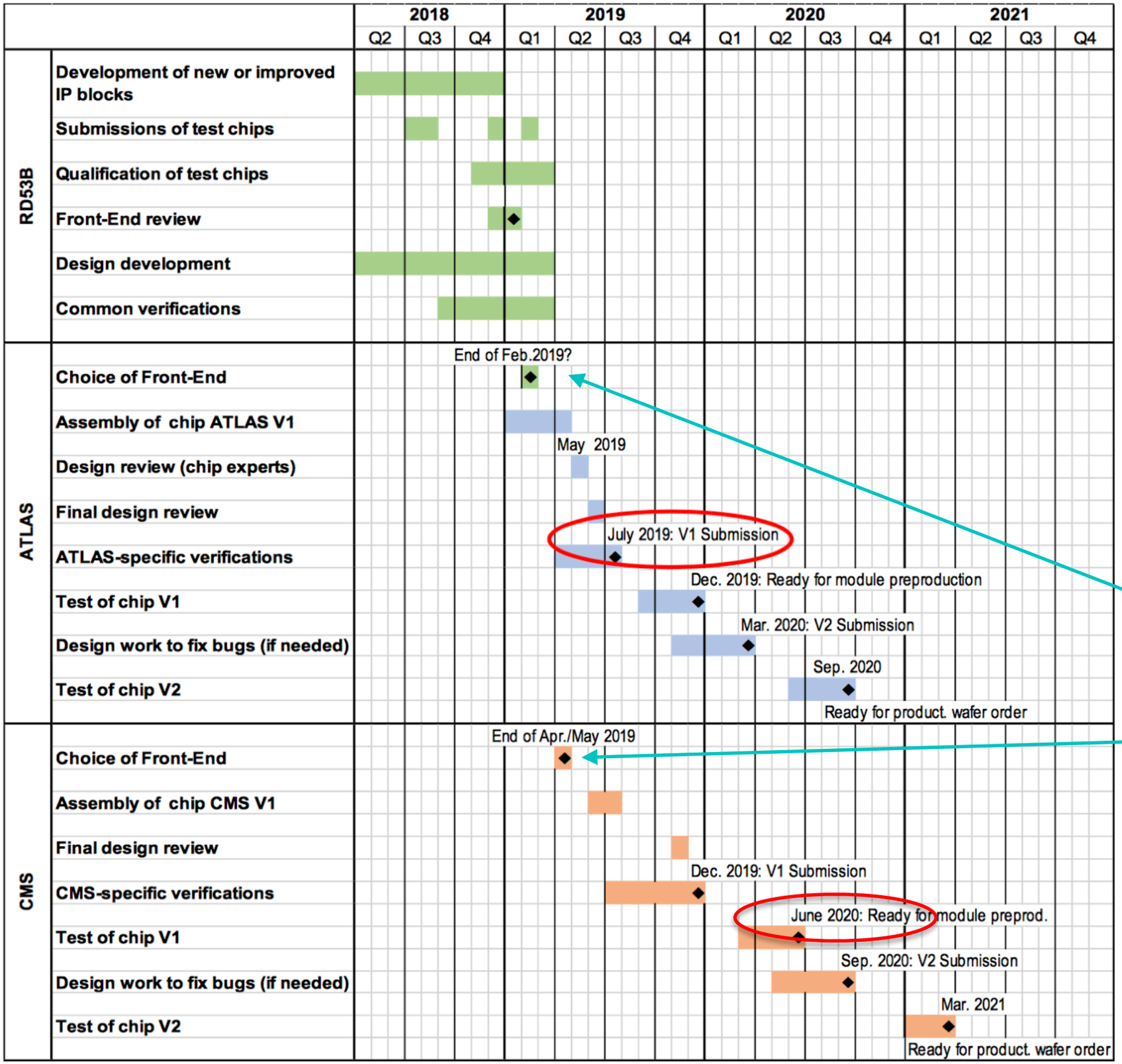
Testing and use of RD53A

- Two test systems : BDAQ53 and YARR
- More than 300 chips distributed among >30 institutes for chip characterisation
- 150 of them are bump bonded to sensors
- In April first test beam, mainly to understand RD53A
- Test beams for Sensor RD started with RD53A
  - May-August with un-irradiated detectors
  - In autumn first test of irradiated detectors
  - 2019 : further. test-beams (Desy/FNAL…)
- Wafer level testing at Bonn - soon other 2-3 centres
- Experiments started intense system-tests with serial powering chains of (1x2) or (2x2) modules

- Good
- Bad
- Partially working
- Visual problem
- Discarded
- Untested



Strategy and timeline



One common design: RD53B with common design team - mainly based on RD53A design team: ~ 30 designers (13 FTE)

Two submissions with different matrix size: **ATLAS** chip first, then **CMS** chip

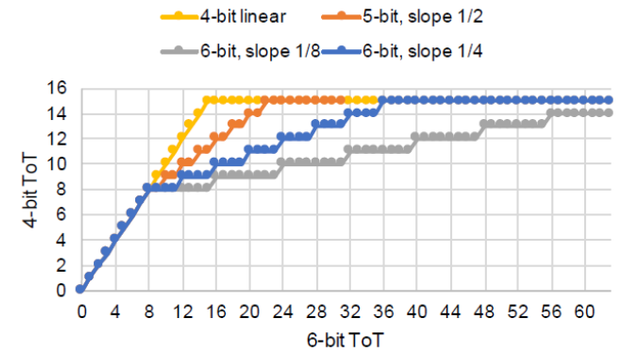
unique architecture - no difference in chip bottom or Core design- matrix size is a parameter in the design specifying the number of Cores in x & y .

Independent choice of Analog FE

RD53A to RD53B

- All RD53A elements with bug fixes and, where needed, technical improvements
- Improved versions of some IPs

- **Additional feature to be implemented:**
  - Bias of edge and top “long” pixels
  - 6-to-4 bit dual slope ToT mapping
  - 80 MHz ToT counting
  - ATLAS 2-level trigger scheme
  - TMR for SEU hardening
  - Power saving ~20%
  - Design for test scan chains
  - Optimal data formatting and compression
  - Date aggregation between pixel chips (CMS requirement now also ATLAS interested)
  - …



Analog FE

- **small Analog FE** : ~ 50% of the 50x50 um2 area
- **high efficiency** : <1% dead-time, low threshold
- **low power** : reference is 5uA per pixel
- **charge measurement** (~1ke- /count) - 4-bit
- **low level of fake rate** : <1E-6 per chip
- **applied to sensor choice and radiation conditions** : reference 50fF detector, 10nA; 500 Mrad

<u>Specification on analog FE have been evolving with time</u>

- Initial RD53A requirements
- Important feedback from Analog FE Review
- Now moving to ATLAS requirements and CMS requirements

<u>Take in mind that</u>

- Essential to understand the impact of AFE performances to the CMS/ATLAS pixel detectors : simulation work essential
- The sensor R&D is heavily dependent on RD53A : no sensor choice done yet

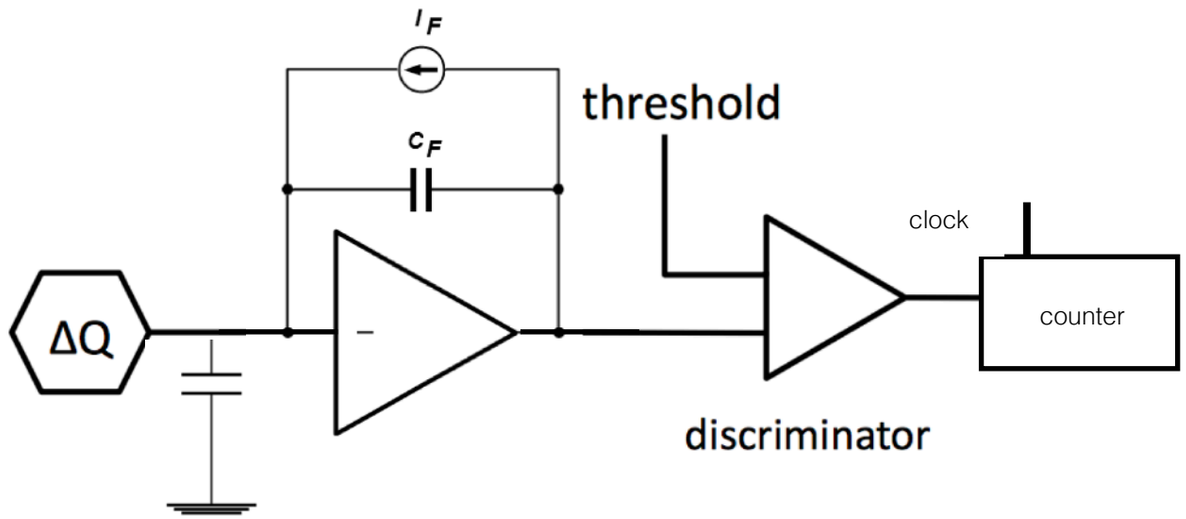
Analog FE review

General Comments

- The present document and the recommendation presented here is strictly based on the measurement results that have been presented during the reviewer meetings (4th-5th December 2018 and 24th January 2019).
- The reviewers believe that, although many measurements have been done on the front-end designs, still more measurements (and interaction between the measurement teams and the design teams) would be required to better understand the effects that are observed on the three front-ends discussed. In particular, the review committee would like to encourage the measurement teams to increase the statistics of analysed chips and assemblies in order to validate the conclusions presented in this document.
- It is also the belief of the reviewers that the circuit simulation tools in their present state are able to simulate any effect that is observed in fabricated circuits (except radiation effects in the electronics and process-fabrication stress effects). For this reason, the reviewers would like to encourage the measurement teams to work closely with the designers to understand and reproduce on simulations the different effects that are or might be observed.

Analog FE : basics

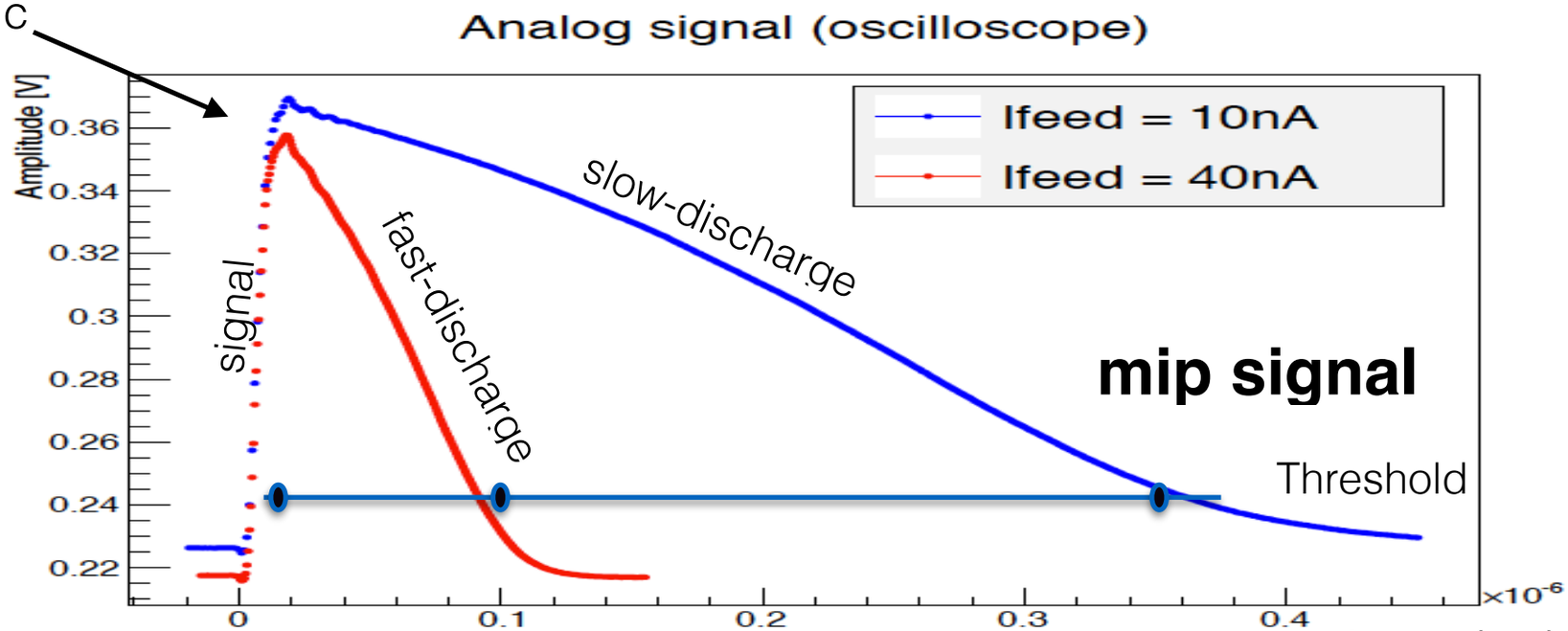
1. Signal charges fast Feedback Capacitance (Cf) ;
2. A stable current discharges Cf, making the signal duration linearly dependent wrt charge;
3. Discriminator determines when the signal is above threshold : **Time over Threshold**
4. a clocked counter counts the ToT



	Input	Ileak to sensor	Feedback-current	Discriminator	Threshold pixel tuning	ToT-count clock
Linear FE	single ended	Krummenacher		Asynchronous	4-bit trimming DAC	40 MHz chip clock
Diff FE	differential	LCC circuit	IFF	Asynchronous	5-bit trimming DAQ	40 MHz chip clock
Synch FE	single ended	Krummenacher		Synchronous with BX	Autozero Pulse 200ns@abort gap	20-400 MHz local clock

Analog FE

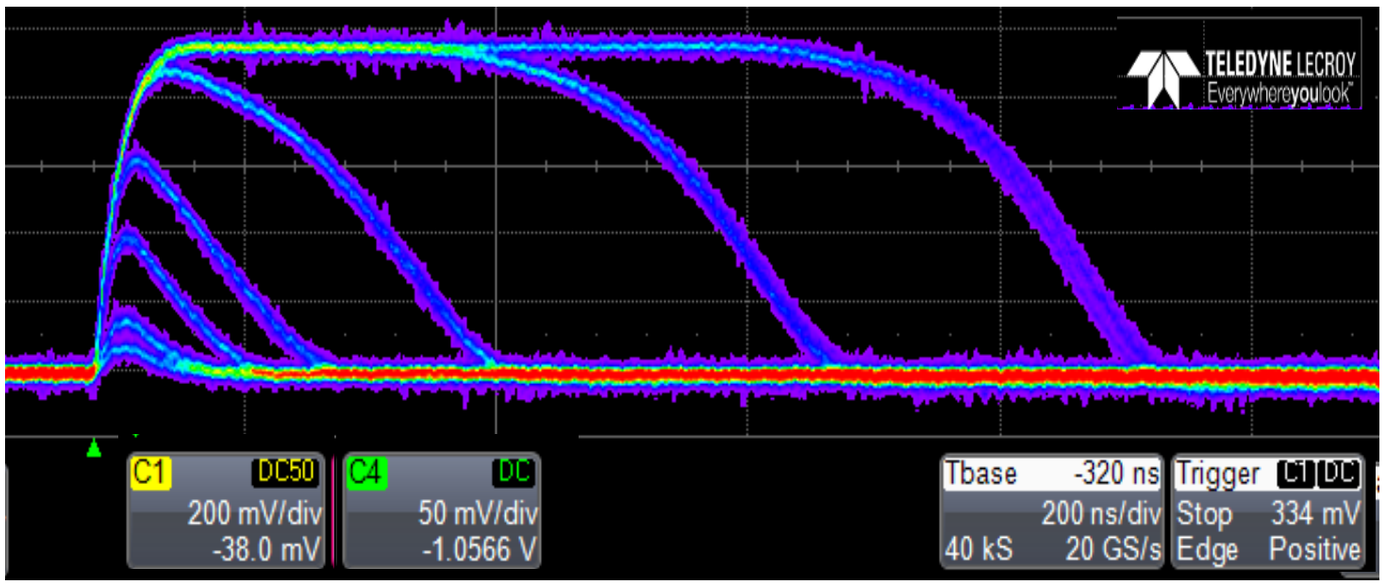
NB: Balistic deficit



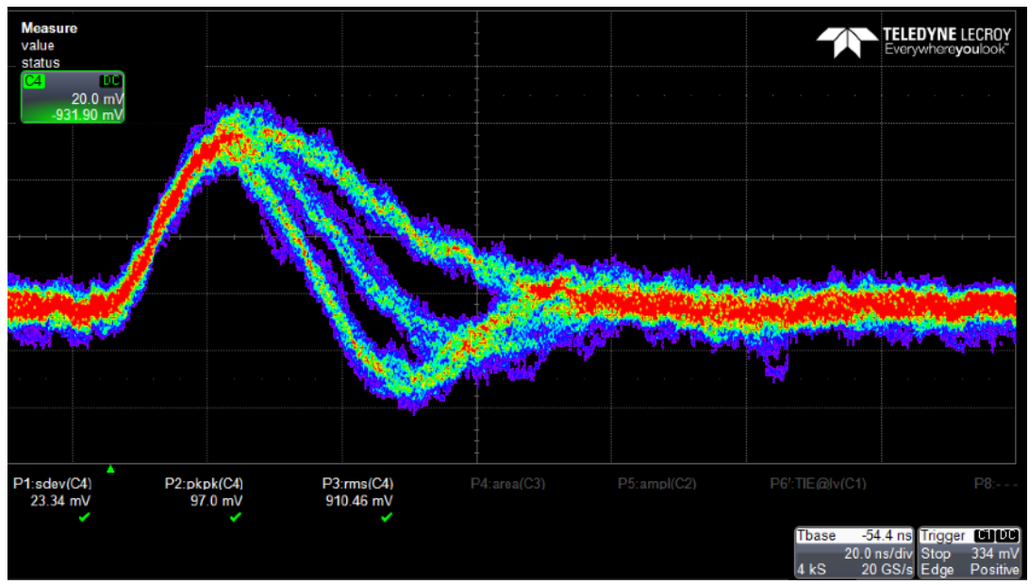
Example:

ToT$_{fast}$ ~85ns

ToT$_{slow}$ ~330ns



CSA output for
Q=30, 20, 10, 5, 3, 1.2, 0.6 ke-

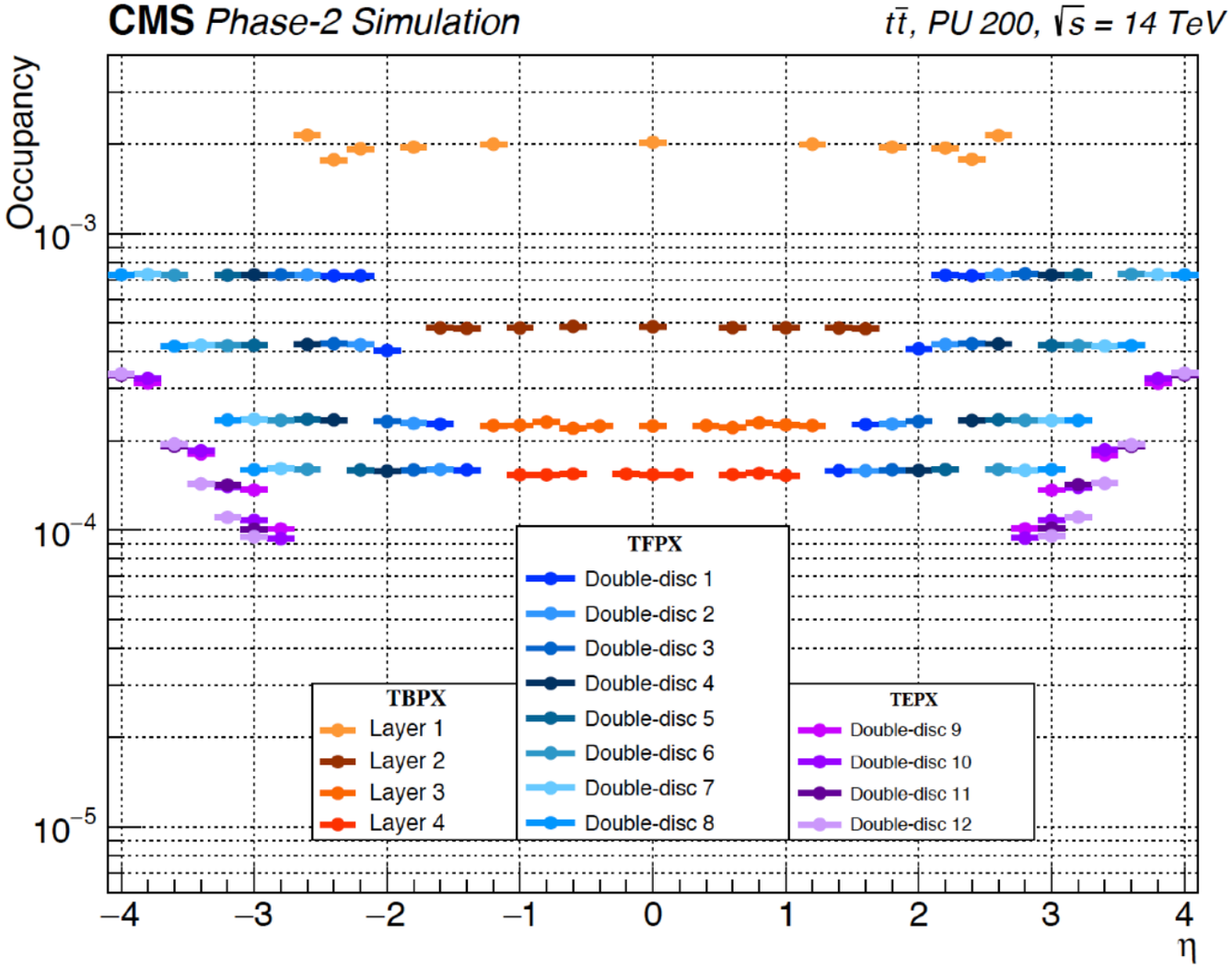


Q-1,2ke- for different return to base line (IK=55,100,155)

Analog FE :dead-time & fakes

TOT is analog dead-time, therefore is has to be kept small is order to determine a negligible inefficiency.

Fake hits have to be kept negligible wrt signal



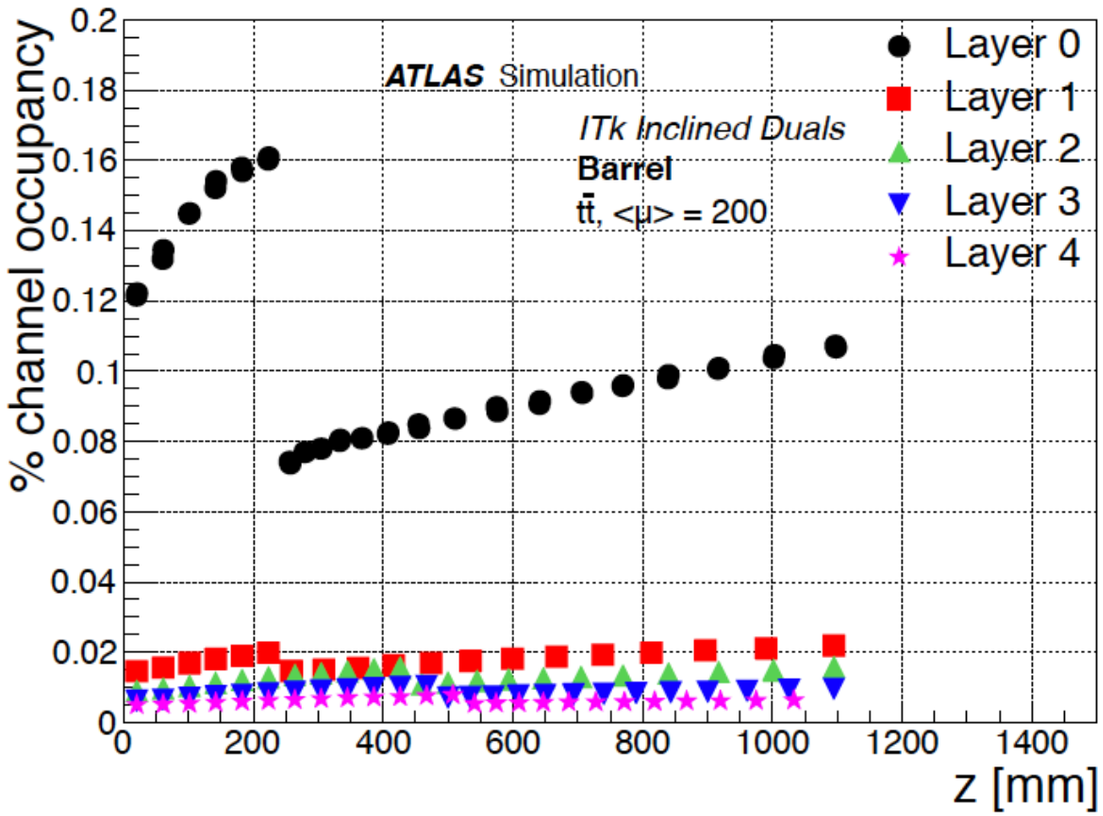
	Occ	AFE ineff	mip ToT	Fake/ Occ	Fake
L1	2E-03	0,5 %	62ns	1 %	**2E-05**
L1	2E-03	**1 %**	**125ns**	1 %	**2E-05**
L2	8E-04	0.5 %	**156ns**	1 %	**8E-06**
L3	2E-04	0,2 %	**250ns**	1 %	**2E-06**
L4	1,5E-04	0,2 %	**330ns**	1 %	**1,5E-06**
lowest	1E-04	0,2 %	**500ns**	1 %	**1E-06**

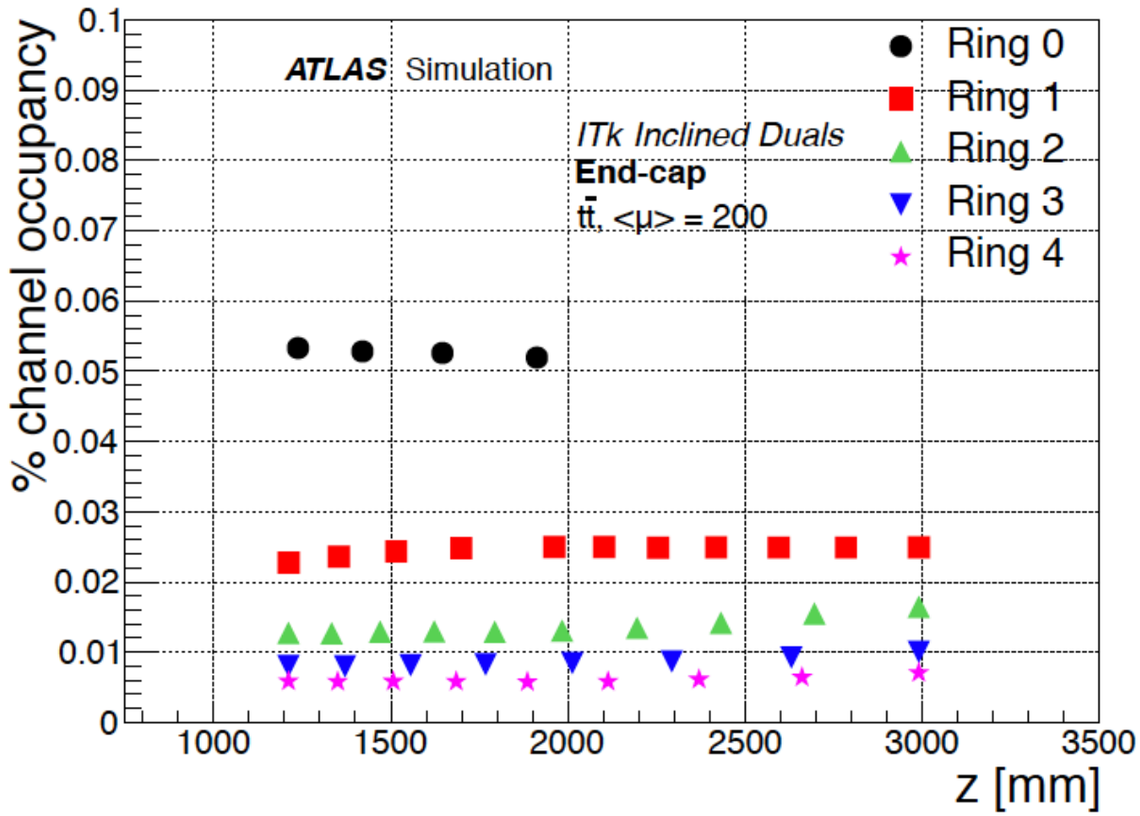
Value used by RD53
up to review

Analog FE :dead-time & fakes

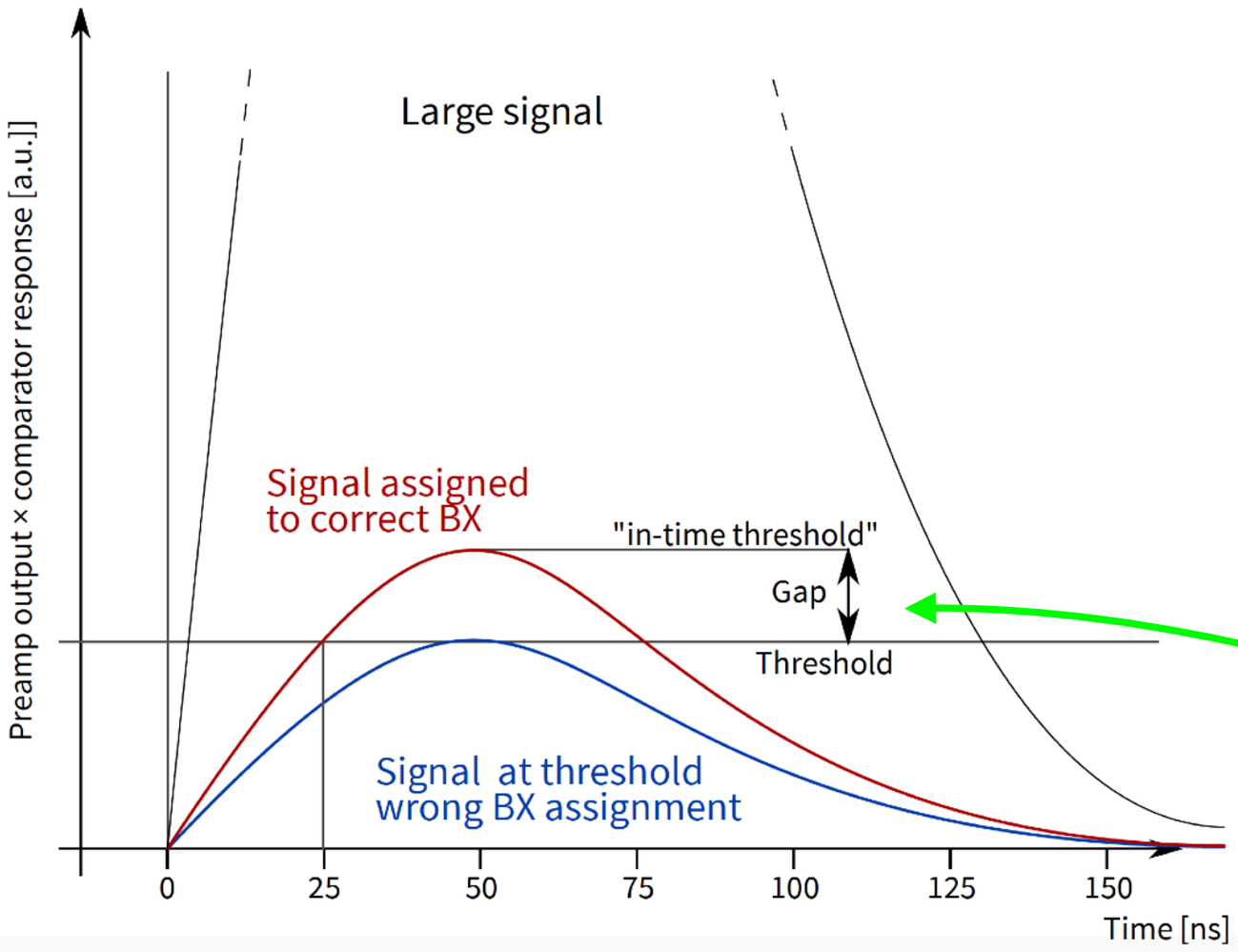
Atlas occupancies

https://cds.cern.ch/record/2285585/files/ATLAS-TDR-030.pdf





Analog FE :threshold(s)



Normally we tend to talk only about the **absolute threshold** that is the signal charge at which the discriminator has 50% to fire

LHC organised in 25ns BX bunches, therefore what matters is the i**n-time threshold,** i.e. the minimum signal that is detected in the right BX

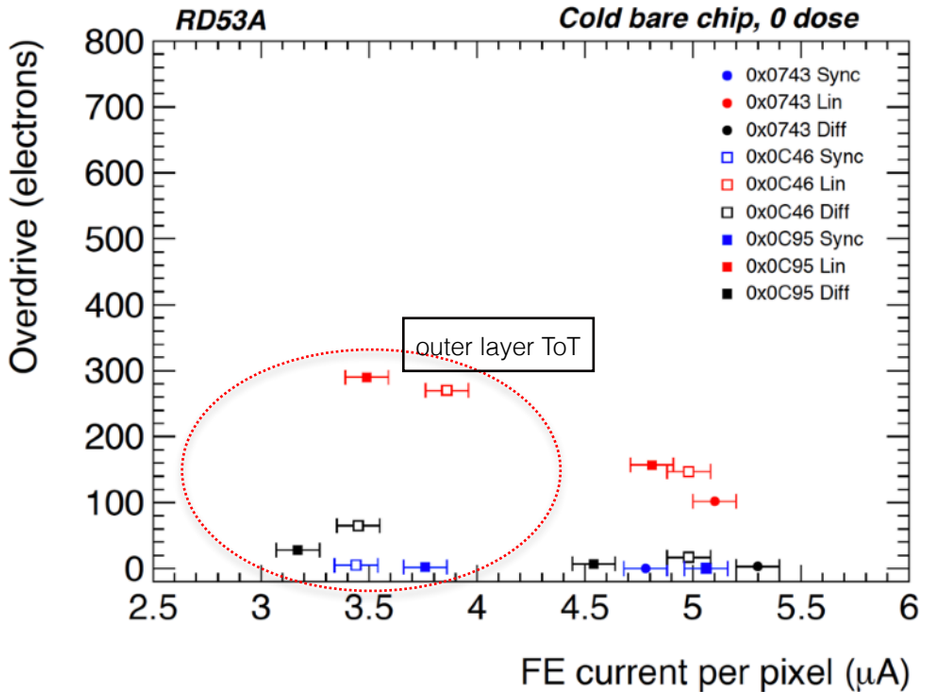
The difference between the absolute and the in-times thresholds is called **overdrive.**

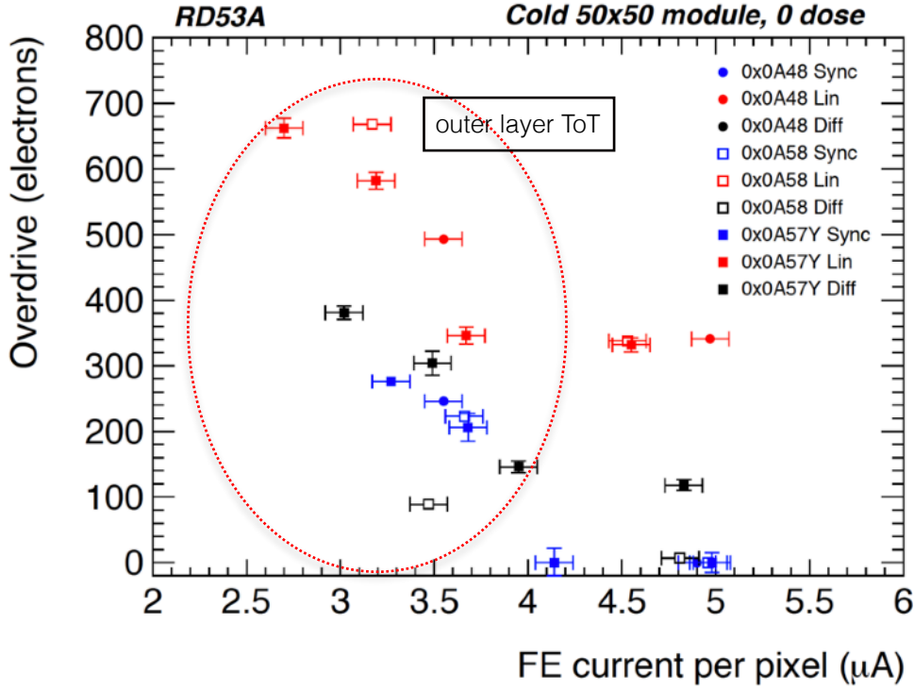
Signal in ‘gap’ are detected but assigned to the wrong BX

1. Only in-time threshold matters
2. Overdrive generate OOT pile-up: 50e- correspond ~1% OOT-pile up

Overdrive = 50e- in L1 = 2E-5 of hits that are ~Fake hits

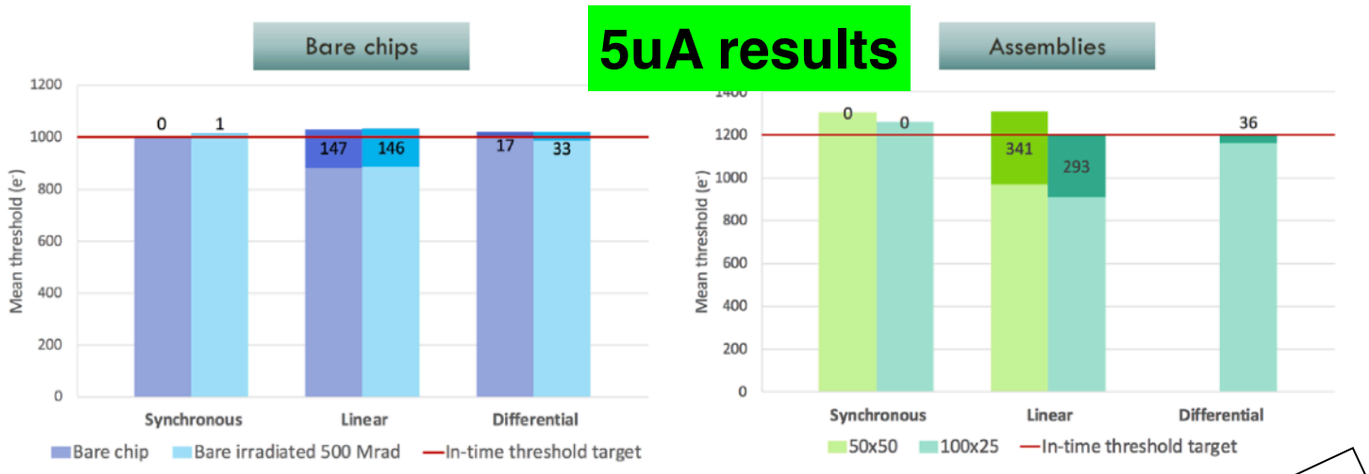
Analog FE :overdrive



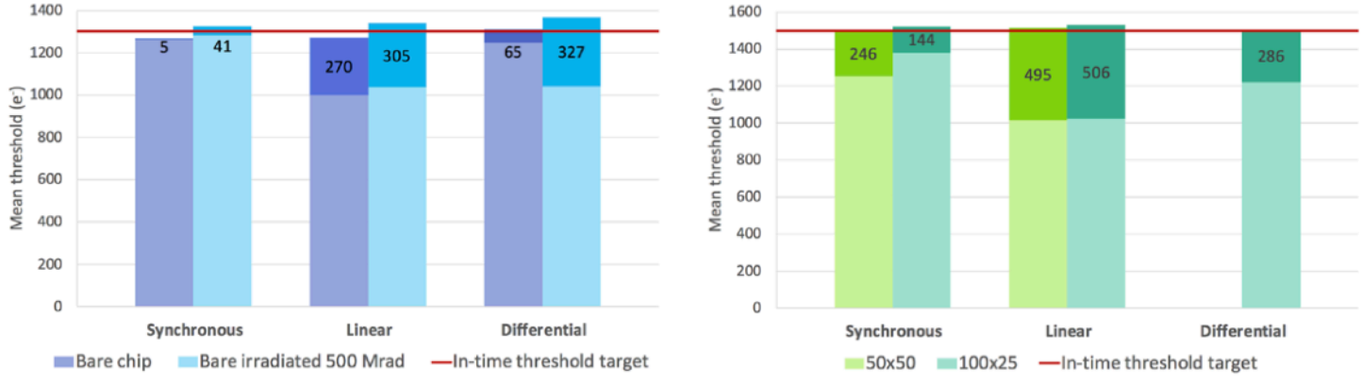


ALL this is with No irradiation

5uA results



3.5uA results



plots from N.Emriskova

Min. stable threshold setting	600 e⁻
Min. charge above threshold resulting in <25 ns time walk	600 e⁻
Min. in-time threshold with free-running front end	1200 e⁻

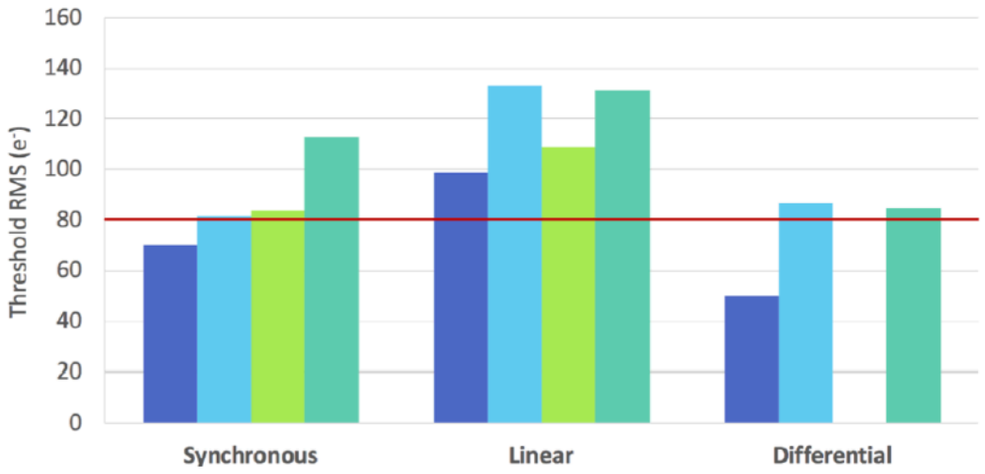
Specs for RD53A

all FEs satisfy this but it is far from being optimal !

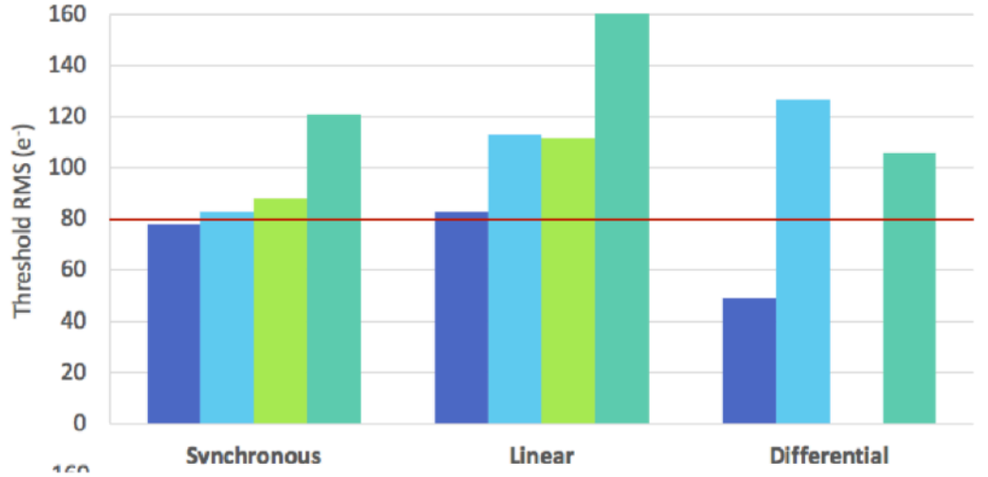
Analog FE :Threshold dispersion

Threshold

5 µA



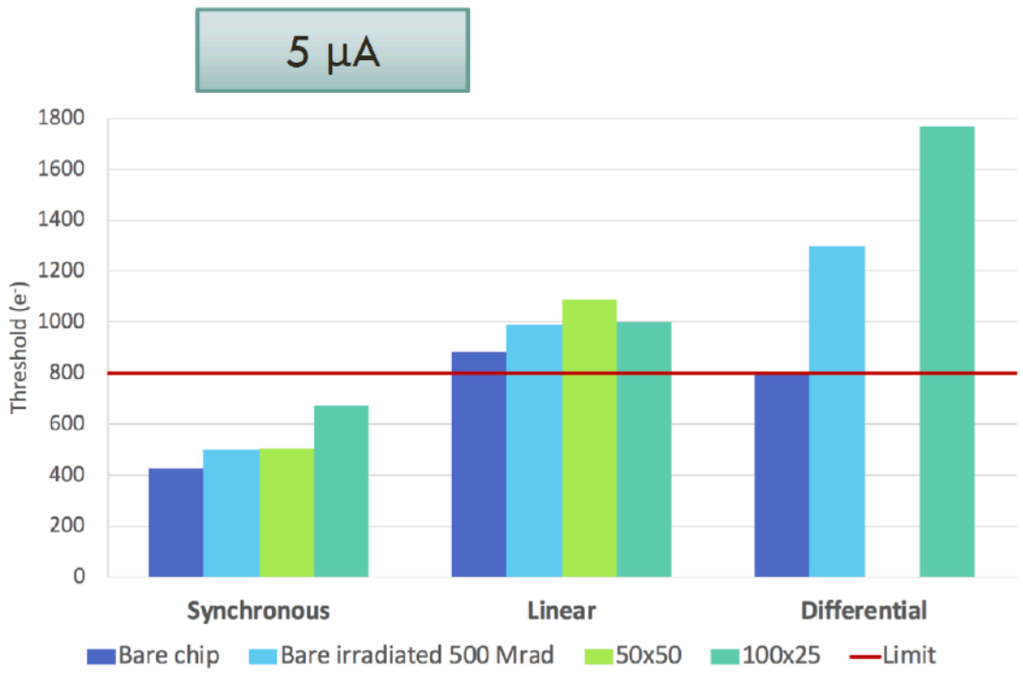
3.5 µA



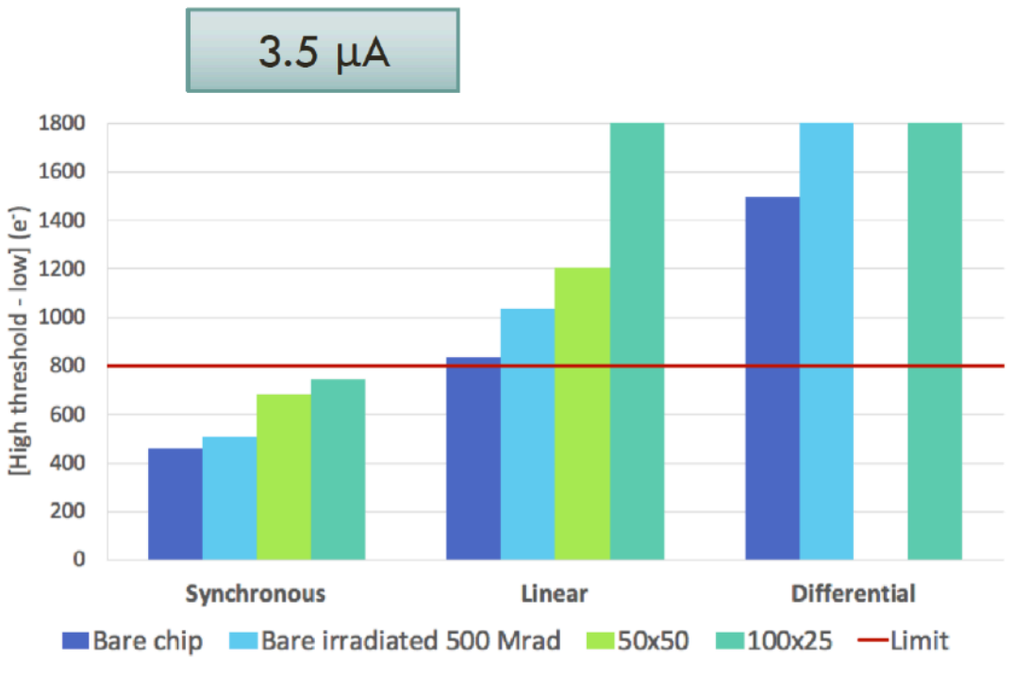
Difference between high and low in-time threshold containing 99.7% of pixels

In-time threshold

5 µA

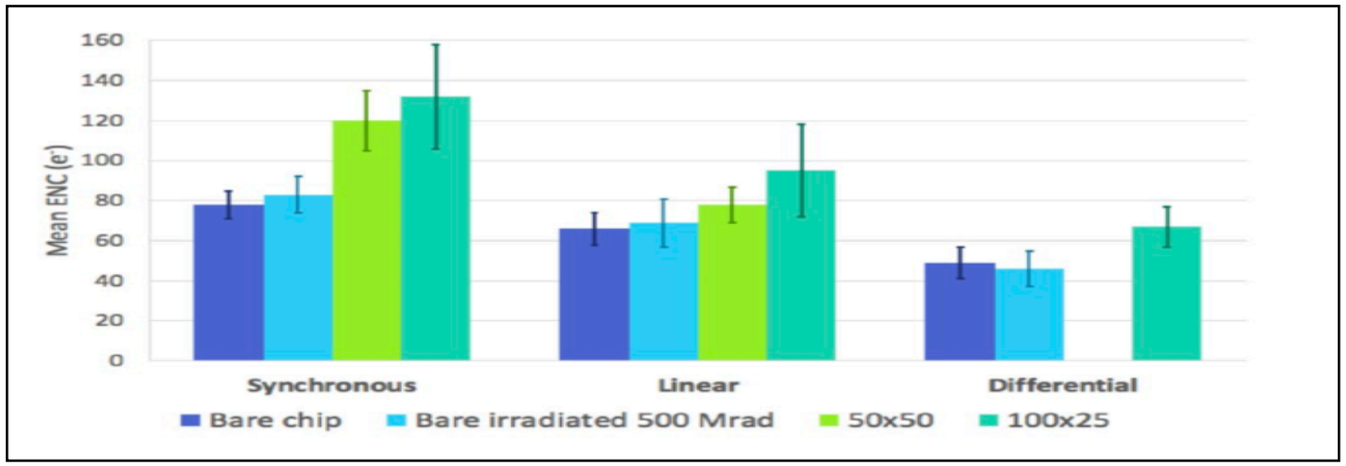


3.5 µA



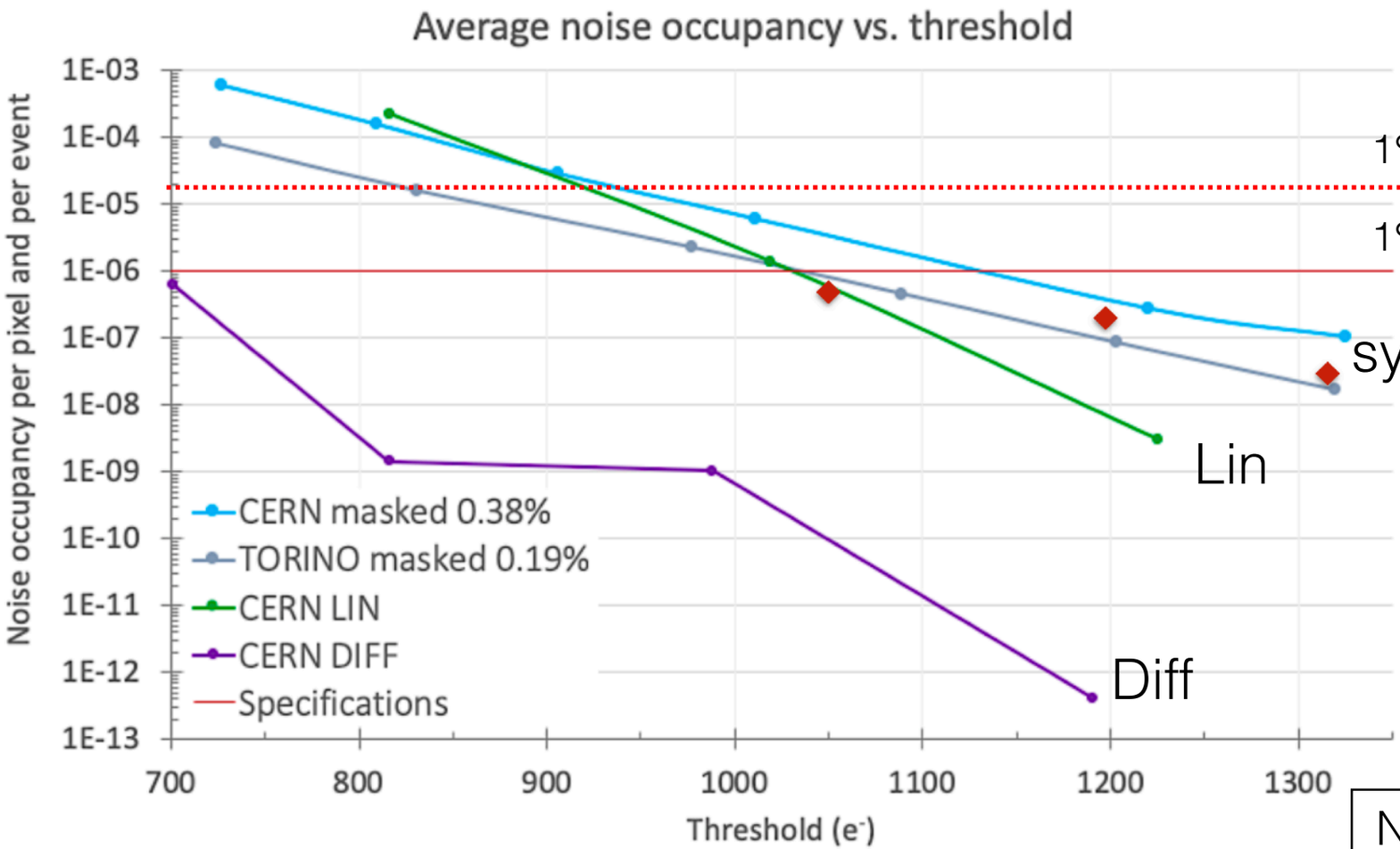
plots from N.Emriskova

Fakes from Analog FE



All this is for 25x100 um^2 sensor and
NO irradiation

NB: only 1-2 modules shown here !



1% L1 occ

1% L4 occ = 0,05% L1 occ

synch

Lin

Diff

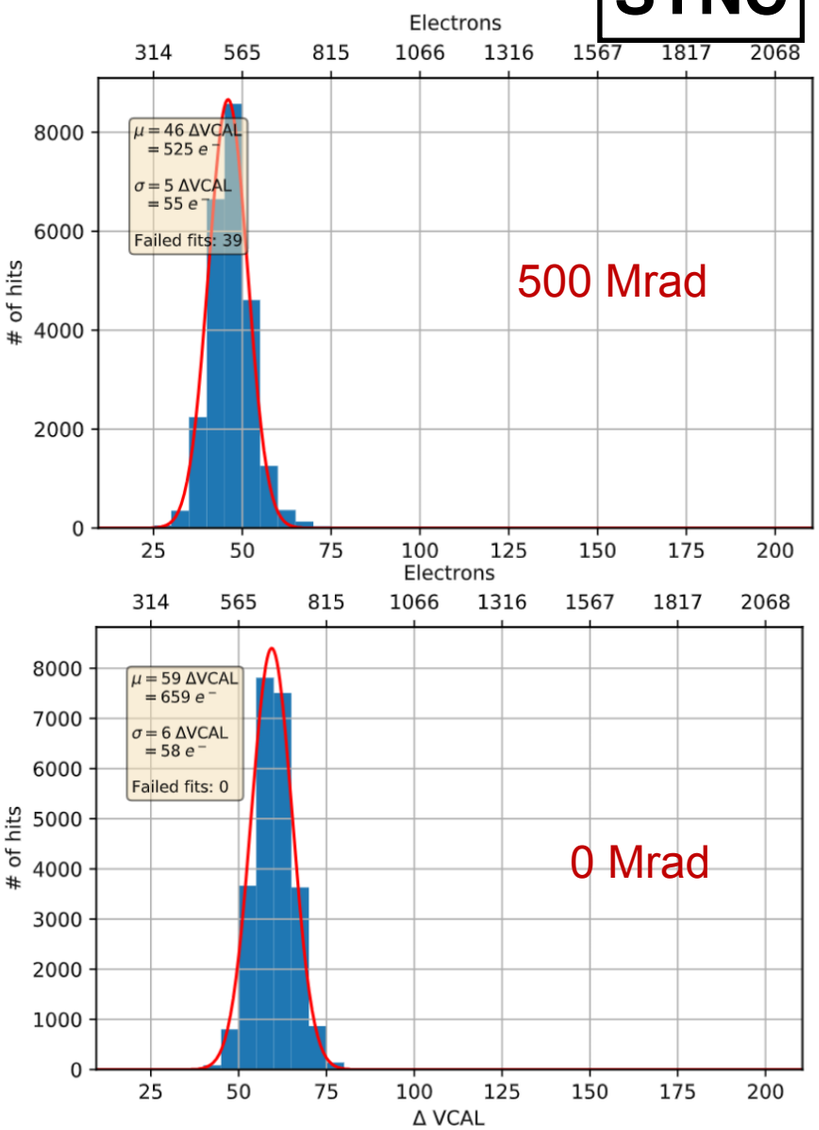
plots from N.Emriskova

NB: OOT-pile up ~1E-6/1E-5 (5-50e-)

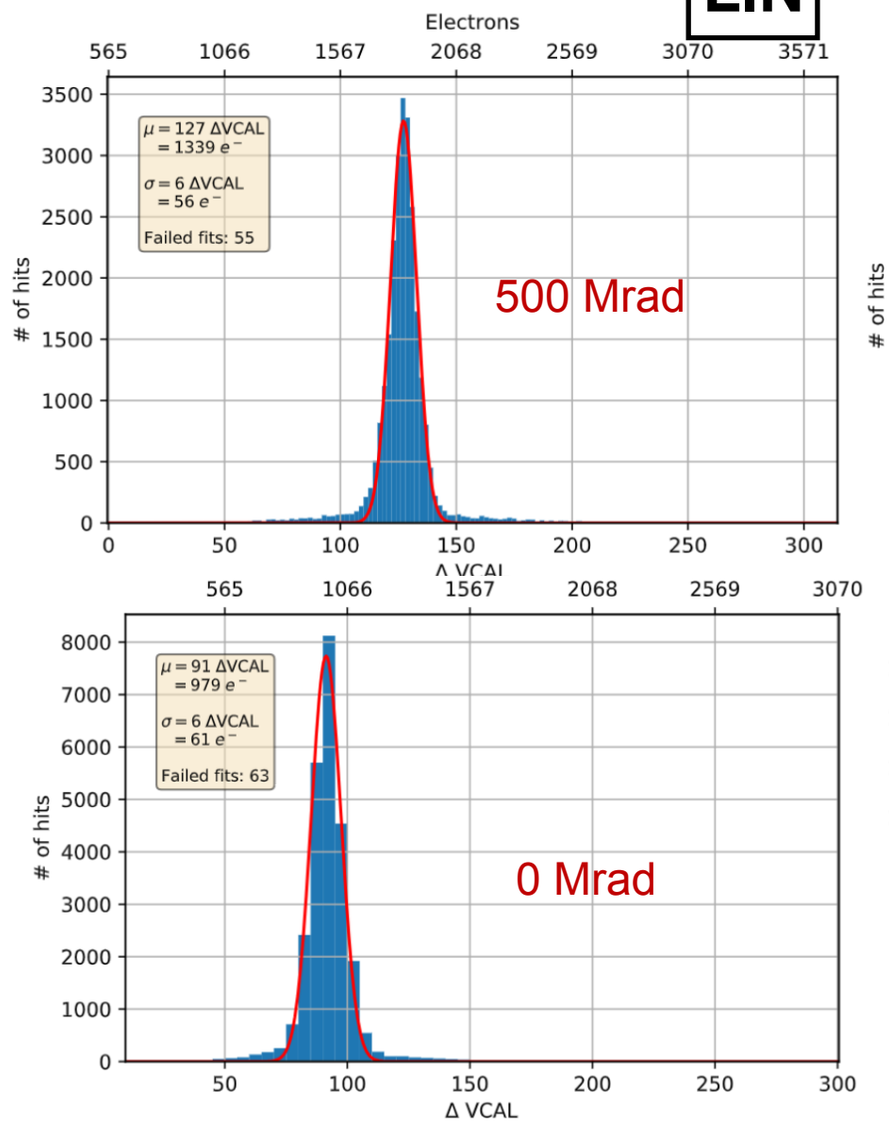
AFE Radiation hardness

Irradiation with x-ray@cold, RD53A powered on and tested/readout continuously
Striking good results - chip works, all three AFE work with low **thresholds** !

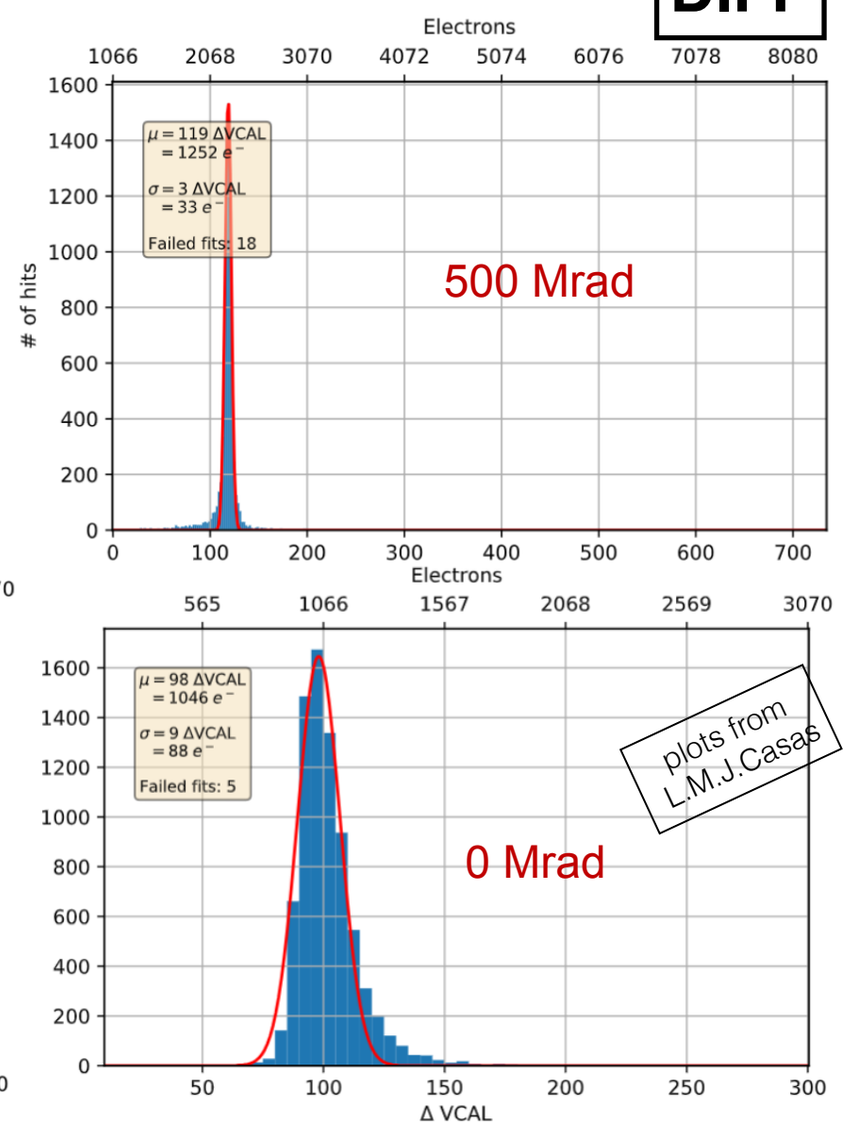
SYNC



LIN



DIFF



other irradiation results show the robustness of Analog FE

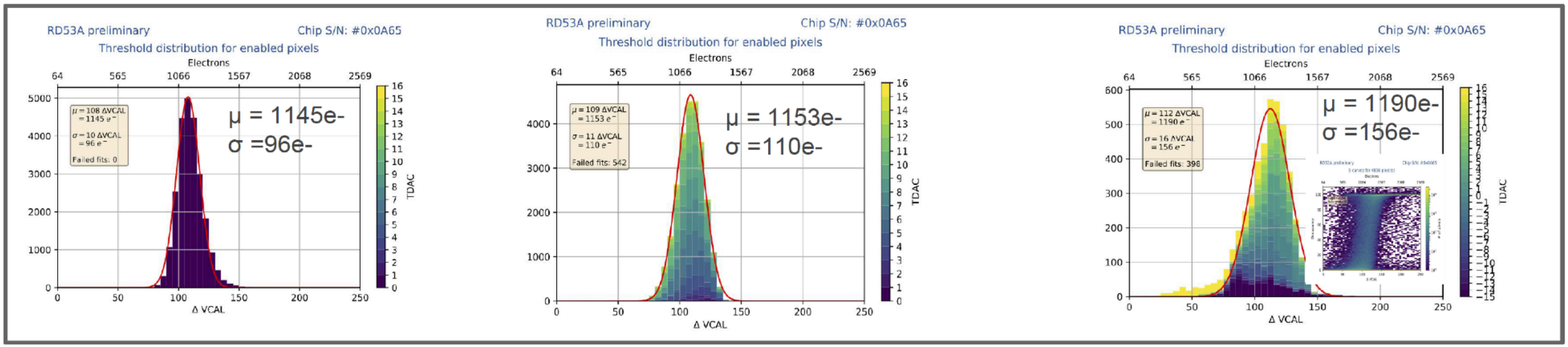
AFE vs Leakage current

Threshold Dispersion 10nA / per pixel

plots from M.I.Lezki

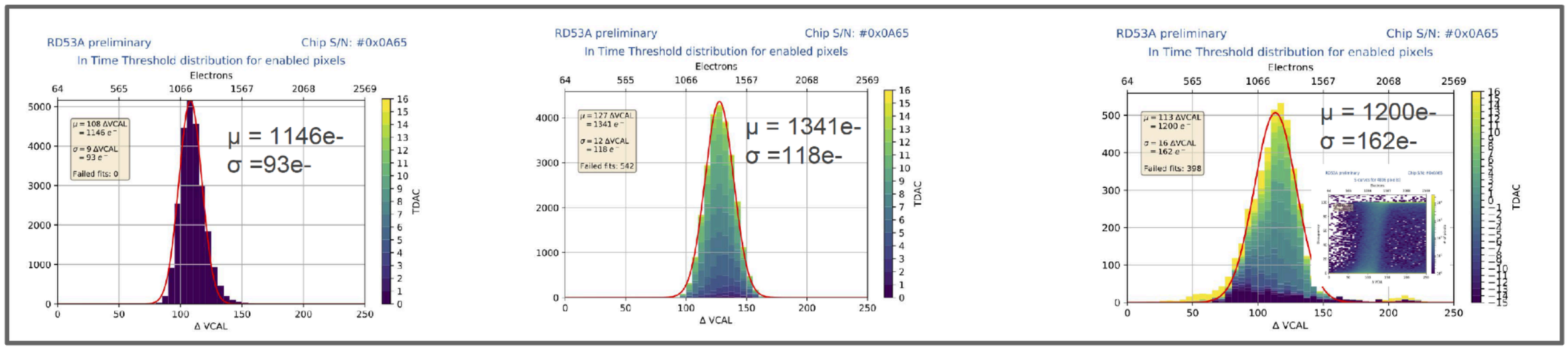
SYNC FE | **LIN FE** | **DIFF FE**

Threshold



Vth= 135, IBIAS_KRUM_SYNC=50 | Vth= 367, KRUM_CURR_LIN=26 | Vth1=113, Vth2=0, VFF= 64, LCC=400, PreCompDiff=512

In-time threshold

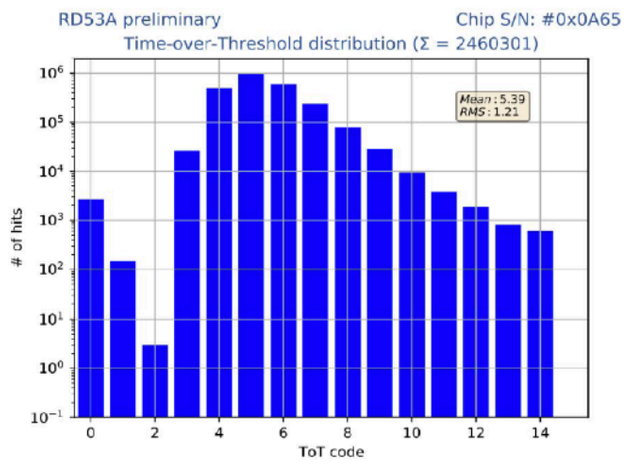


50×50 μm2(MPP W2-54GNA) no PT, 100 μm thickness - chip #0x0A65, irradiated fluence (neq/cm2) = 3.00E+15

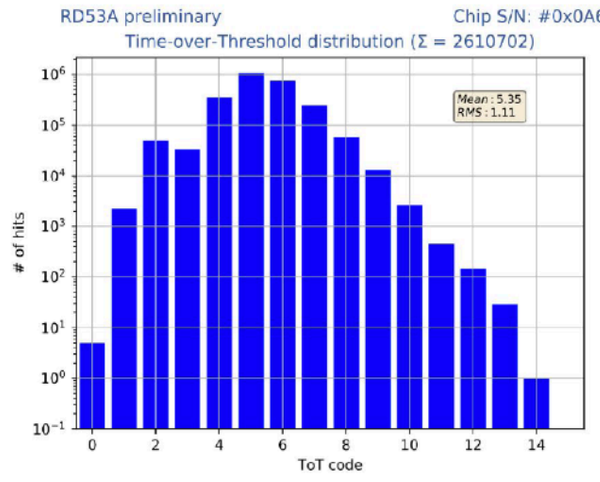
Analog FE:ToT for Q=6ke-

SYNC FE | **LIN FE** | **DIFF FE**

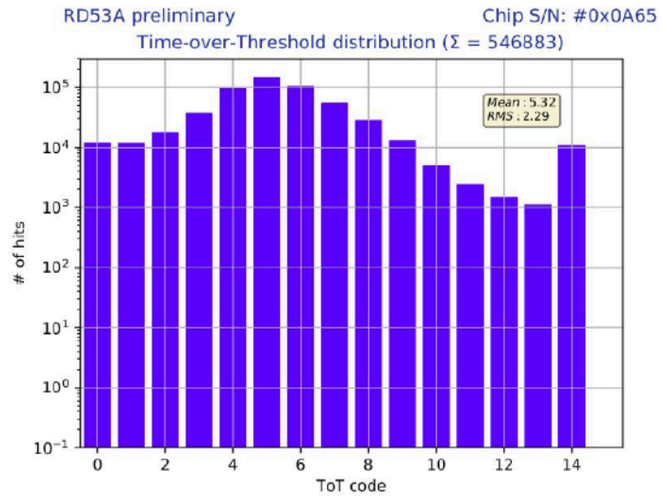
3 nA/per pixel



Mean ToT= 5.39, RMS= 1.21

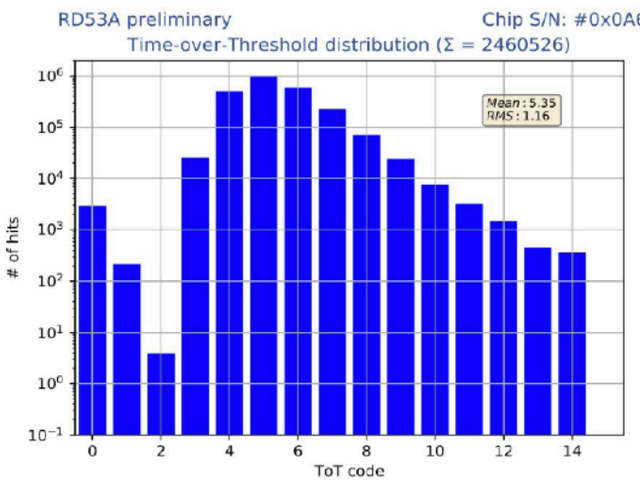


Mean ToT= 5.35, RMS= 1.11

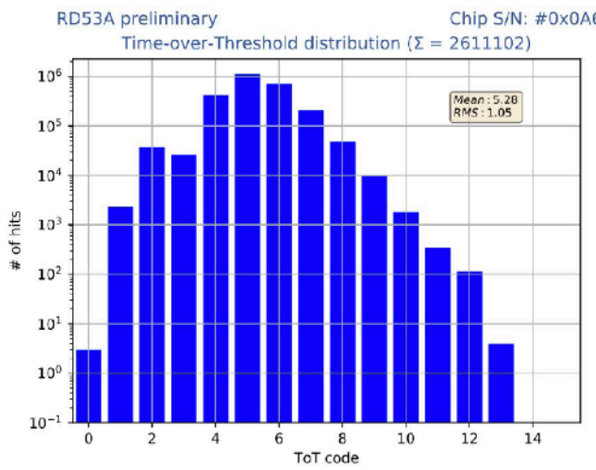


Mean ToT= 5.32, RMS= 2.29

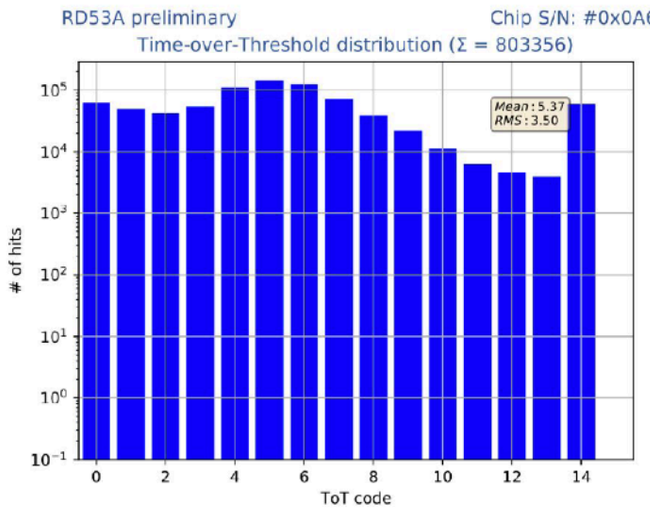
10 nA/per pixel



Mean ToT= 5.35, RMS= 1.16



Mean ToT= 5.28, RMS= 1.05



Mean ToT= 5.37, RMS= 3.50

plots from M.I.Lezki

AFE Summary

	ENC with assembly	Threshold dispersion	Overdrive @5uA 1200e-	Fake hits @thr=1200e-	ToT	ToT res (for 6ke=125ns)
Linear FE	80-115e-	.11-.13ke- rms; 1-1,1ke- perc.	~300e-	1,E-07	linear	500-1000e-
Diff FE	65-90e-	.08ke- rms; 1,25-1,7ke- perc.	0-40e-	1,E-12	not-linear	500-1000e-
Synch FE	120-130e-	.08-.11ke- rms; .5-.65ke- perc.	0	1-5E-7	linear	50-1000e-

ALL FE needs to be modified from RD53A version

Linear FE :

- non-linearity of TDAC fixed
- working to decrease overdrive

Synchronous FE

- improving AZ circuit (current spike, stability in time)
- working in improvement of ENC and matching with simulations

Differential

- defining solution to solve timing issues : Analog/Digital interface and speed of discriminator
- understanding operational stability at cold, high leakage current
- working to understand high irradiation

Analog FE review

Conclusions

- In this document we have presented measurement results showing that the three front-ends have shown strong points but also imperfections. Unfortunately and due to timing, the cause of some of the imperfections are to this date not understood. Based on the technical facts exposed in this document, the review committee believes that the Linear Front End is the design that presents a lower risk in its integration into a full scale chip. The reviewers recommend the designers to follow the recommendations that have been exposed in this document and to study the performance of the comparator for its optimization (with minor modifications).
- The reviewers would like to encourage the other teams to continue investigating the limitations on their front-ends.

Basically : continue to work but in urgent need the lowest risk on chip integration is the Linear FE

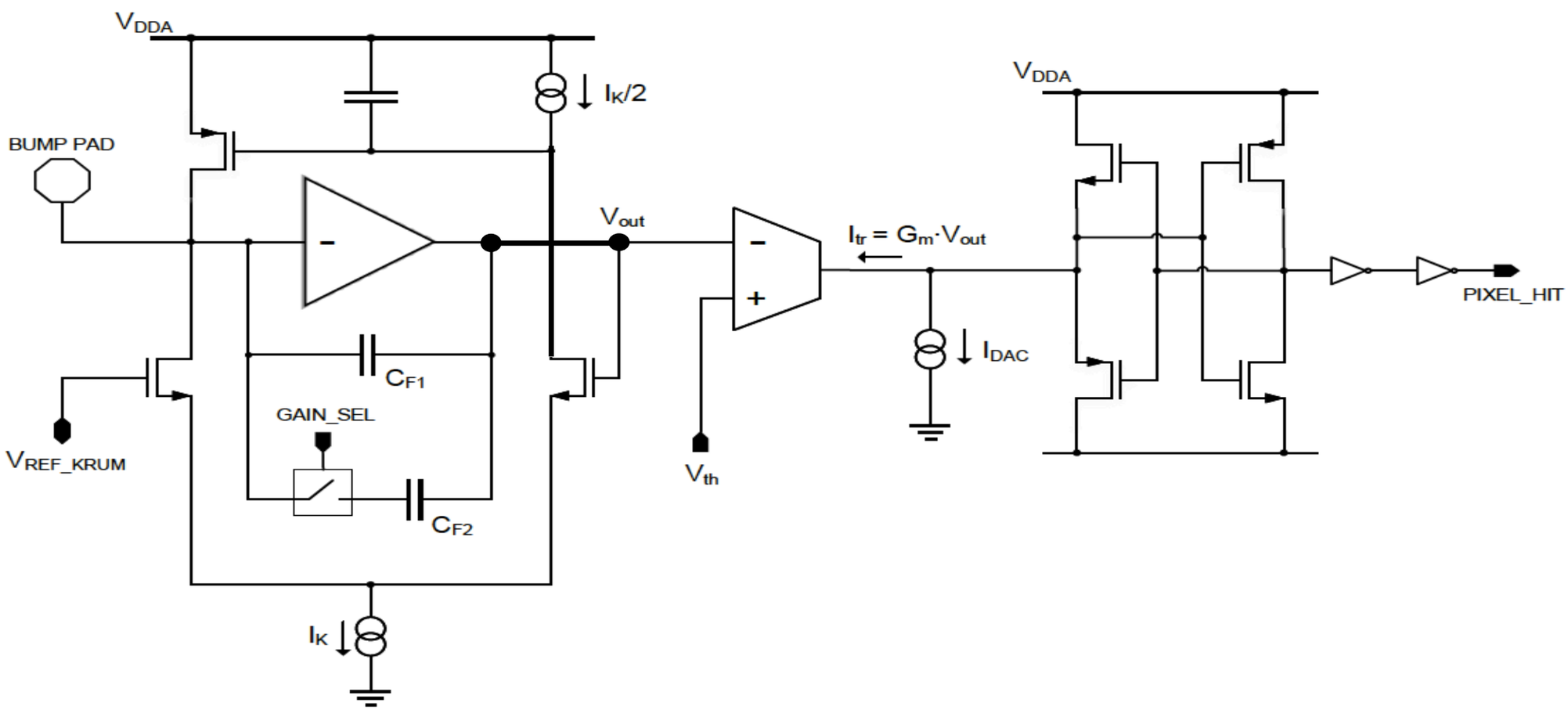
Conclusions

- RD53A shows excellent results: low power, low threshold particle detection with 4-bits signal digitisation at extreme particle rates of HL_LHC are demonstrated for large scale ASIC. Radiation hardness is proved up to at least 500 Mrad
- Sensor R&D is now based on using RD53A. Several test beam are on-going for different type of sensors and level of irradiation and will bring lot of results and information
- ATLAS and CMS chips are planned to be submitted during 2019 as implementation of the RD53 design
- All Analog FE could be made to work for Phase-2 Pixel detector, but improvements is needed in all of them. More measurements and work is needed to better define the Analog FE : work is not finished.
    - comparative measurements with all species of sensor
    - only planar 50x50 and 25x100 have been used
    - only one irradiated module have been deeply tested
- ATLAS and CMS need to take decision very soon

BACKUP

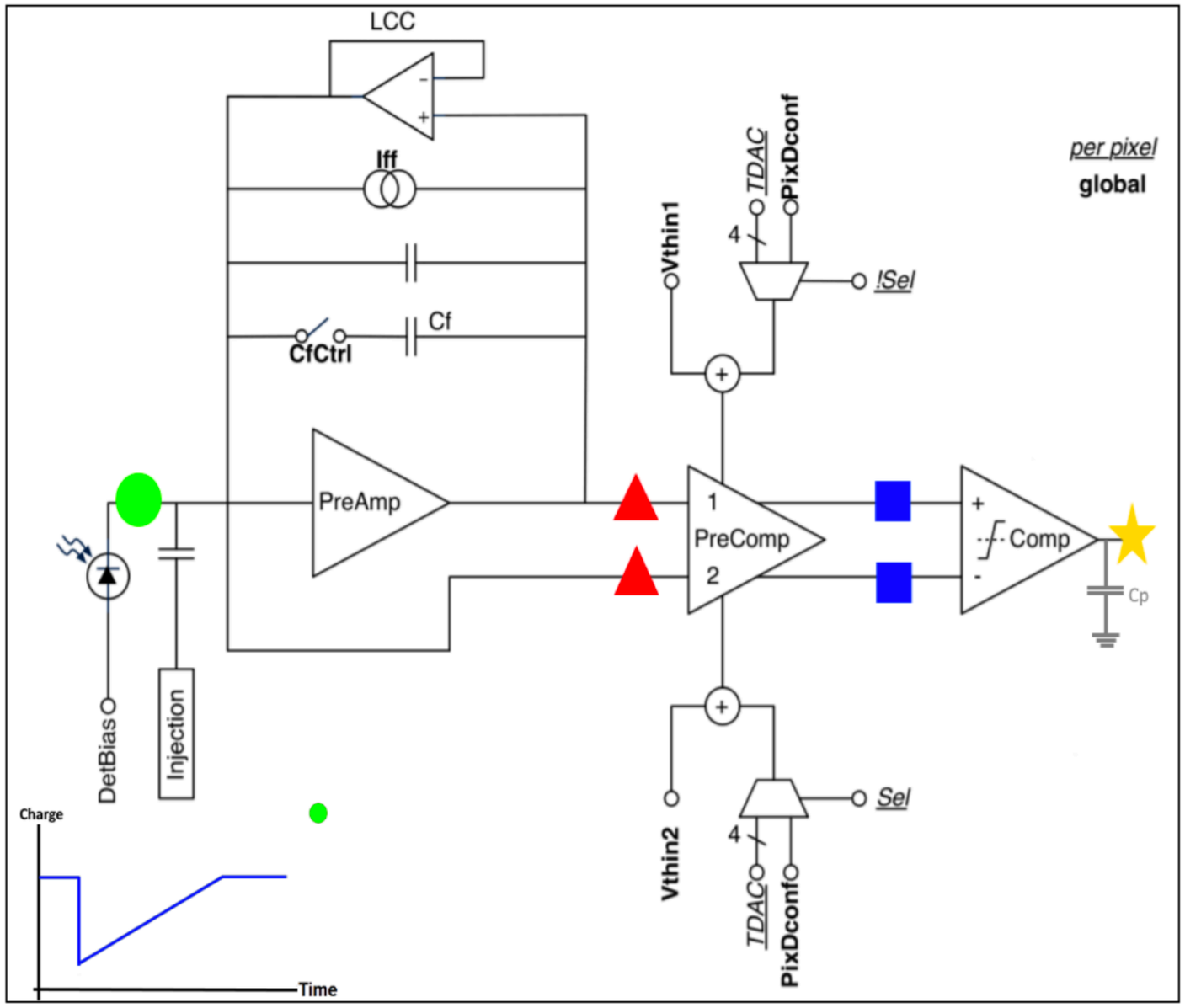
Linear FE

- **Single amplification stage** for minimum power dissipation
- **Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- Asynchronous, low power **current comparator**
- **Threshold adjusting with global 8bit DAC and local 4 bit DAC single pixel for threshold tuning**



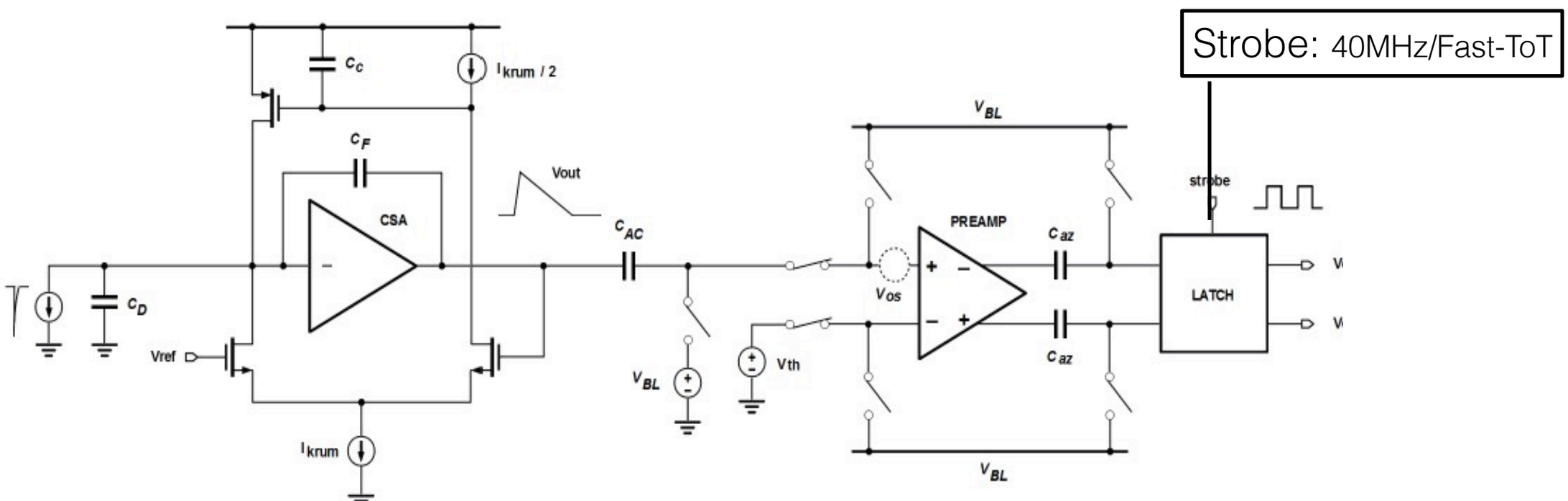
Differential FE

- **Continuous reset integrator** first stage with **DC-coupled pre-comparator stage**
- Two-stage open loop, **fully differential input comparator**
- **Leakage current compensation**
- **Threshold adjusting** with global 8bit DAC and local 4+1 bit DAC



Synch FE

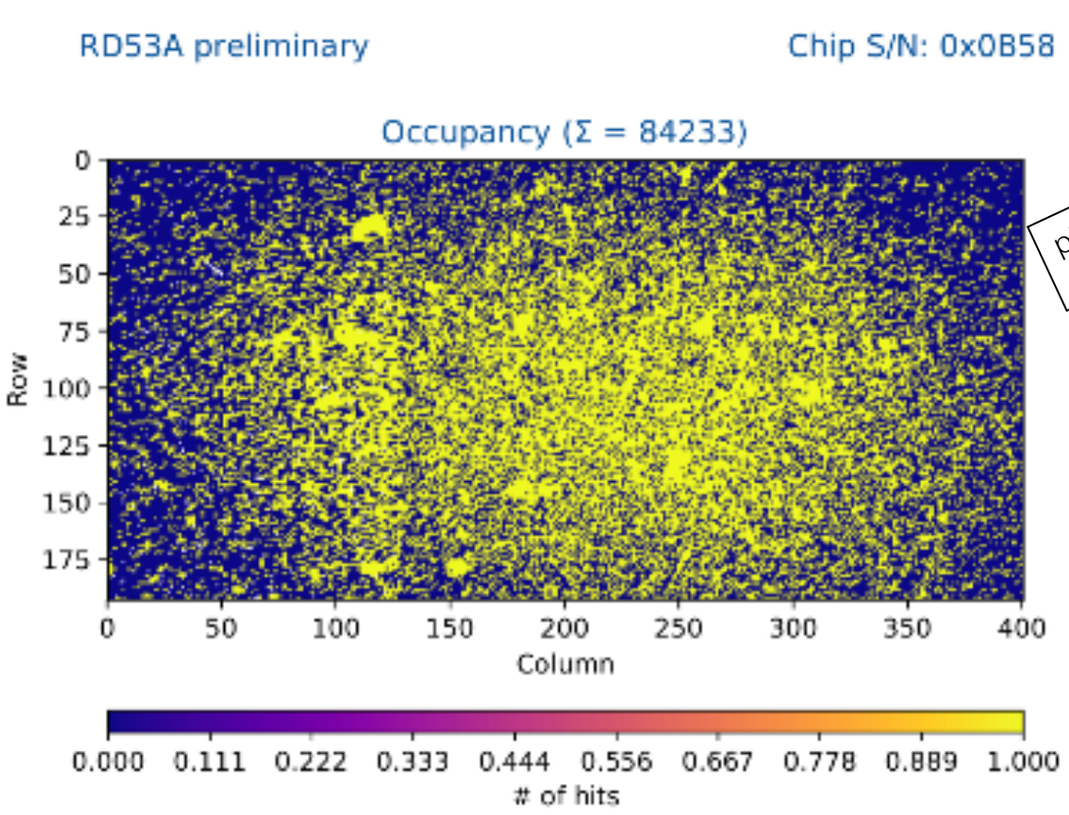
- Telescopic-cascoded CSA with Krummenacher feedback for linear ToT charge encoding
- Synchronous hit discriminator with track-and-latch comparator
  - I**n-time threshold ~ absolute threshold**
- No local trimming needed, threshold tuning done using the auto-zeroing technique
  - Efficient self-calibration can be performed according to online machine operations (take about 4-600ns every 80 µs, during *Abort Gap* which is 3us long), so even if some parameters like radiation or T change, tuning is re-optimized immediately
  - No trimming-DAC -> less prone to SEU misconfiguration -> pixels don't risk to become too noisy
- ToT counting using 40 MHz clock or **Fast local oscillator** using latch as local oscillator (30-400 MHz)



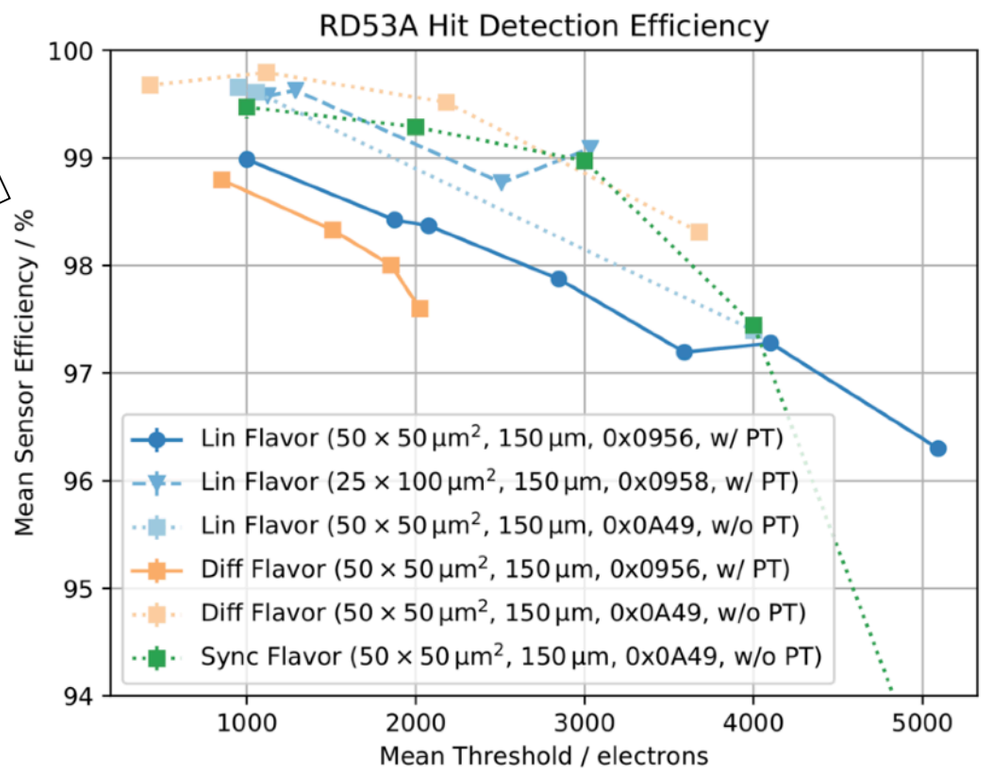
Measurements with Modules: test-beams

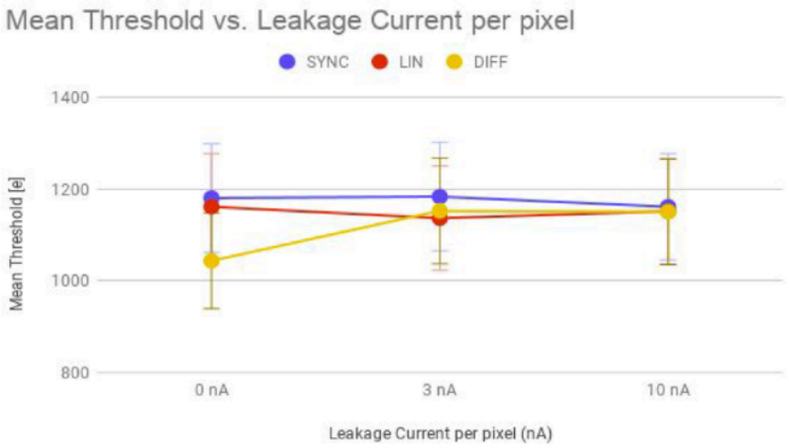
- Test beam done by RD53 to understand chip more than the sensors
  - Preliminary studies show similar results for the three FEs

- Now several test-beam have been done (AIDA-2020, ATLAS, CMS) by the sensor community to study planar and 3D silicon sensors. From October also irradiated modules have started to be studied.
  - Low thresholds (~800e- to 1200e-) are normally achieved
  - Lot of results are coming
  - Important learning curve for everybody in the sensor and RD53 community : tuning of FE is important and has to be optimised depending on the detector and its conditions



plots from M.Vogt

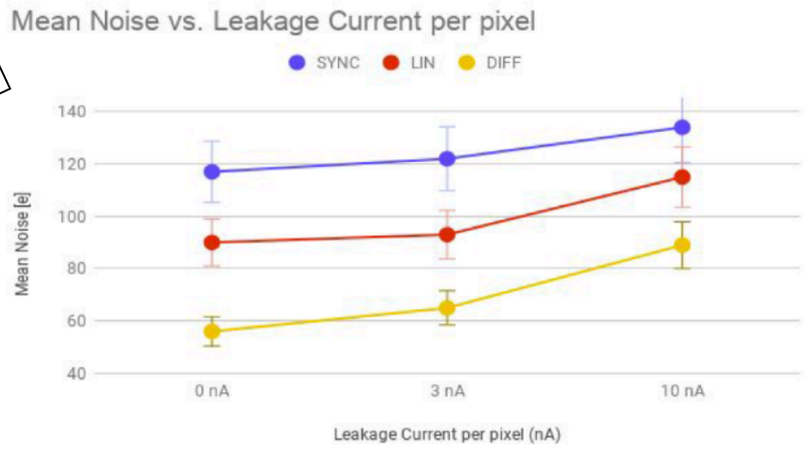




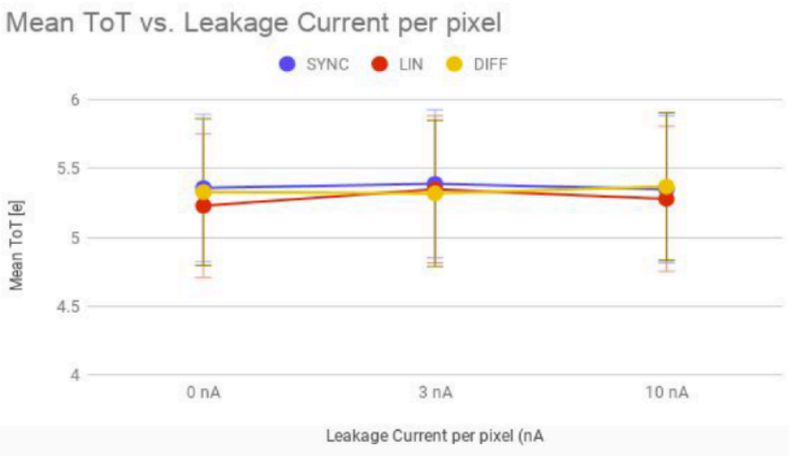
Mean Threshold vs. Leakage Current per pixel (nA)

- All FEs almost have the same threshold dispersion for 10nA scenario.
- LIN FE has less mean threshold than SYNC and DIFF for 3nA scenario.

plots from M.I.Lezki



Mean Noise vs. Leakage Current per pixel (nA)



Mean ToT vs. Leakage Current per pixel (nA)

- All FEs tuned to the target ToT in all configurations.

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