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Results and perspectives from RD53 on the Next Generation Readout Chips for HL-LHC silicon pixel detector phase 2 upgrades

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The Phase 2 upgrades of silicon pixel detectors at HL-LHC experiments feature extreme requirements, such as: 50um x50um pixels, high rate (3 GHzx/cm2) unprecedented radiation levels (1 Grad), high readout speed, serial powering. As a consequence a new readout chip is required

The RD53 collaboration has designed RD53A, a large scale chip demonstrator designed in 65 nm CMOS technology, integrating a matrix of 400x192 pixels. It features design variations in the analog and digital pixel matrix for testing purposes.
The chip size is 20.0mm by 11.8 mm. RD53A is not intended to be a production IC for use in an experiment, and contains design variations for testing purposes, making the pixel matrix non-uniform. The 400x192 pixel matrix features in fact three flavors of analog front-ends and two digital readout architectures. The pixel matrix is built up of 8 by 8 pixel cores. In addition the 64 front-ends within a core are organized in 16 so-called analog islands with 4 fronts ends each, which are embedded in a flat digital synthesized sea.

RD53A has been submitted in August 2017, was received in December 2017 and the whole 2018 year has been dedicated to its comprehensive characterisation.

Test results on single chips including performance qualification for the three analog front-ends will be presented. In addition, the ongoing activities in view of the final chip implementation for the experiments will be outlined

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