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Prototyping and System Testing for the ATLAS ITK Pixel Detector Upgrade

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In 2026 the High-Luminosity Large Hadron Collider (HL-LHC) is scheduled to replace the successful LHC. The HL-LHC will deliver up to ten times the amount of data as the currently running machine, owing to a higher instantaneous luminosity. This increased luminosity will result not only in a much more demanding environment in terms of radiation damage, but also in up to 200 interactions happening simultaneously in one bunch crossing –conditions the current ATLAS tracking detectors can not cope with.
It is therefore foreseen to replace the whole inner tracking system of ATLAS with an all-silicon tracker comprising pixels in the inner layer and strips of varying length in the outer layer. The tracker will cover a pseudorapity region up to eta<4 considerably extending the range of the current tracking capabilities.
The Pixel detector will consist of five layers in the central region and multiple disk-like structures in the forward regions. The total silicon area will amount to about 13 m2 with a total of nearly 10000 individual silicon pixel modules. To provide sufficient radiation tolerance, different sensor types will be employed depending on the region of the detector. A radiation hard readout chip is developed in cooperation with the CMS collaboration within the RD53 Collaboration in 65 nm technology. To be able to accommodate the much more advanced detector within the envelopes of the existing experiment, novel powering, control and data transmission techniques are being employed.
To prototype the system and integration aspects of these new approaches, an extended system testing program is currently exercised. As first prototypes of the foreseen readout ASIC only become available now, a complete first testing campaign has been performed on modules based on the readout frontend of the ATLAS insertable b-layer, the Fei4 ASIC[1]. The Fei4 includes already many of the features of the future readout chip and allows to test a wide range of system aspects.
Modules are assembled in a distributed fashion over many participating institutes. Their testing, shipment and continuous quality control is exercised. In parallel, fully functional local supports are constructed and their mechanical, thermal and electrical performance is tested. Modules and local supports are combined into system tests which allows to exercise the integration and study system aspects of the planned detector layout.
As the detector will for the first time employ a serial powering scheme [2-4], particular attention is put on all aspects related to the powering concept, its control and its influence on the operation and performance of the detector.
In this talk, experience and results from various system tests will be discussed and an outlook on the future plans for prototyping, system testing and integration will be given.

References:
[1] M. Garcia-Sciveres et al., NIM A636 (2010), 155
[2] T. Stockmanns et al., NIM A511 (2003), 174-179
[3] D. Bao Ta et al., NIM A557 (2006), 445-459
[4] L. Gonella et al., JINST 5 (2010), C12002

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