Testbeam characterization of irradiated SINTEF 3D pixel sensors

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On behalf of

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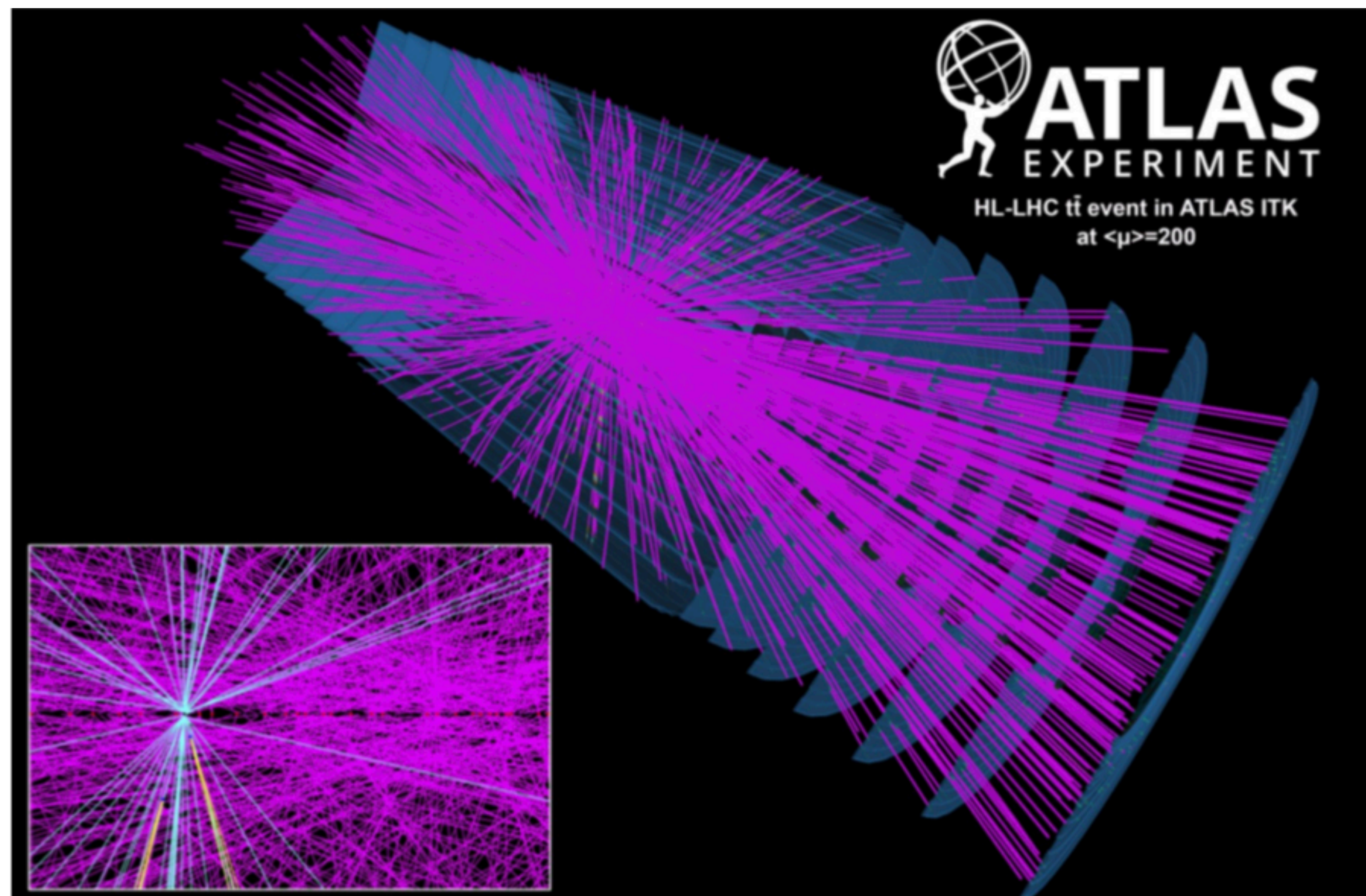
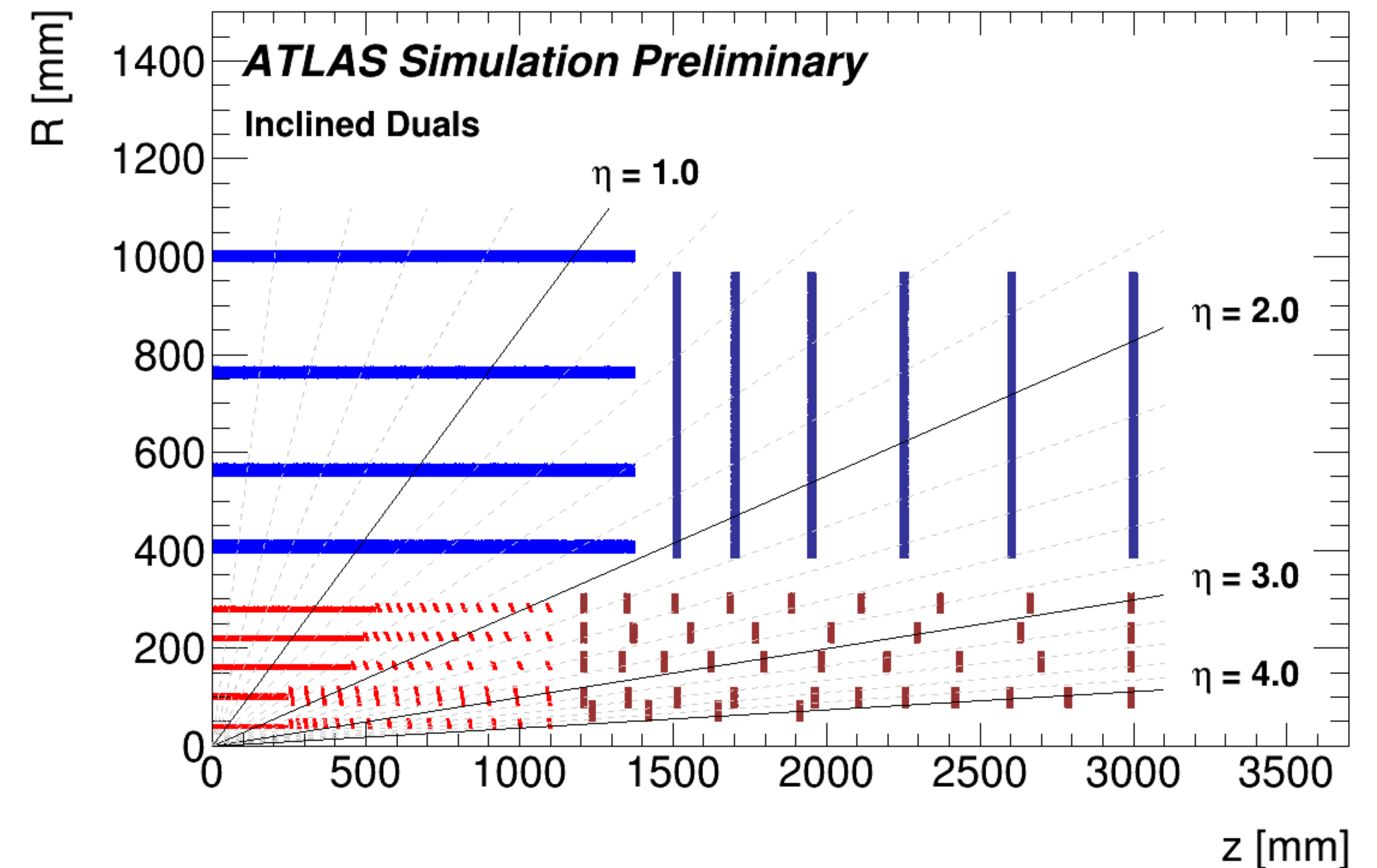
14th Trento workshop on advanced radiation detectors

Upgrade of the LHC and ATLAS

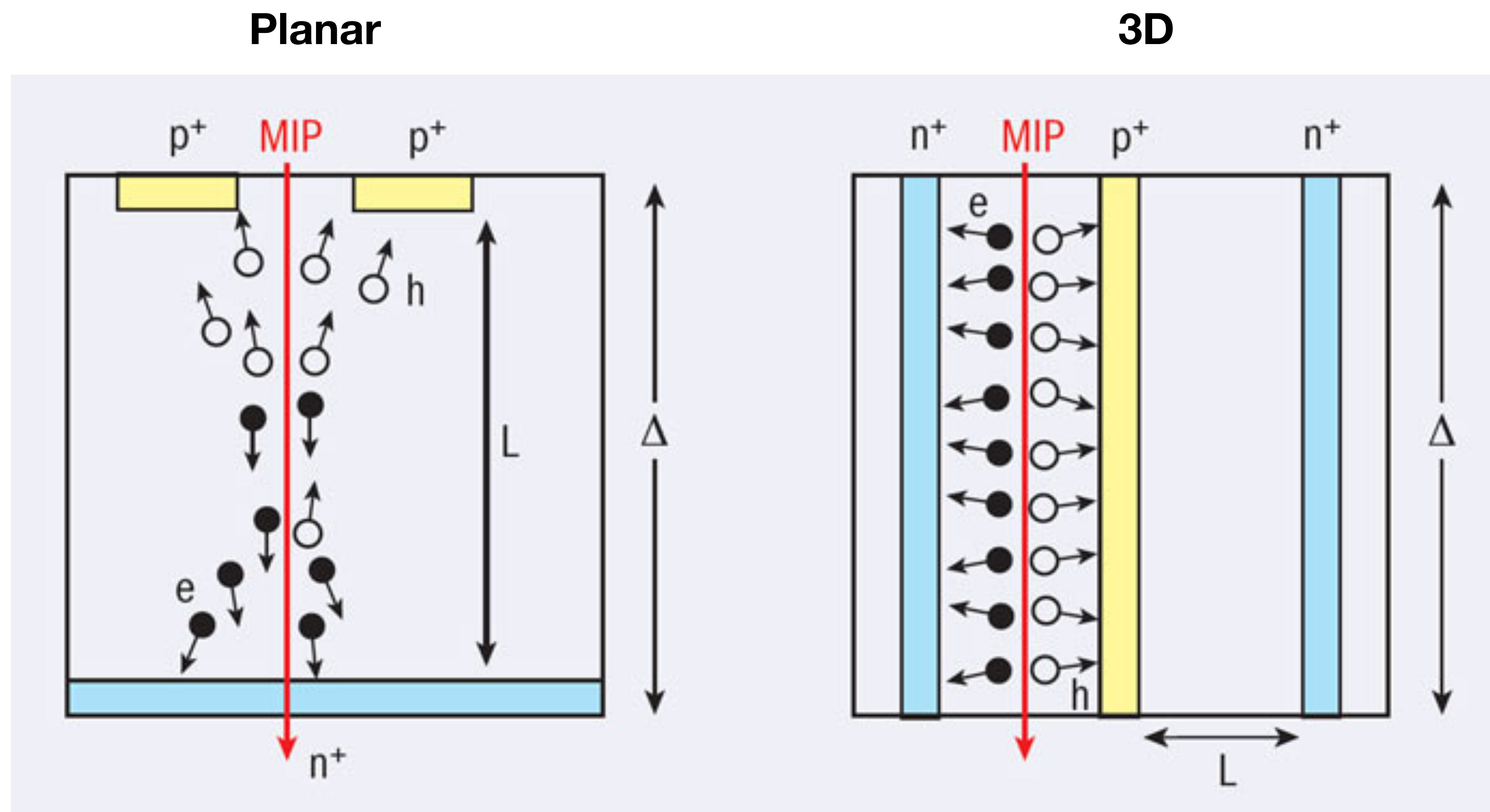
- By 2026 the High-Luminosity LHC should be completed
- Large increase in radiation levels
- The ATLAS detector will be upgraded to cope with this
- Entire Inner detector will be replaced by a new all silicon detector called the Inner Tracker (ITk)





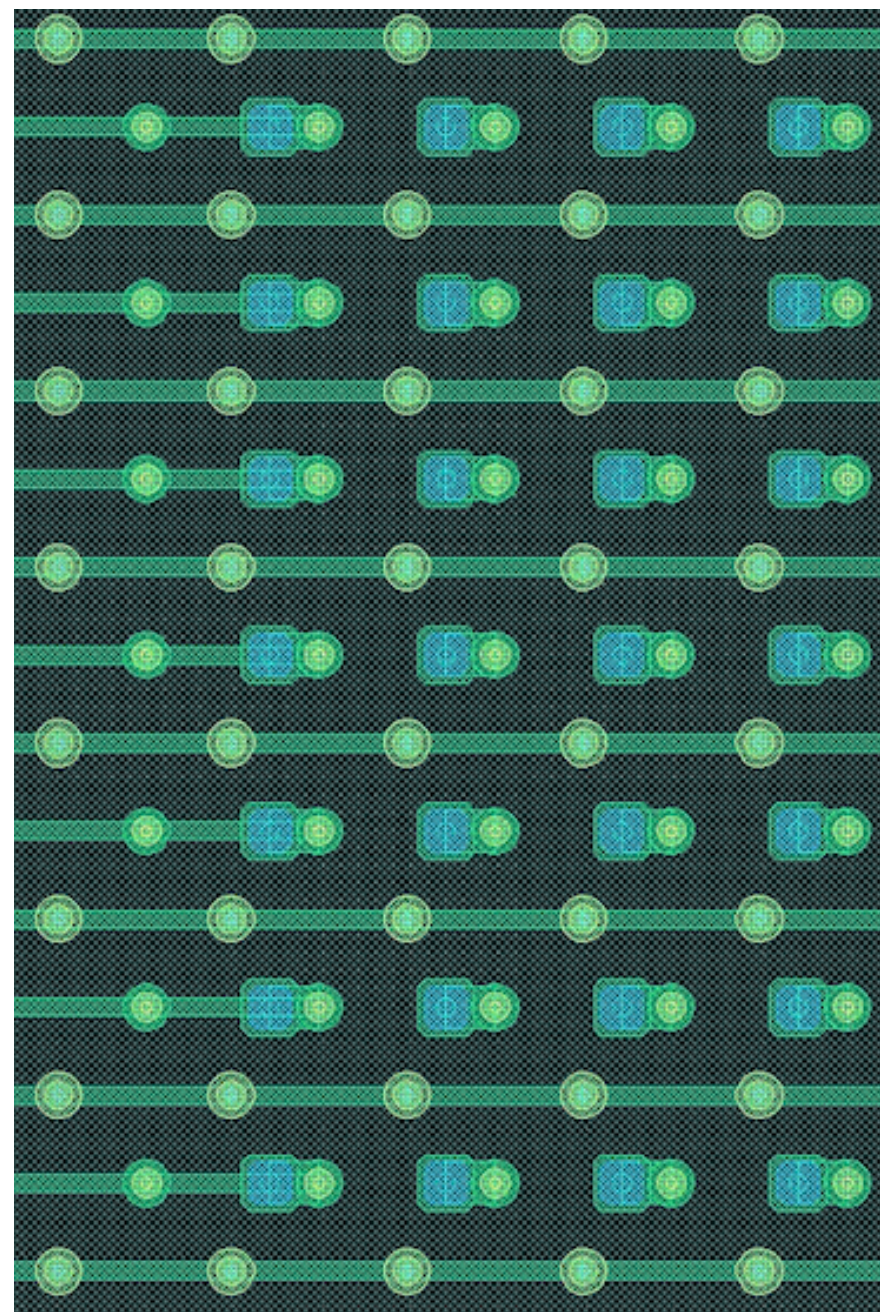
3D silicon pixel detectors

- Different electrode geometry than planar pixel devices
- -> Lower operation voltage and higher radiation hardness

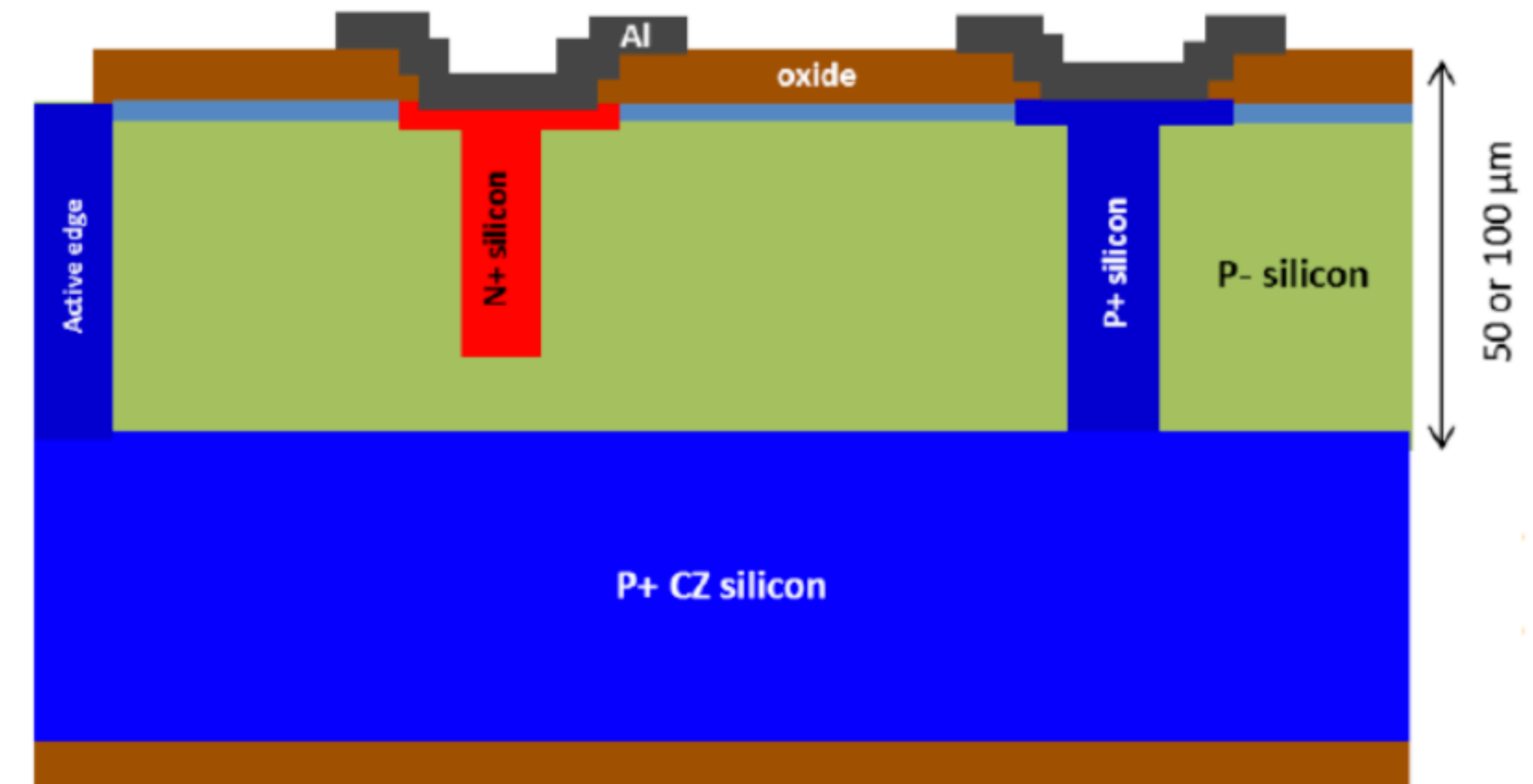


SINTEF prototyping Run 4

- Full 3D active edge Si-on-Si sensors
- 50 - 100 μm active layer, column diameter drawn as 3 μm
- Active edge trench 2.5 μm wide

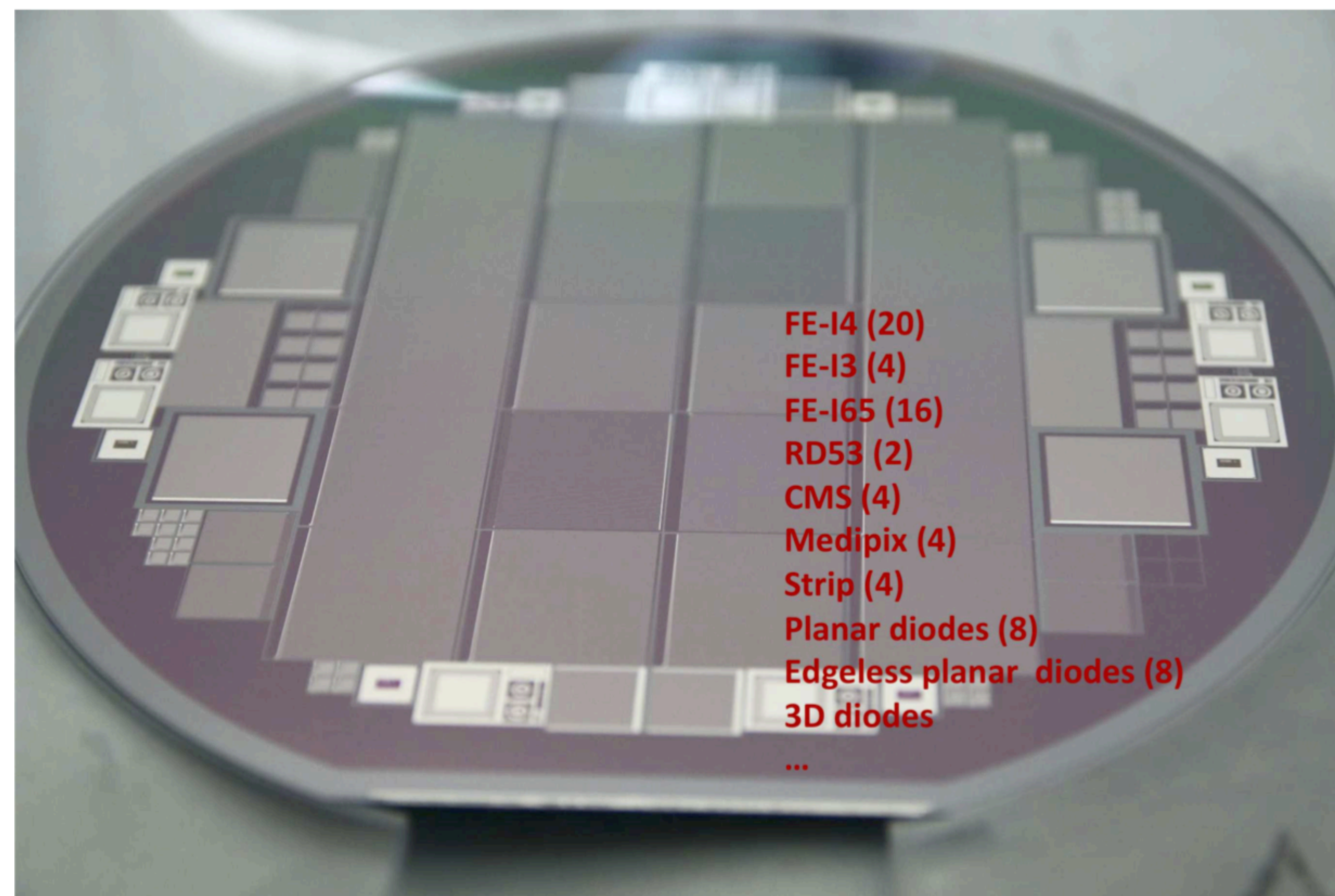


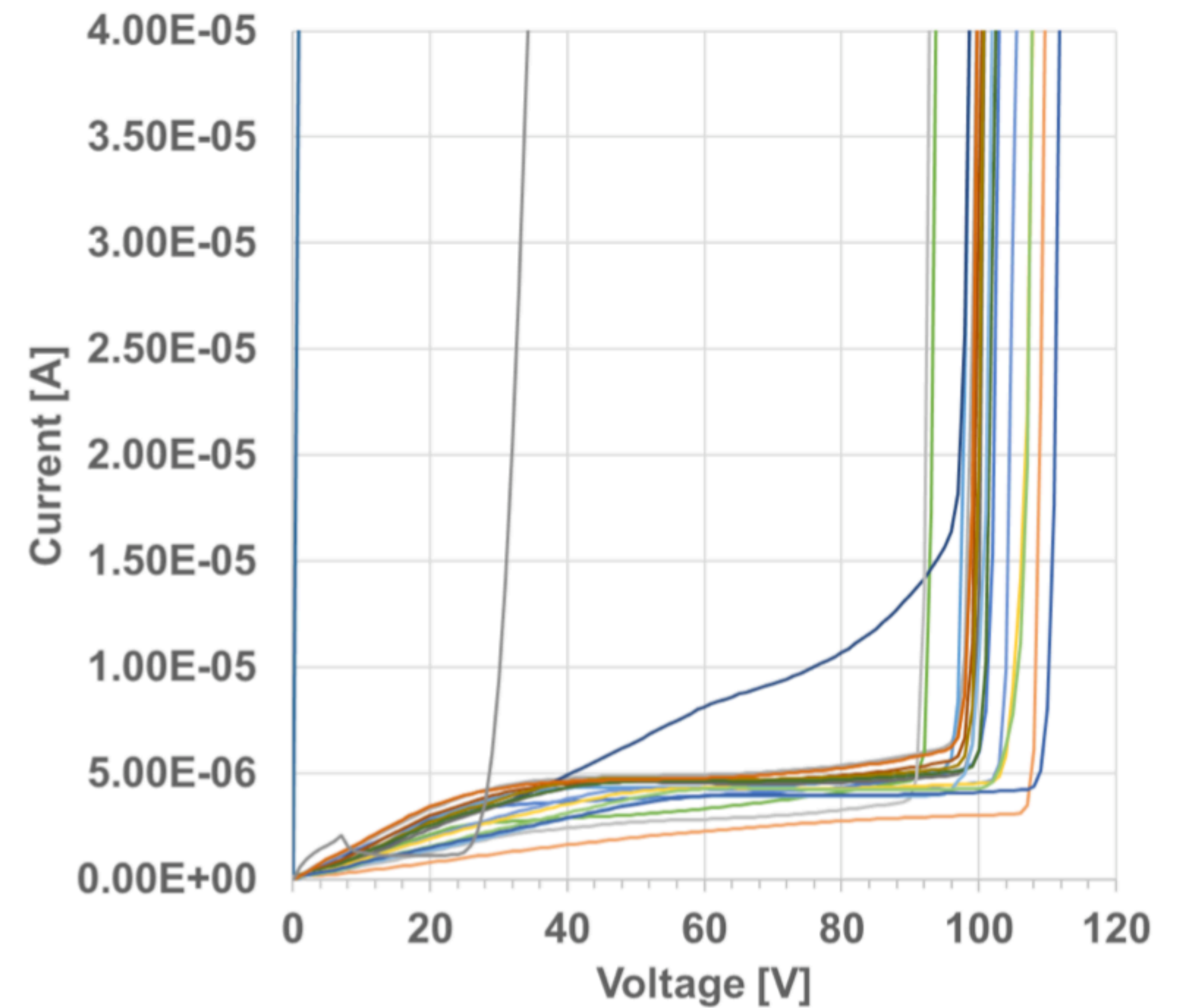
- 50x50 μm pixel size
- 1 electrode pr. pixel cell
- Bias electrodes etched through bulk
- Readout electrode column not connected to support wafer -> shows some efficiency



Fabrication and yield

- Wafer floorplan has a number of layouts, notably the IBL-generation (FE-I4 compatible) and the ITk prototype (RD53A compatible)
- Most FE-I4 (20), 2 RD53 on each wafer.
- Manual probing on temporary metal show a yield of ~70% (FE-I4)
- Breakdown at -100V





I-V curves for all FE-I4 sensors on one wafer

RD53A

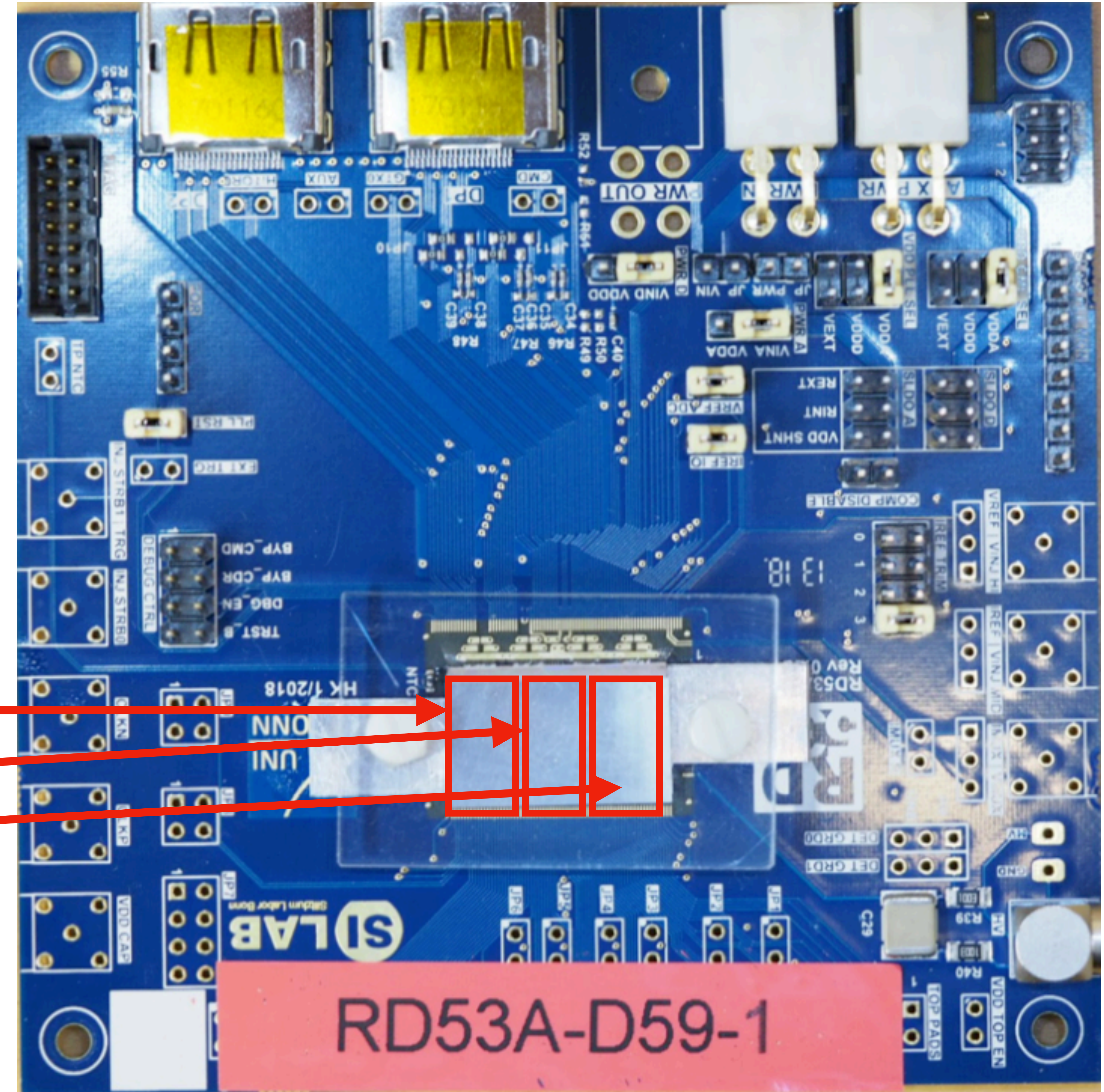
- ATLAS ITk prototype ASIC
- Contains 3 different front ends:
    1. Synchronous
    2. Linear
    3. Differential

Characterized the sensors using the linear and differential front ends

Synchronous

Linear

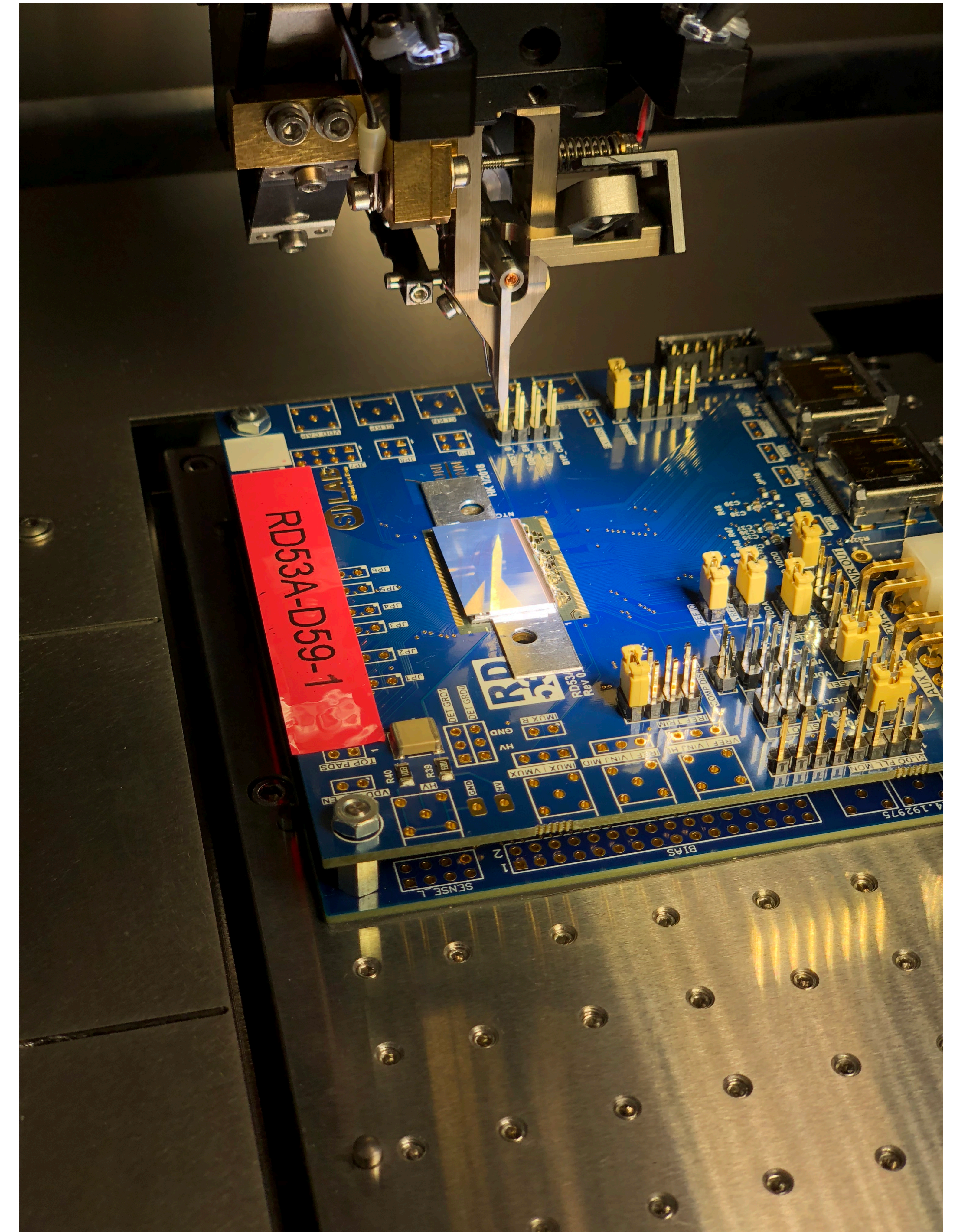
Differential



Further processing

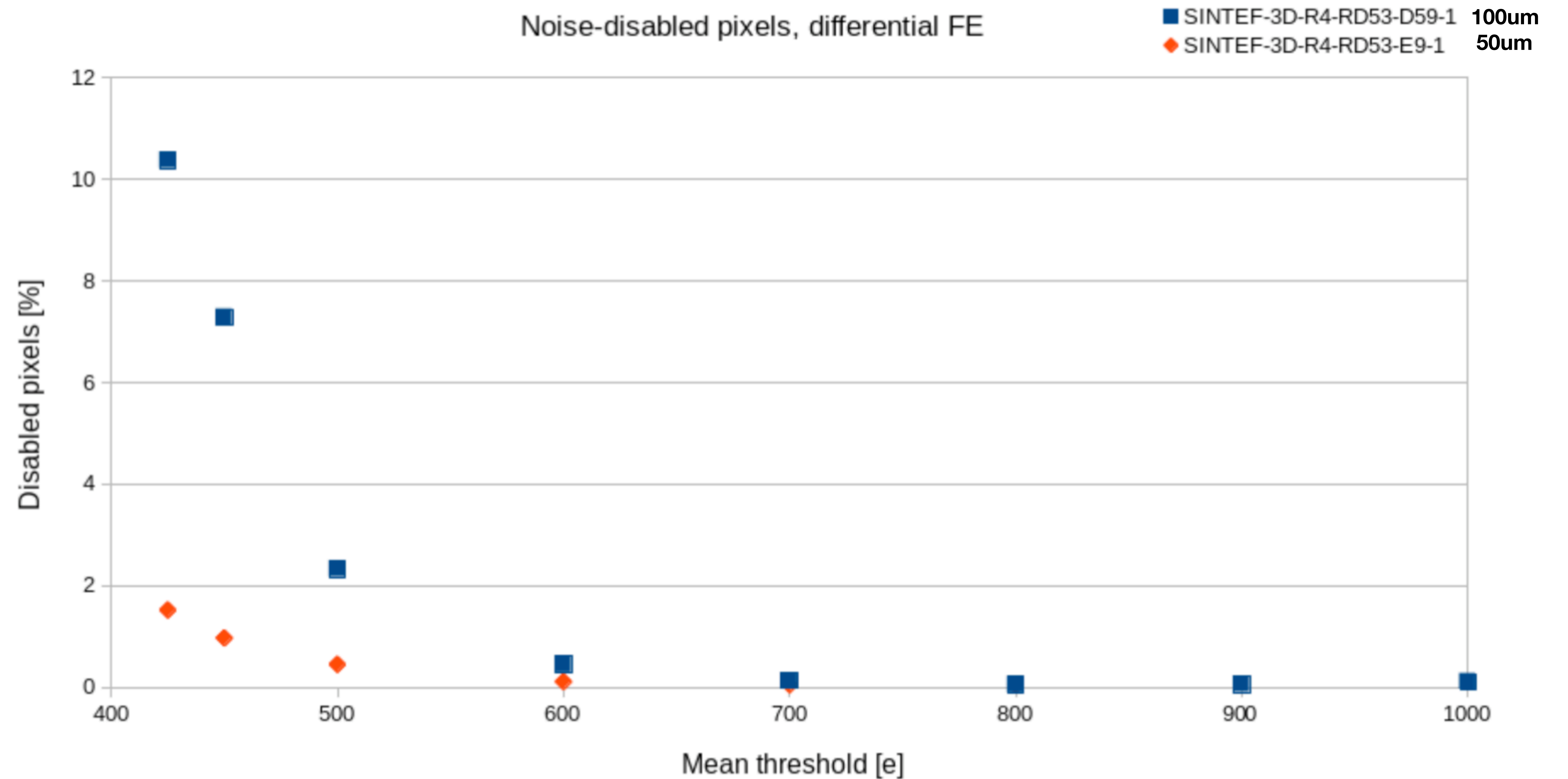
- Under-bump metallisation (UBM) and Flip-Chip was done at Fraunhofer IZM in berlin.
- 8 wafers selected for this, 4 of which was back-side thinned
- Mounting and wire-bonding to SCCs was done at the University of Oslo

RD53A hybrid assemblies ready for mounting



Bench test of modules

- RD53 asic with RD53 compatible sensor chip
- Scans show a relation between noise and device thickness as we go to lower thresholds
- Thinner device -> lower capacitance -> lower noise -> fewer disabled pixels



Testbeam at CERN - unirradiated

- Tested un-irradiated modules at CERN
- In October/November we tested 1 RD53A module (D59-1)
- Normal incidence
- Data taken at bias voltages from -10V to -120V.

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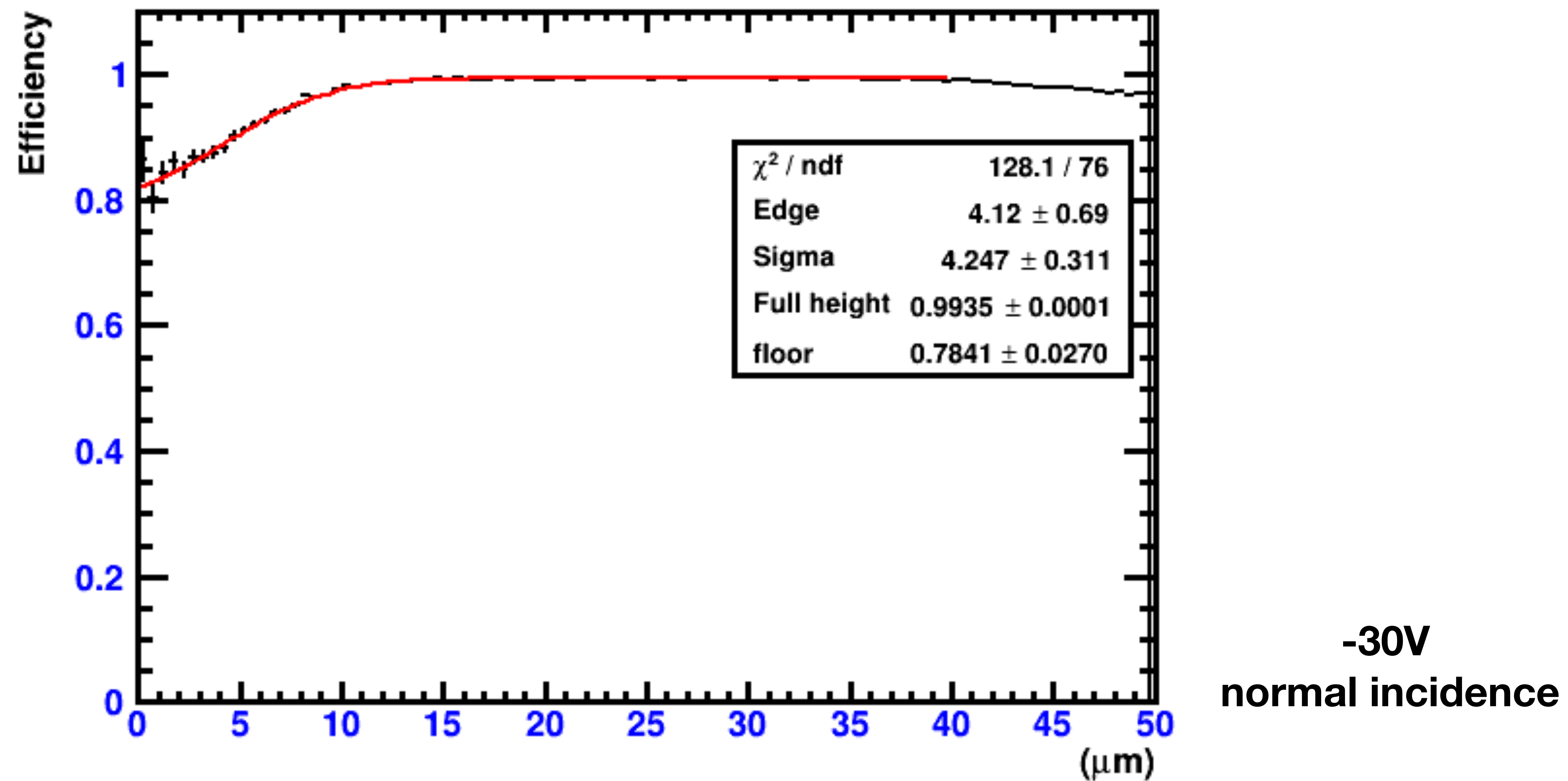
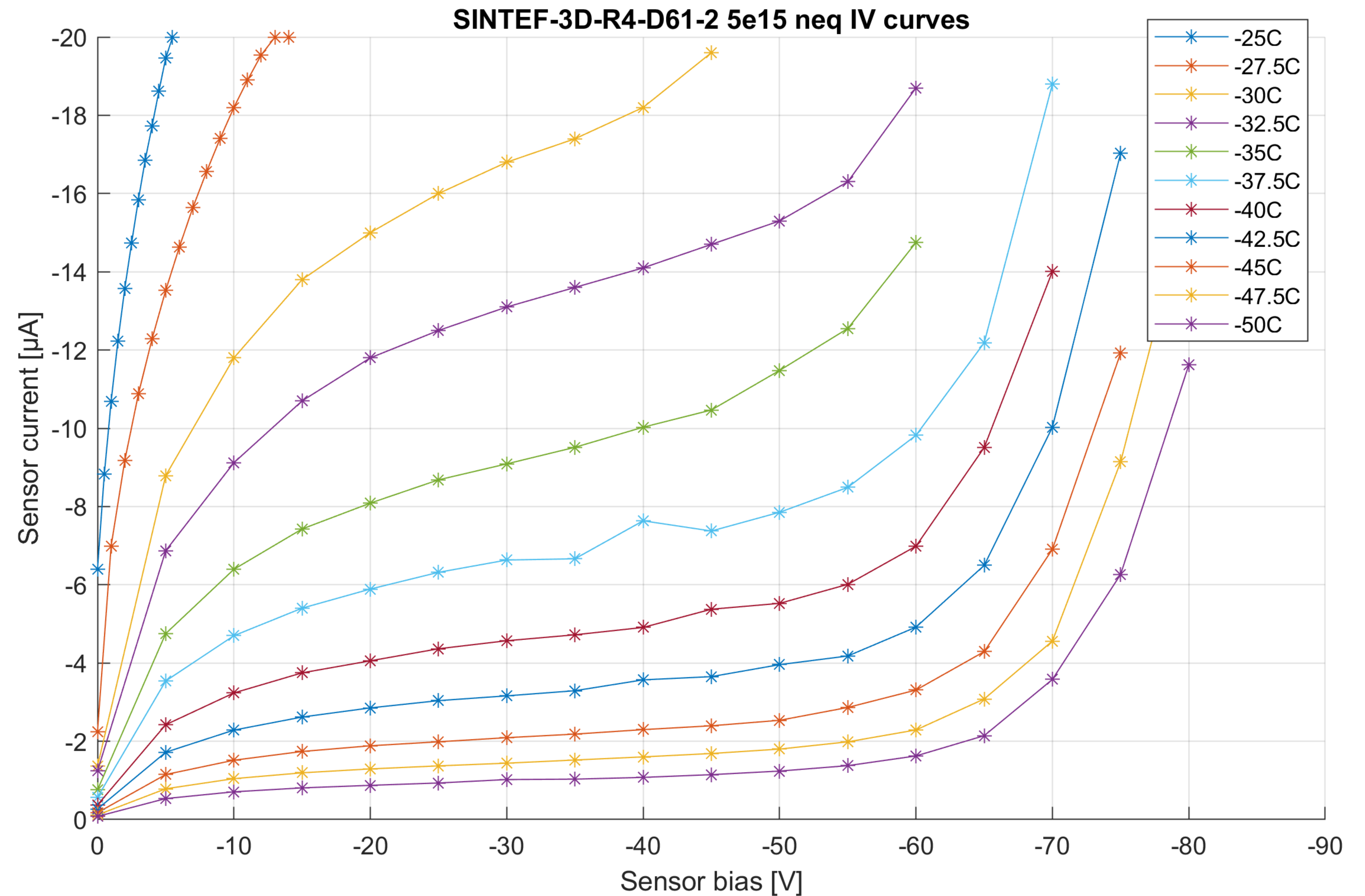
Testbeam at CERN - unirradiated

- Edge of fit = observed diameter of 4.1±0.7μm
- Efficiency >98%



Irradiation and local tests

- Irradiation at Karlsruhe (Germany) and Josef Stefan institute (Slovenia)
- Nominal fluence 5×10^{15} neq/cm2
- IV curves show operational conditions at ~ -40°C
- Module taken to testbeam at DESY in December 2018
- Plan to bring more irradiated modules to DESY in March (Target fluence of 1×10^{16} neq/cm2)

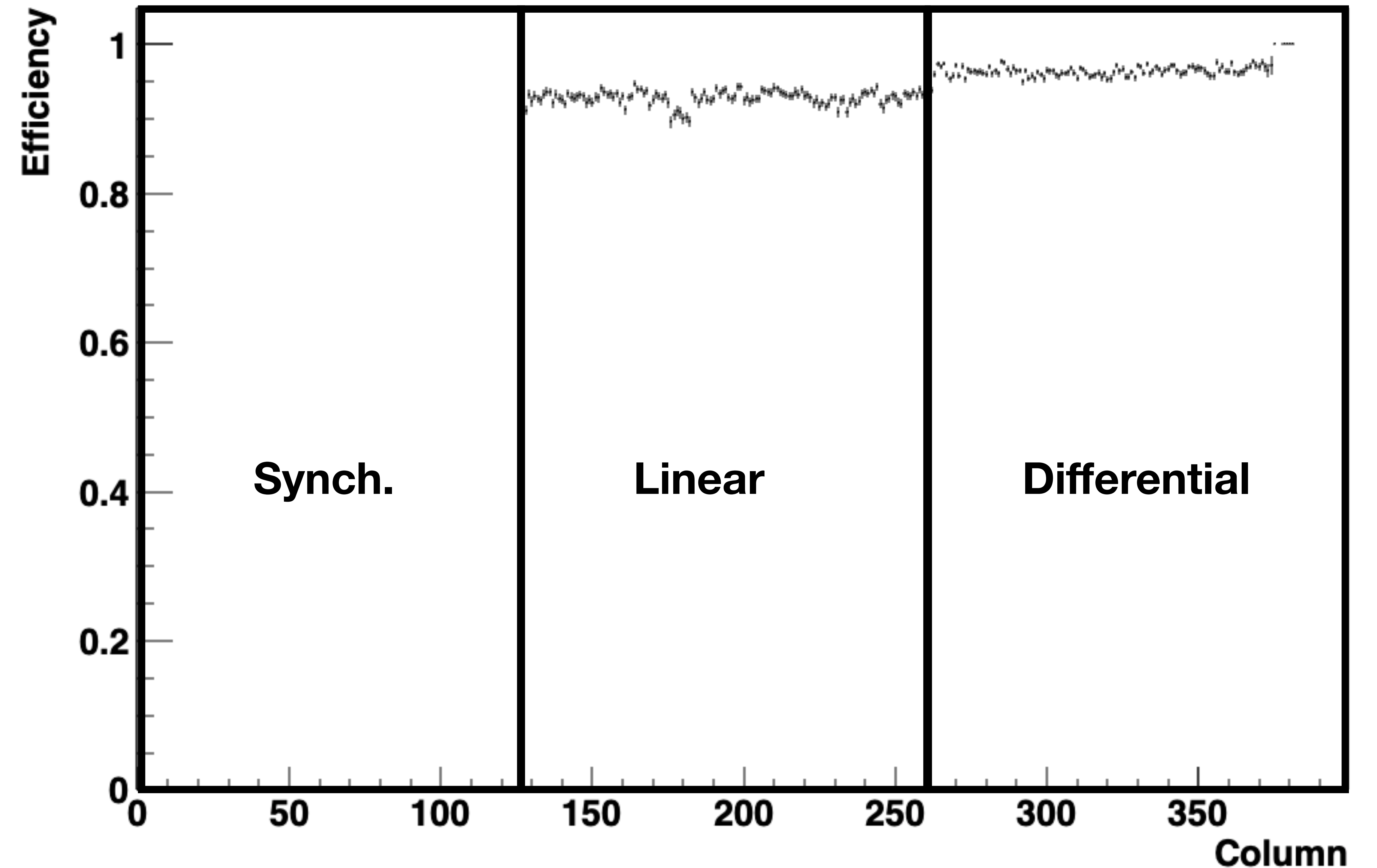


Testbeam at DESY

- Irradiated module (fluence $5x10^{15}$neq/cm2)
- 100um thick device, 50x50um pixel size
- Electron beam -> more multiple scattering
- Cooling by dry ice down to ~ -50°C
- Tuned to ~1000e^-
- Bias voltages between -15V and -60V
- Data taken at normal incidence

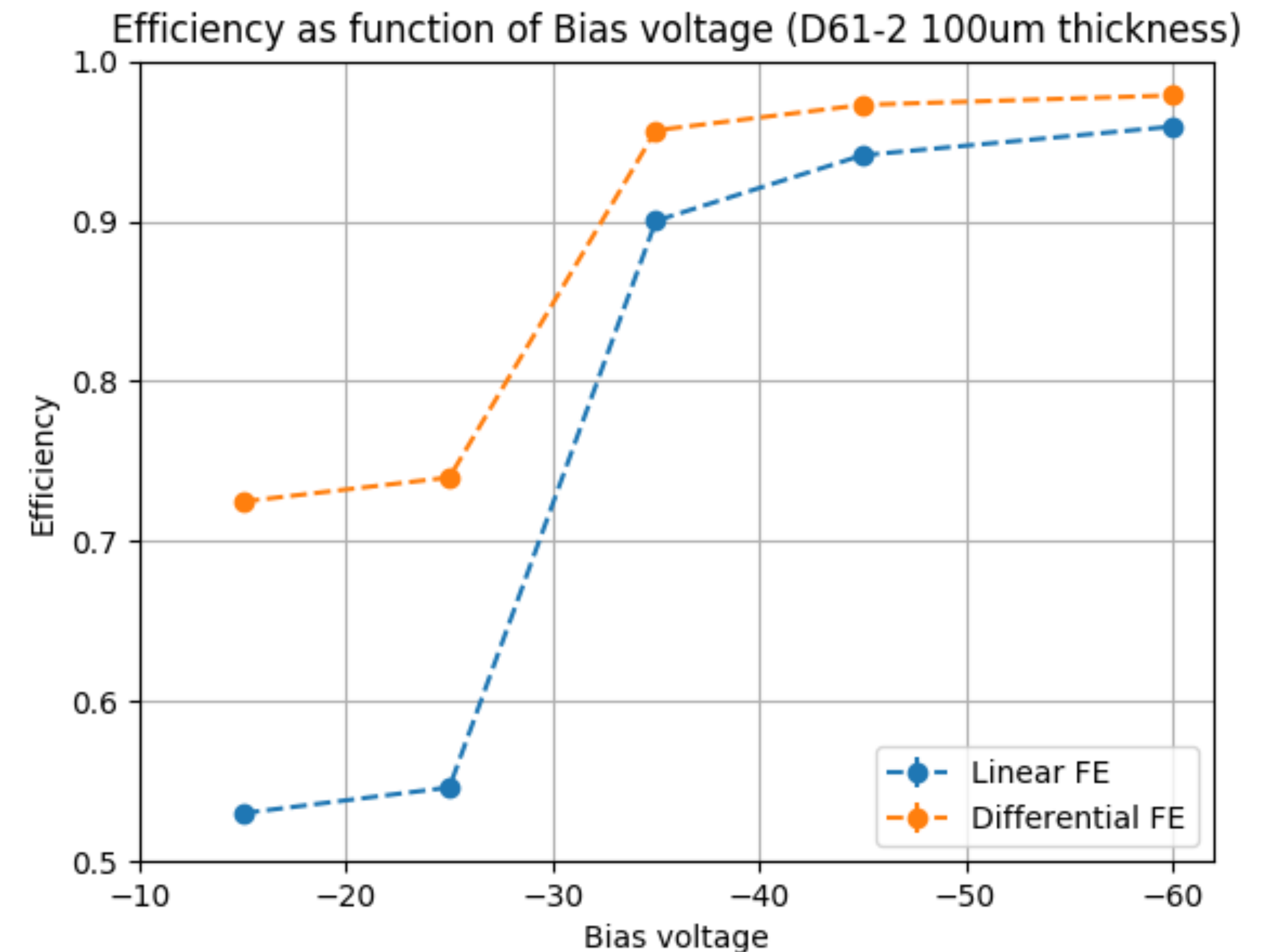
Efficiency analysis - irradiated

- Reconstructed using EUTelescope and analysed with TBmon2
- Difference between linear and differential FE
- Overall efficiency for all runs ~94%



Efficiency vs. Bias voltage - irradiated

- Difference between linear and differential FE decreases with applied bias voltage
- Efficiency for differential FE >97% at -45V
- Efficiency for linear FE >94% at -45V



Conclusion and outlook

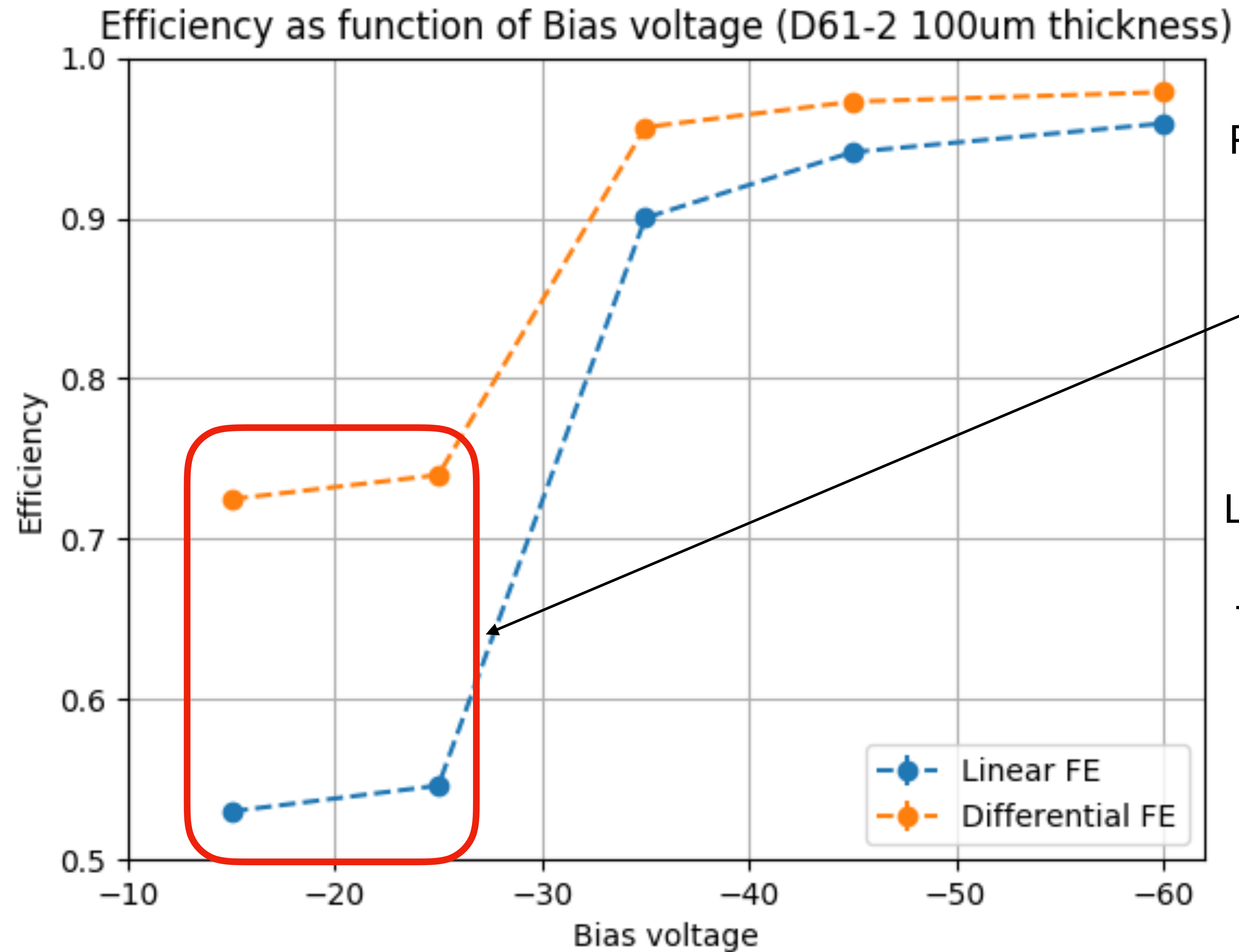
- SINTEF 3D Run-4 achieved very high test-metal yield
- SiSi wafer backside thinning workflow implemented, integrated with UBM
- Successfull flip-chip to FE-I4 and RD53 ASICs
- Promising efficiency measurements of 100um devices after a fluence of $5x10^{15}$neq/cm2

Outlook:

- Efficiency measurements after fluence of $1x10^{16}$neq/cm2
- Finishing 3 more Run-4 wafers
- Expect Run-5 results before summer

Backup slides

Backup



Platau at lower bias voltages might be due
To higher temperatures at -25V runs
Since some dry ice have evaoporated

Possible explanation:

Higher temp -> higher leakage current ->
Larger voltage drop across the 2x100KOhm
resistors in series with sensor
-> lower bias on sensor -> lower efficiency