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Design optimisation of depleted CMOS detectors using TCAD simulations within the CERN-RD50 collaboration

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[1]University of Liverpool, UK; [2]Fondazione Bruno Kessler, Italy

UNIVERSITY OF LIVERPOOL

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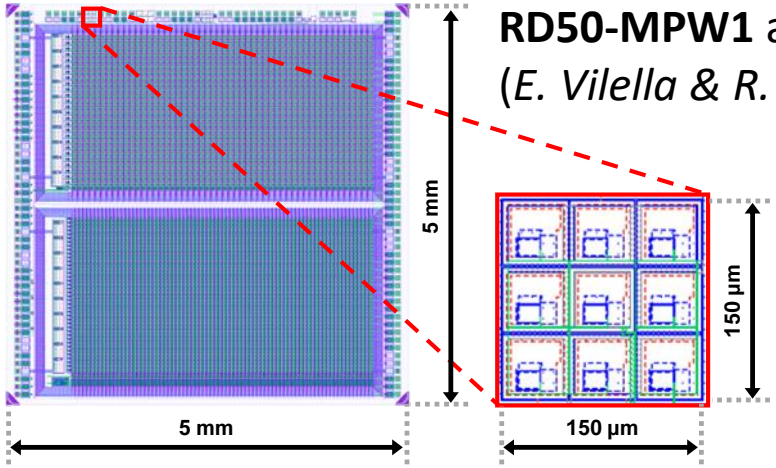
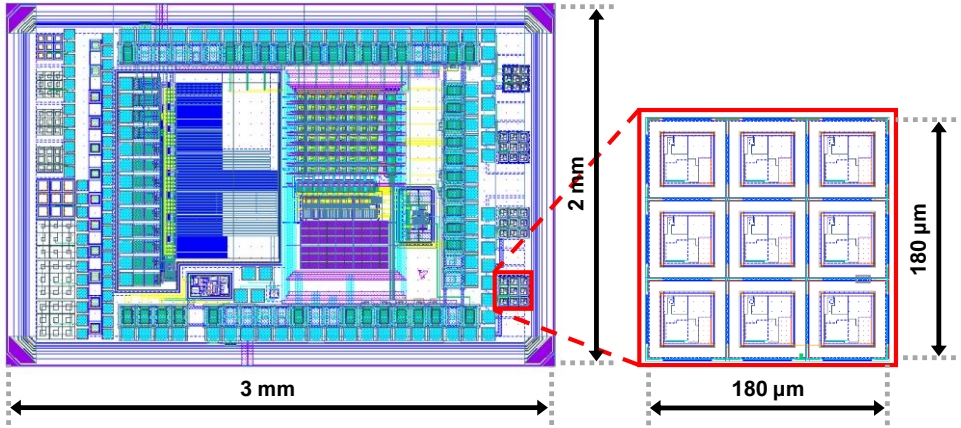
Contents

- Introduction
  - CERN-RD50
  - RD50-MPW1 measurements
- **Leakage current** simulations
  - Post-processing filling
  - Edge defects
- **Breakdown voltage** simulations
  - Electrode spacing
  - Corner geometries
- Future plans
- Summary



RD50-MPW1 and test structure (*E. Vilella & R. Casanova*)

RD50-MPW2 and test structure (*C. Zhang,* et al.)



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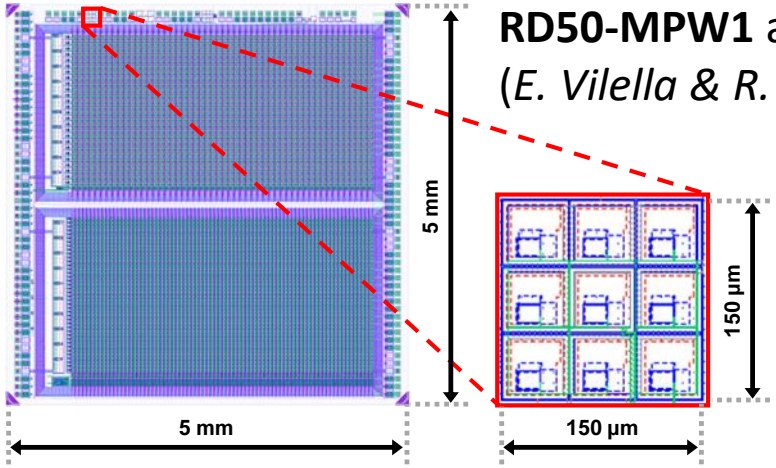

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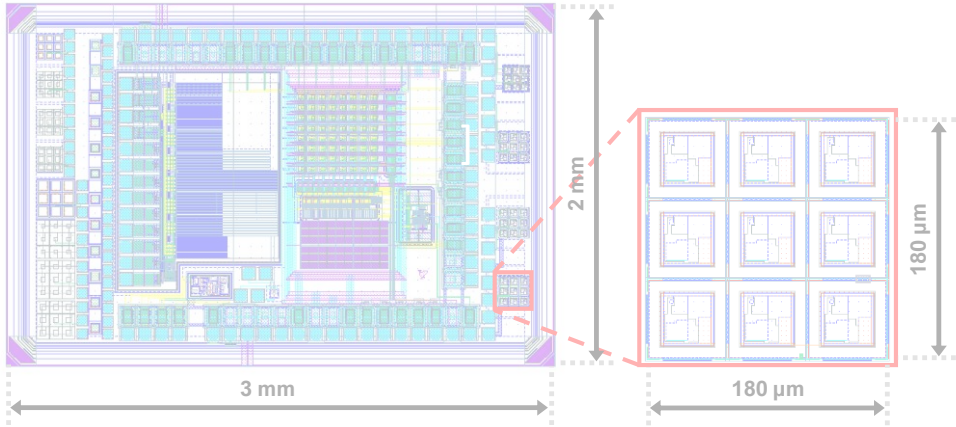
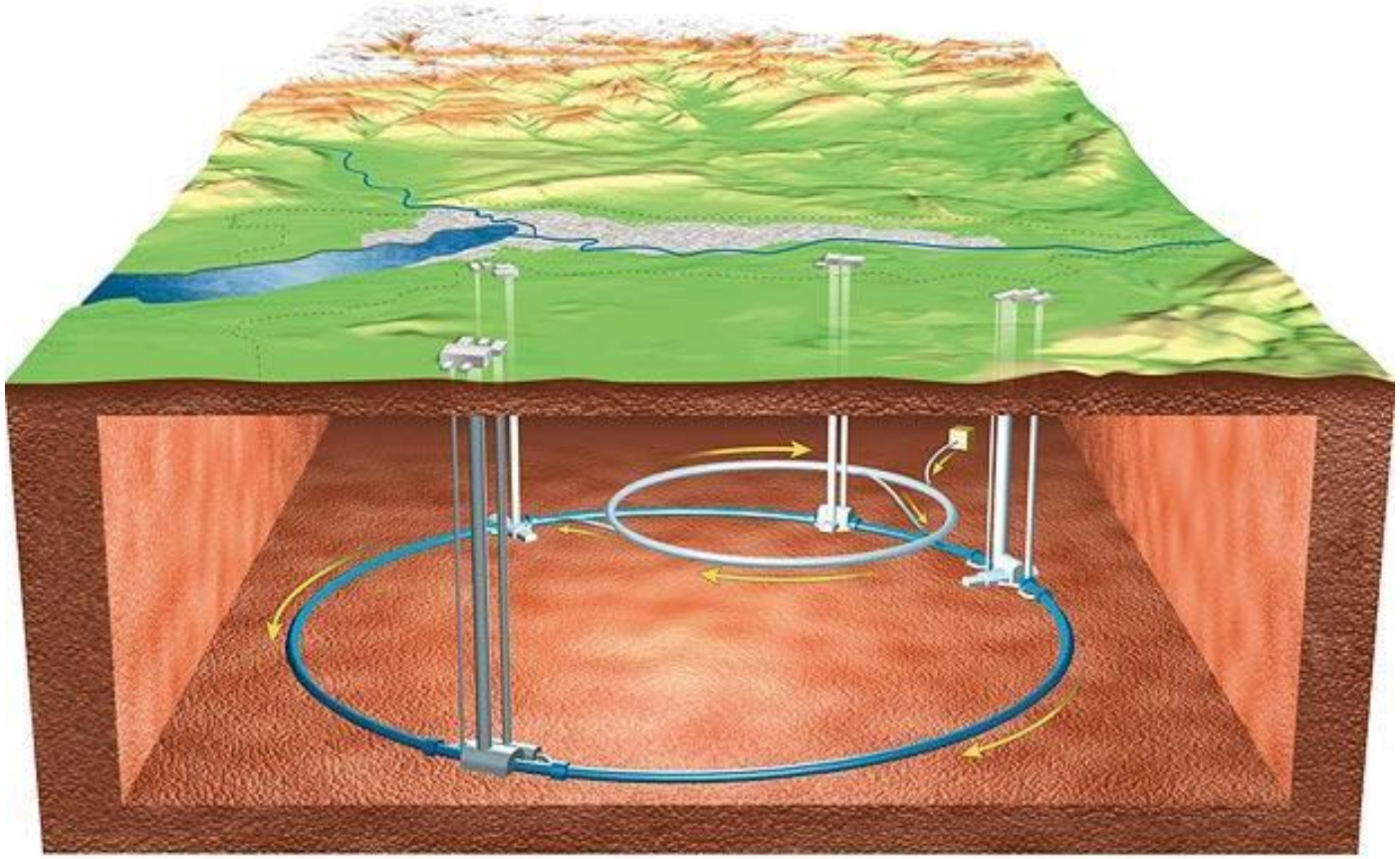


CERN-RD50 collaboration



(above) Diagram of the underground particle accelerator, the Large Hadron Collider (LHC) at CERN *(image from telegraph.co.uk)*

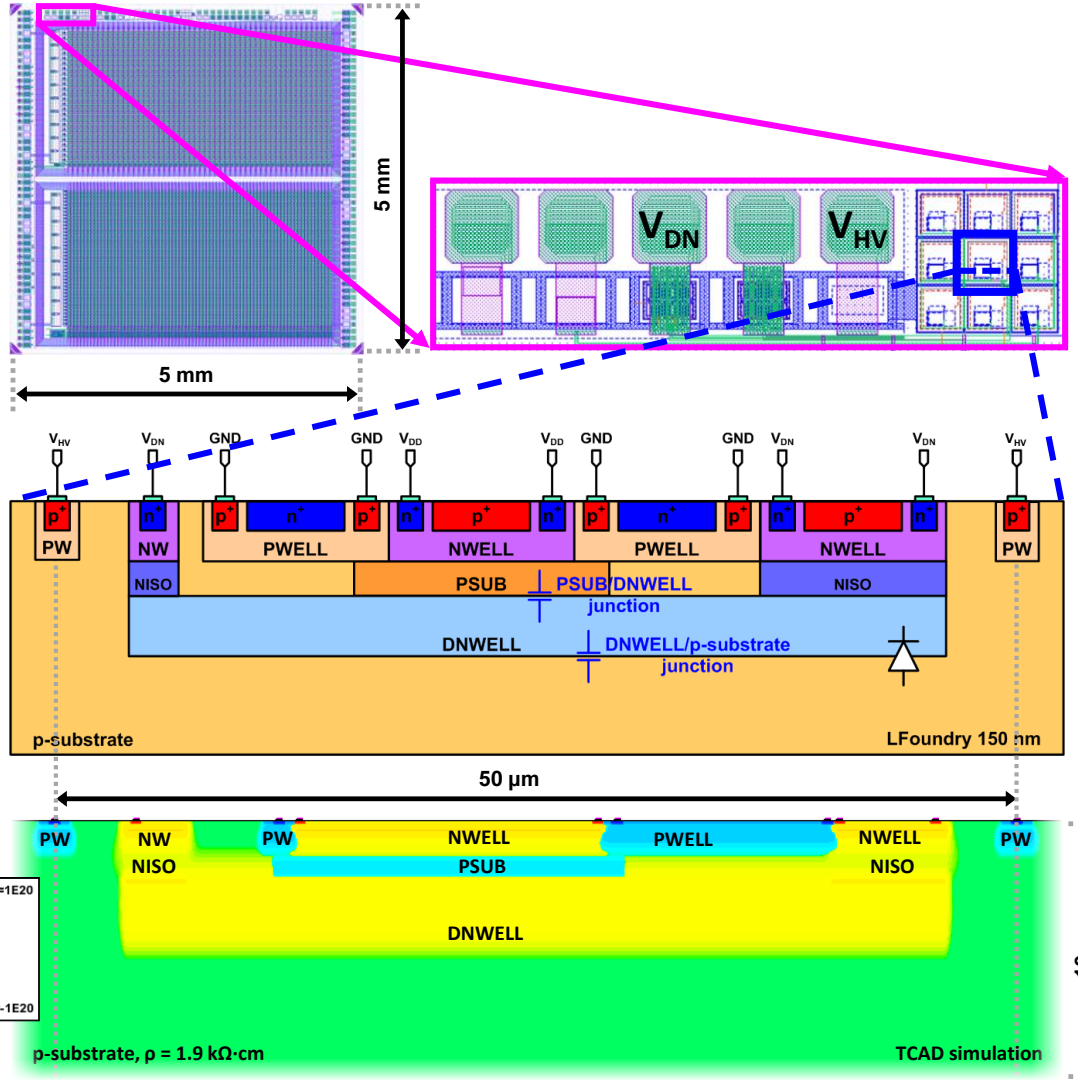
CERN

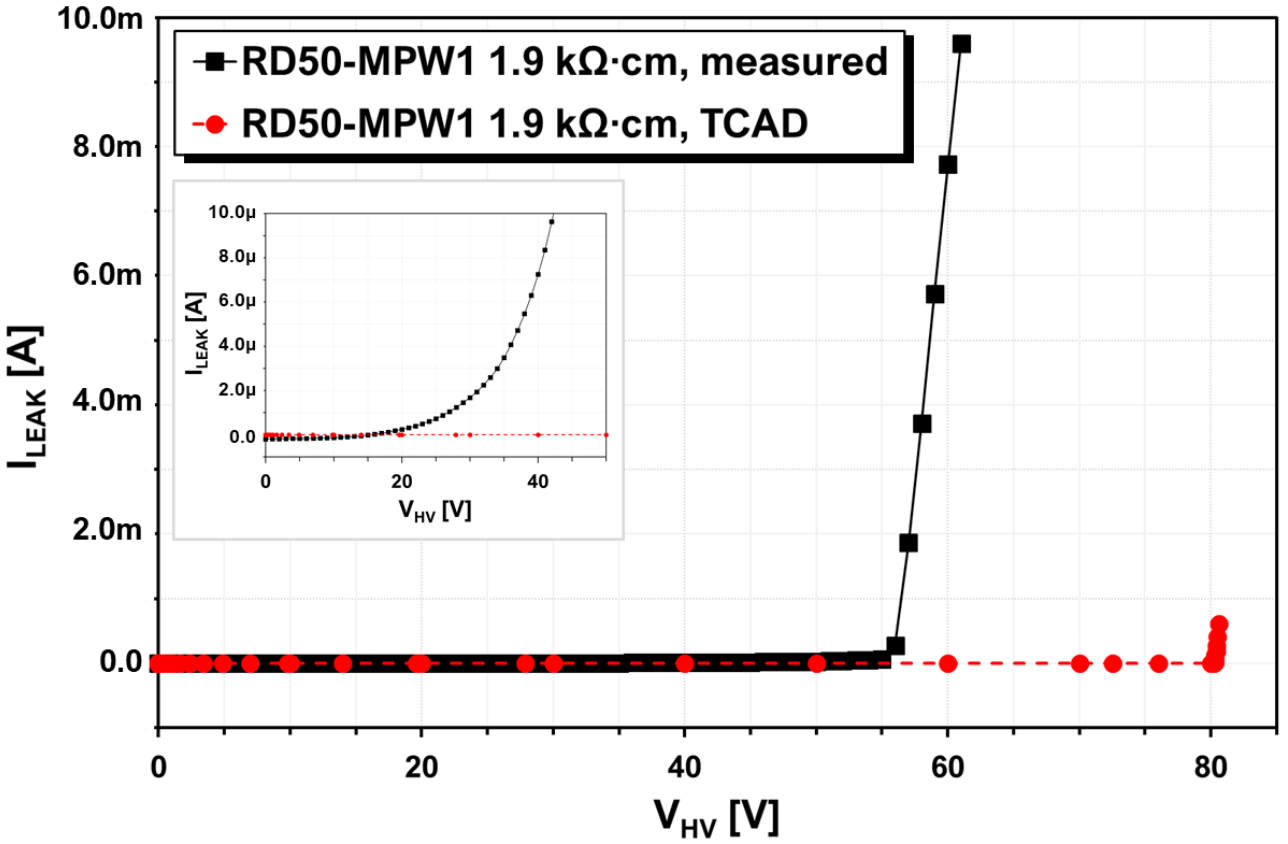
- European Organisation for Nuclear Research
  - What is the nature of our universe?
  - What is it made of?

CERN-RD50 collaboration

- R&D into radiation tolerant semiconductor devices for high energy particle physics experiments
  - HL-LHC (High Luminosity-Large Hadron Collider)
  - FCC (Future Circular Collider)

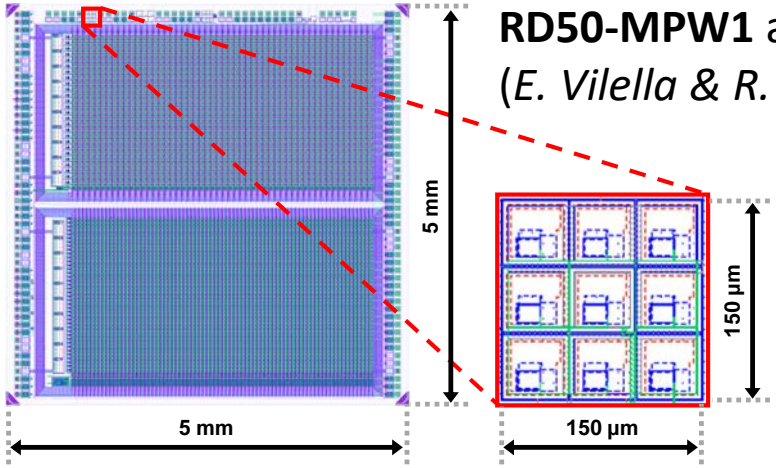
RD50-MPW1 leakage current studies





(above) RD50-MPW1 I-V measurements *(E. Vilella)* compared with TCAD simulation data, **(top-left)** RD50-MPW1 and test structure and pads *(E. Vilella & R. Casanova)*, **(middle-left)** RD50-MPW1 pixel cross-section diagram, not to scale *(E. Vilella)*, **(left-bottom)** RD50-MPW1 pixel cross-section TCAD simulation

Contents



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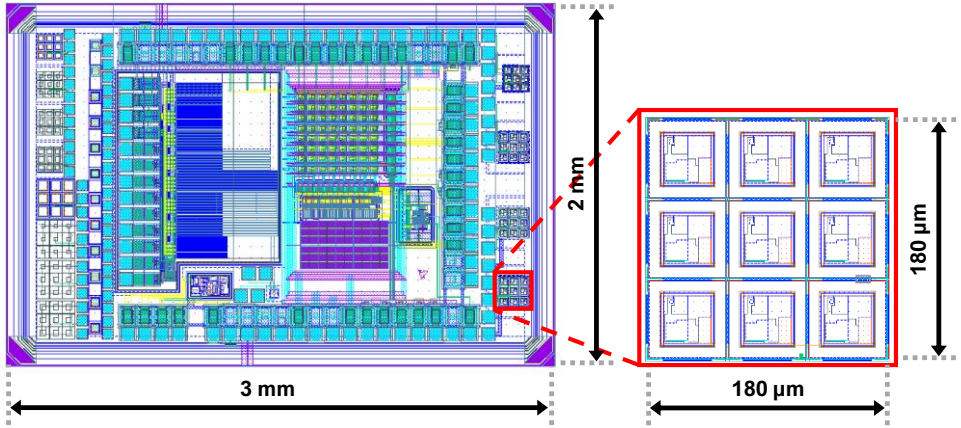

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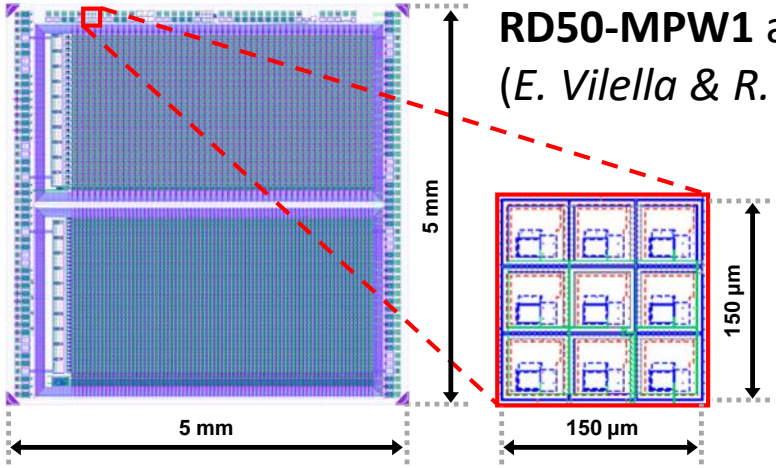

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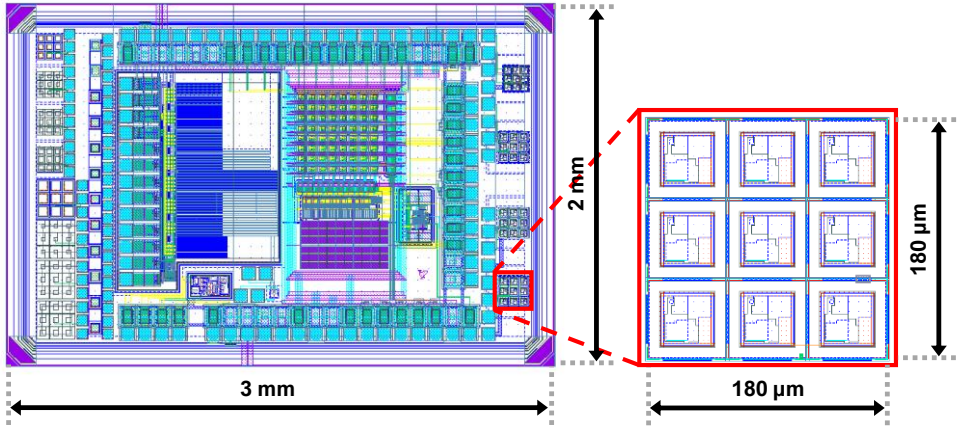
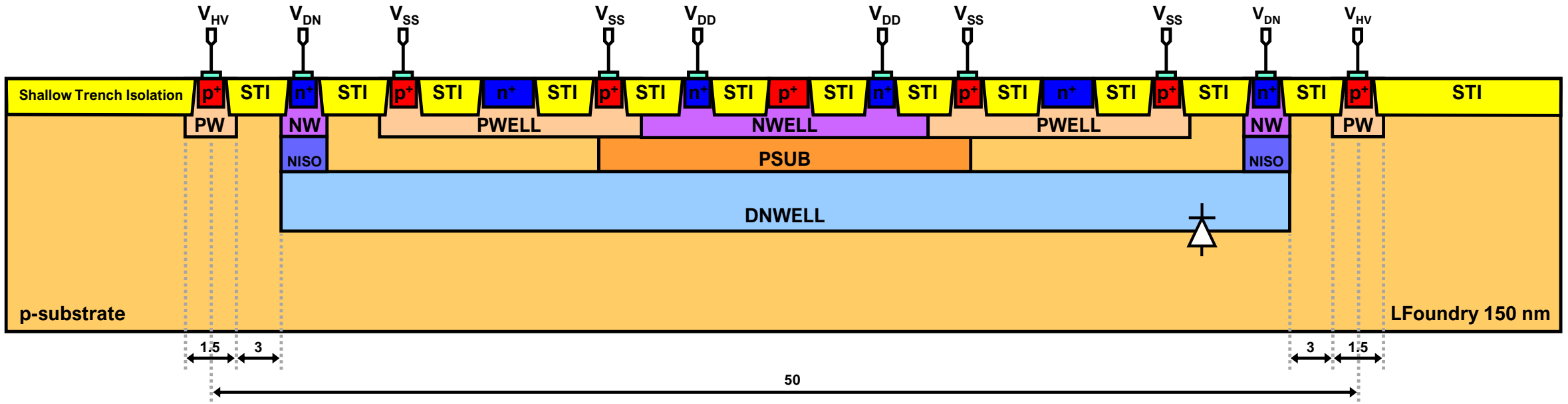


RD50-MPW1 leakage current – What happened?

- The original designers intended to have isolated pixels
- LFoundry adds structures to optimise design file for capabilities of their manufacturing processes



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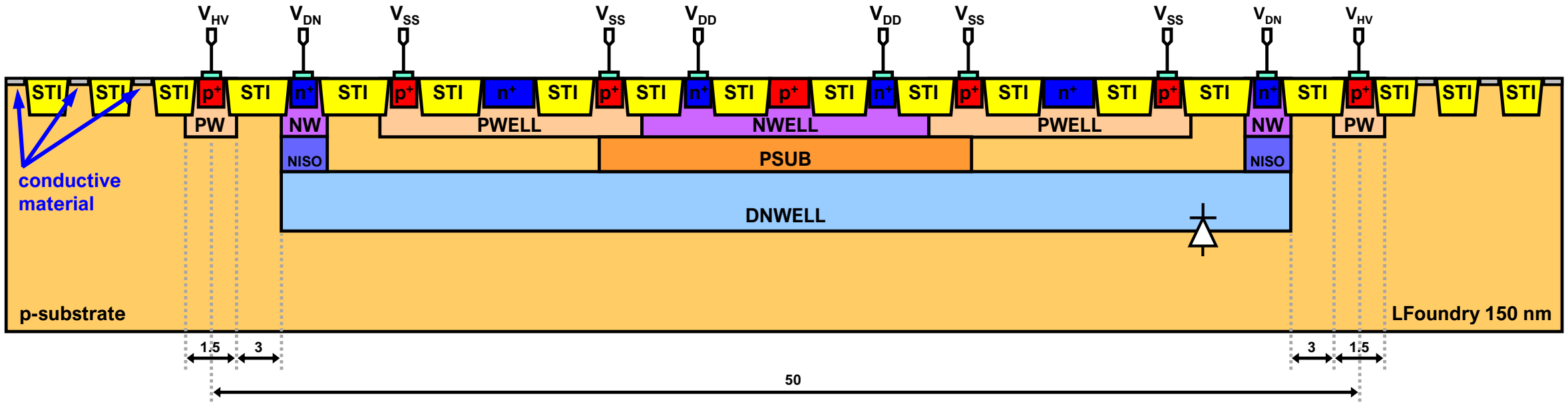

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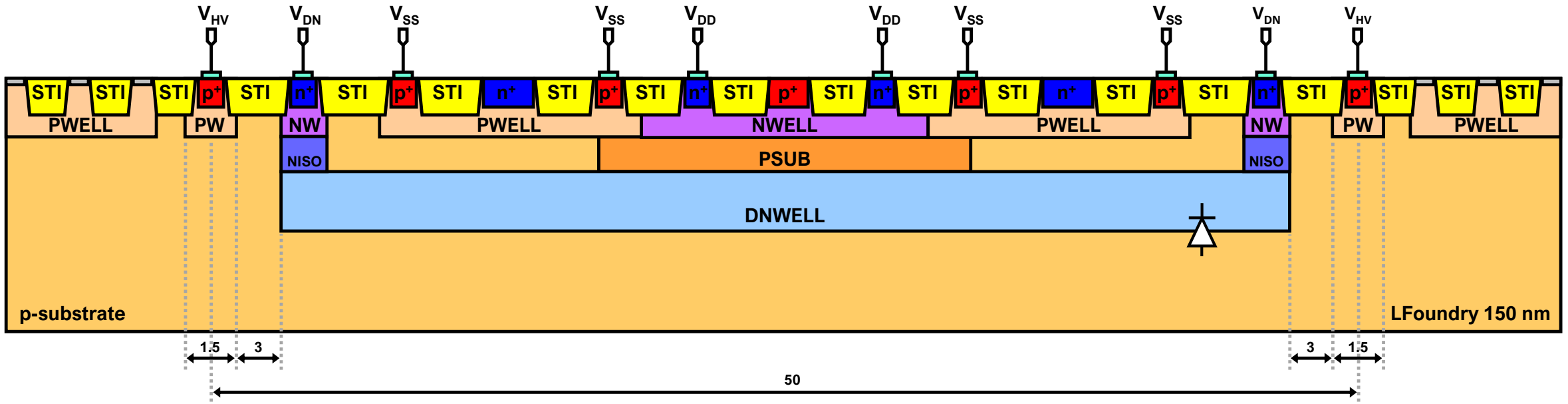
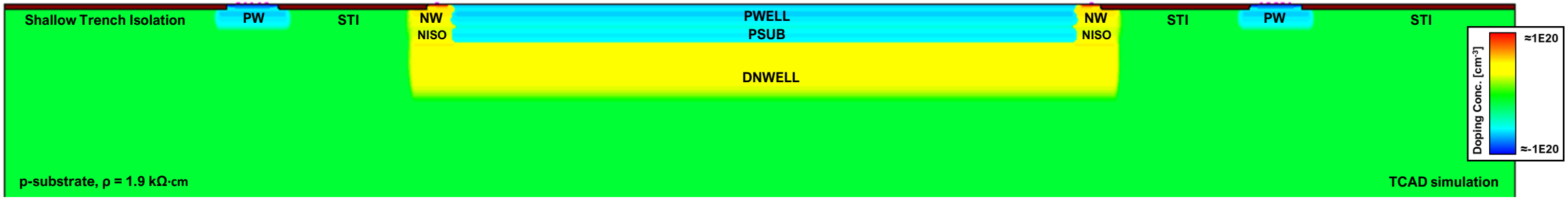
- LFoundry adds structures to optimise design file for capabilities of their manufacturing processes
- LFoundry confirmed process involves conductive material. This is believed to be the source of leakage current
- LFoundry suggested placing conductive material in a PWELL to reduce leakage current

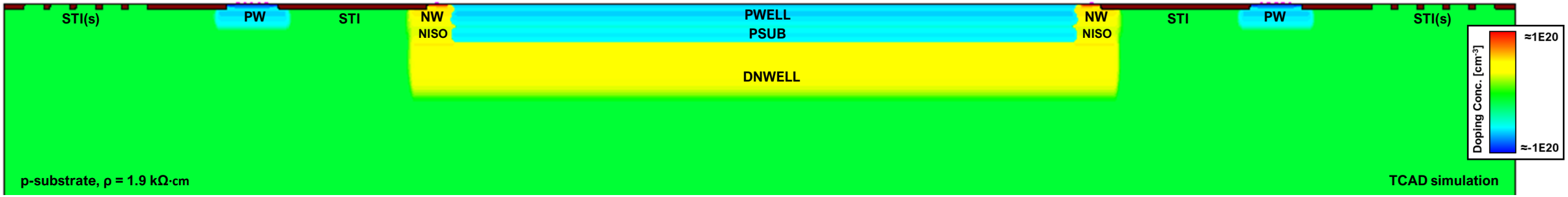


RD50-MPW1 leakage current - pad diode simulations

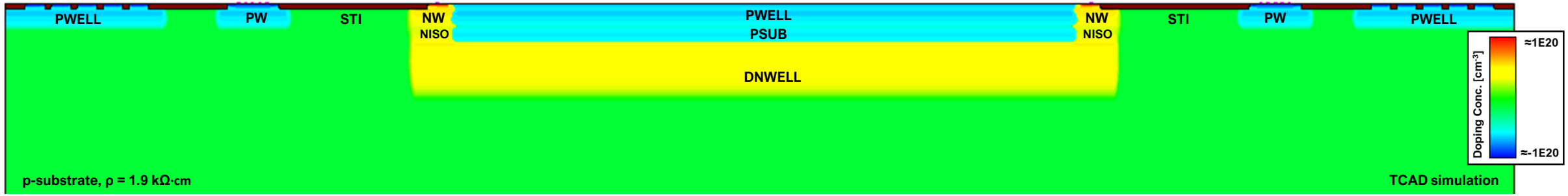
"Ideal"



RD50-MPW1



RD50-MPW2



RD50-MPW1 leakage current - pad diode simulations

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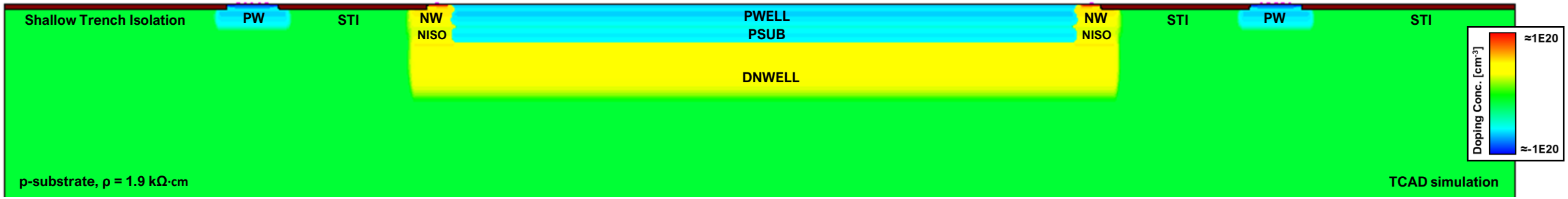
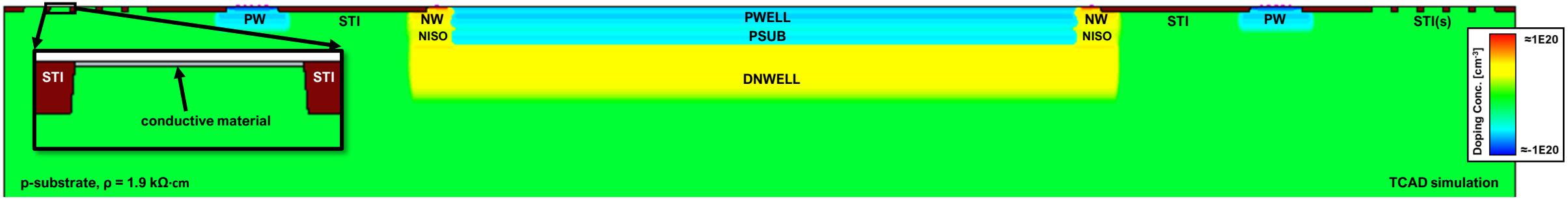
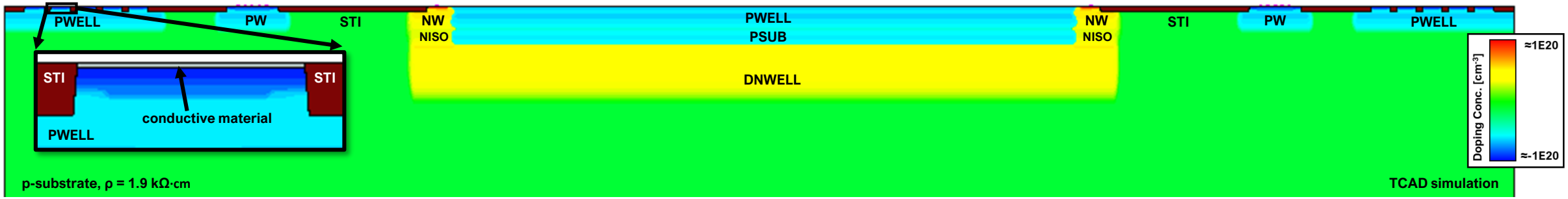


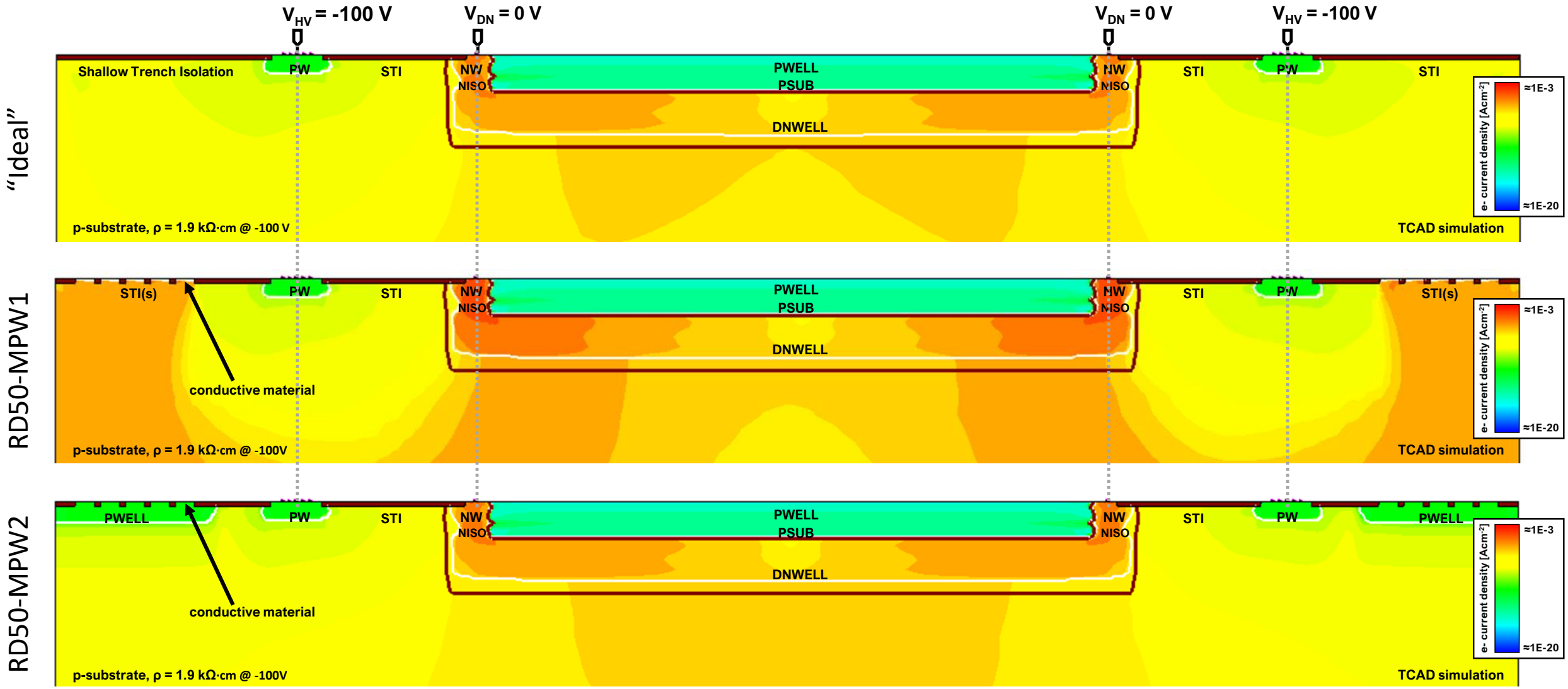
RD50-MPW1



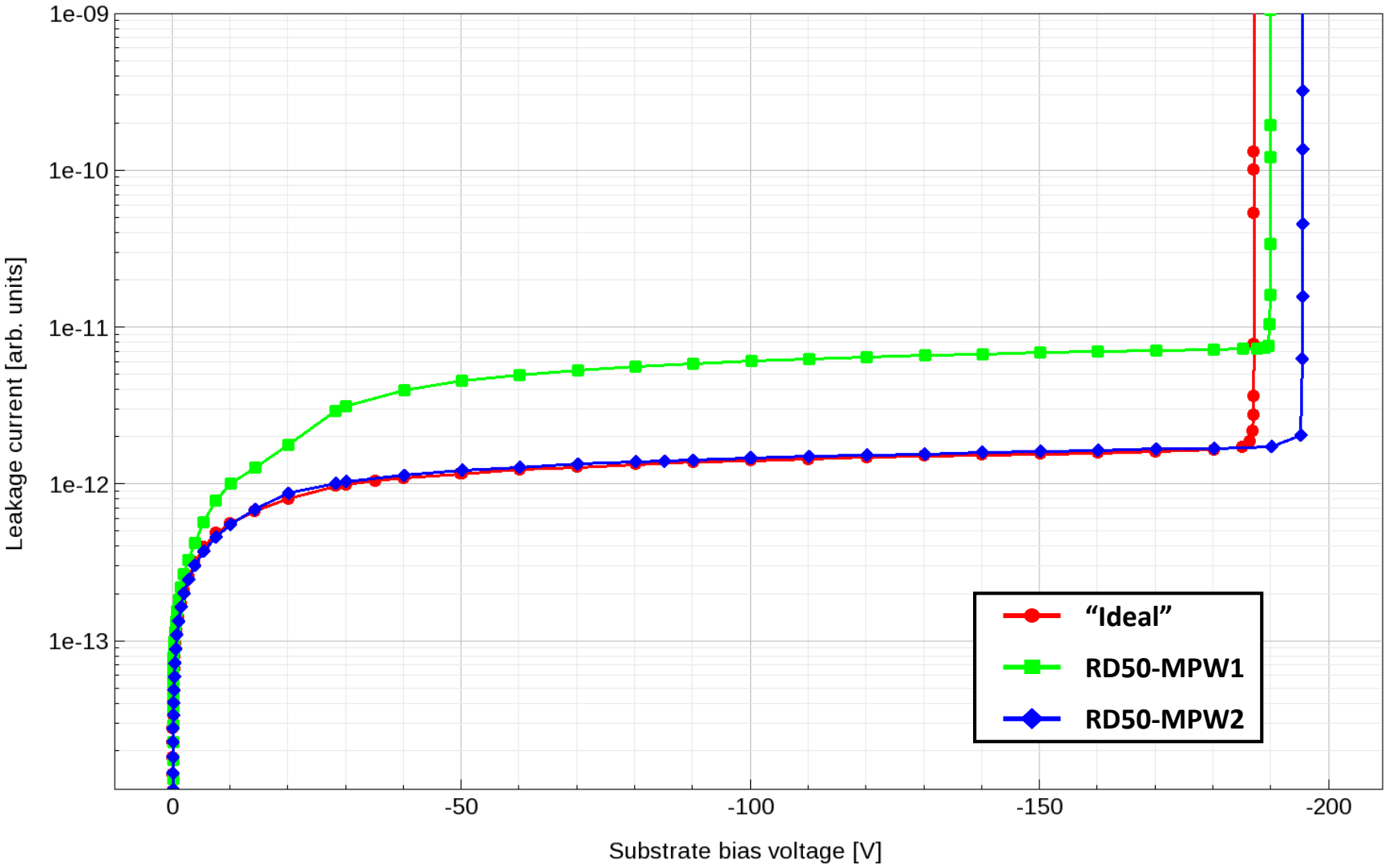
RD50-MPW2



RD50-MPW1 leakage current - pad diode simulations



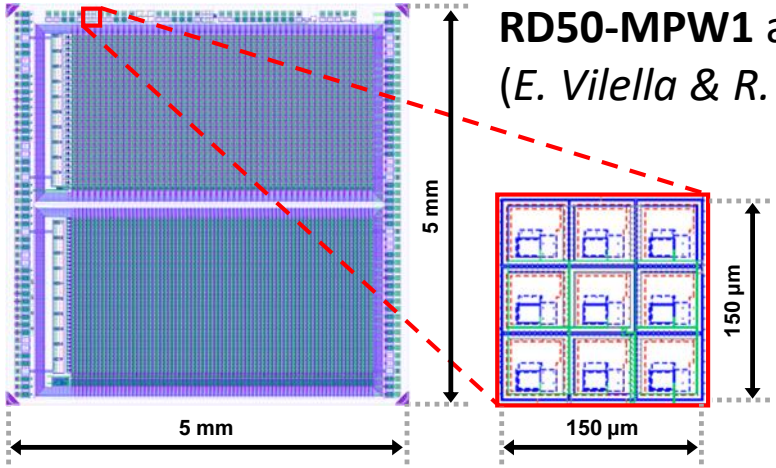
RD50-MPW1 leakage current - pad diode I-V curves



Comparison of I-V curves of the three simulations:

- Increase in I_{LEAK} when conductive material is present on the surface (**RD50-MPW1**)
- I_{LEAK} is reduced when conductive material is placed in PWELL (**RD50-MPW2**)

Contents



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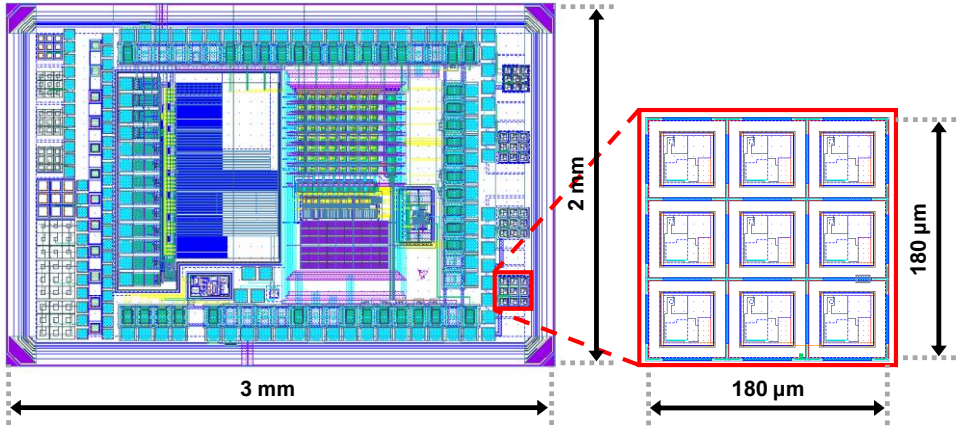
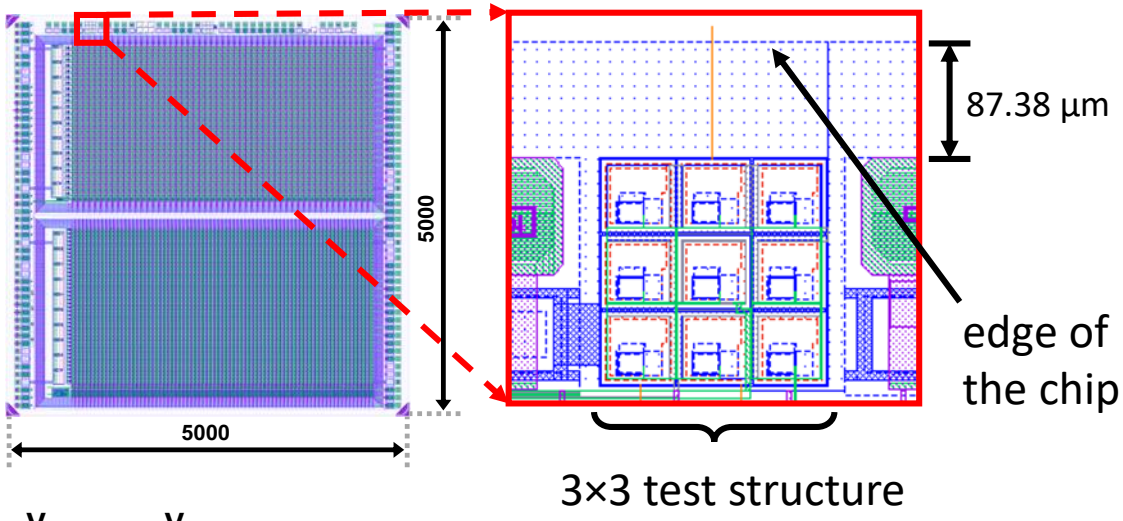
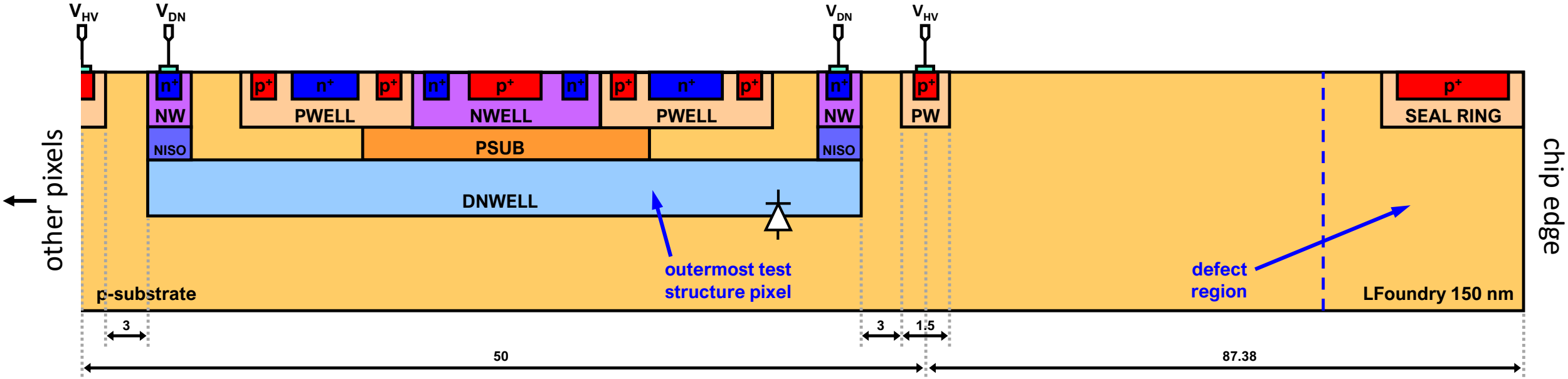


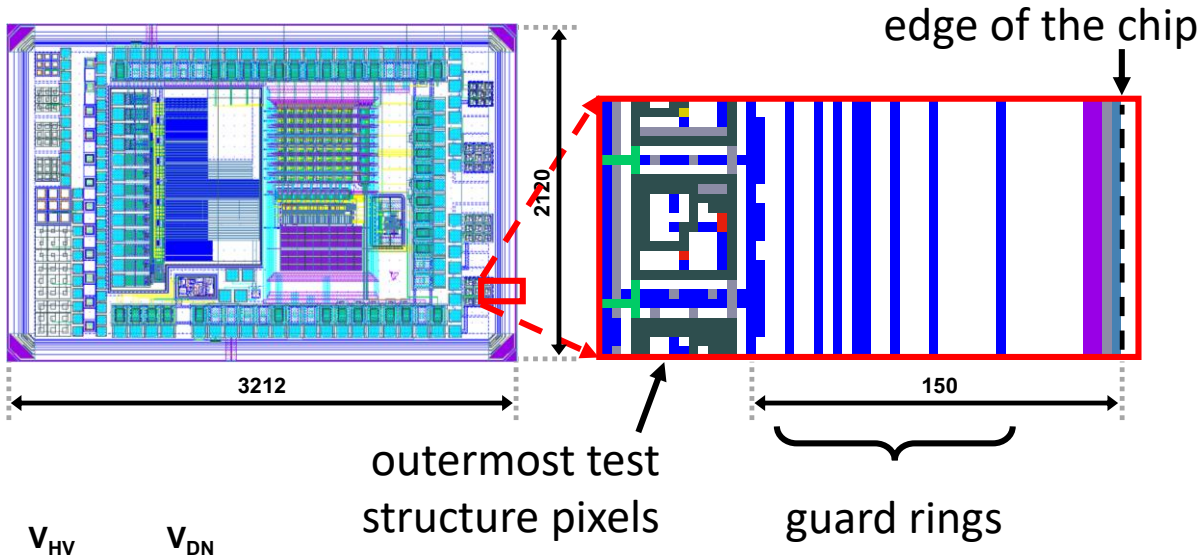
RD50-MPW1 leakage current due to edge defects



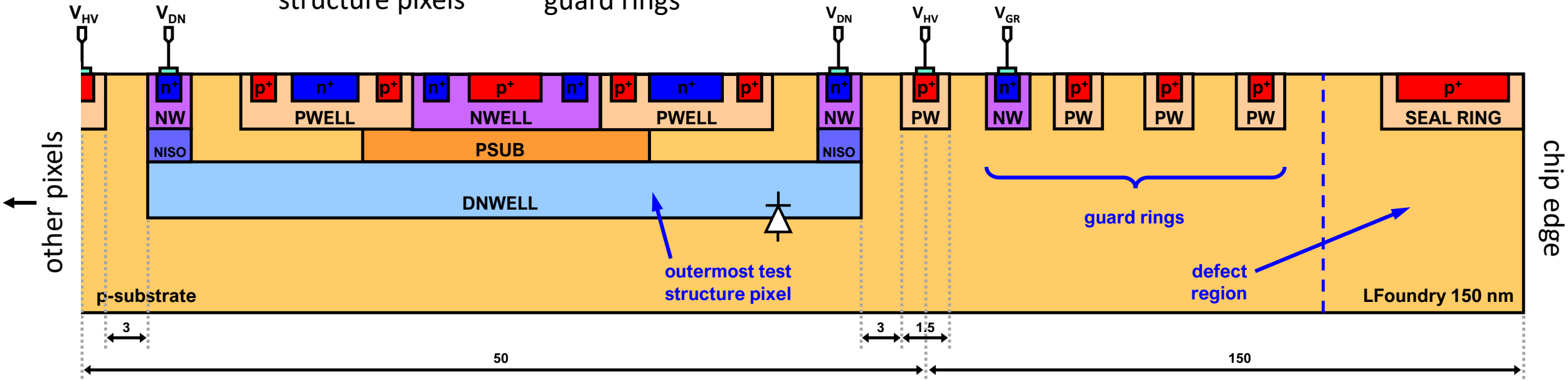
- Test structure lies close to the edge of the device
- Defects in silicon lattice **due to dicing** become significant
- Leakage current increases when pixel depletion region is near defect region



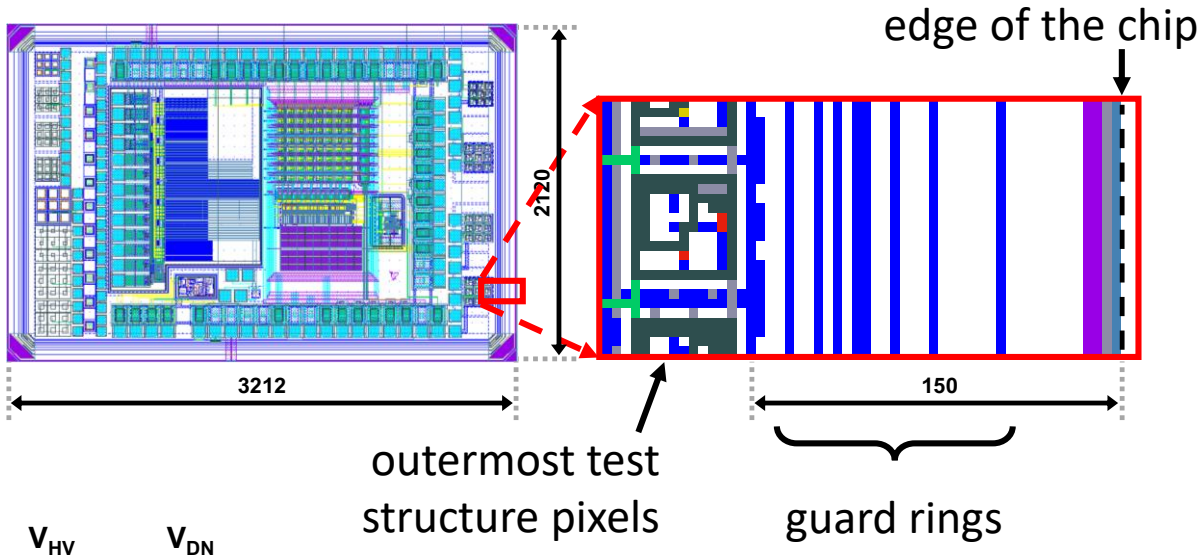
RD50-MPW2 guard rings



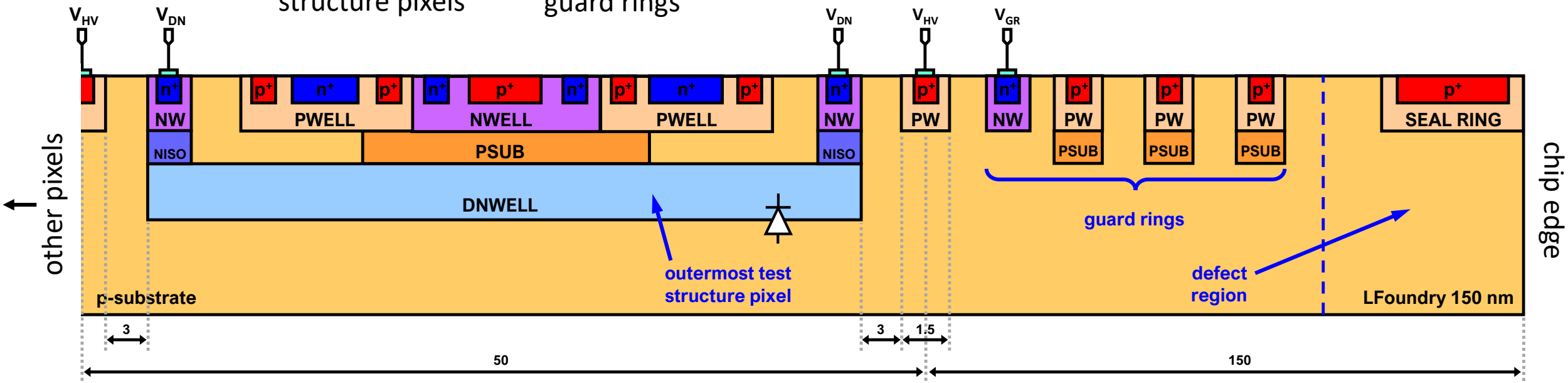
- Leakage current increases when pixel **depletion region** is near defect region
- n-type guard ring added as safeguard to “collect” leakage current
- p-type guard rings can be added to reduce ‘lateral’ **depletion**



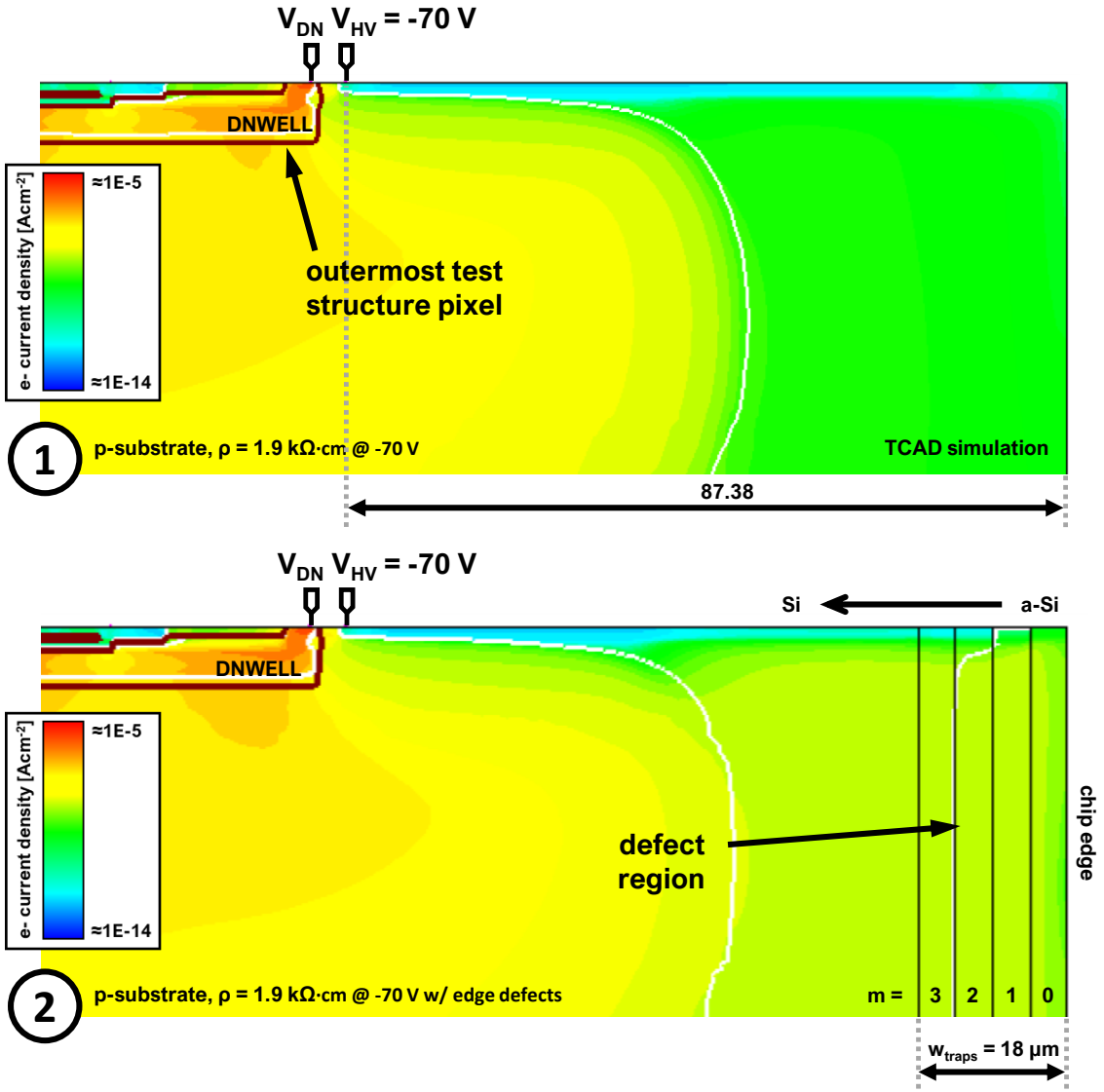
RD50-MPW2 guard rings



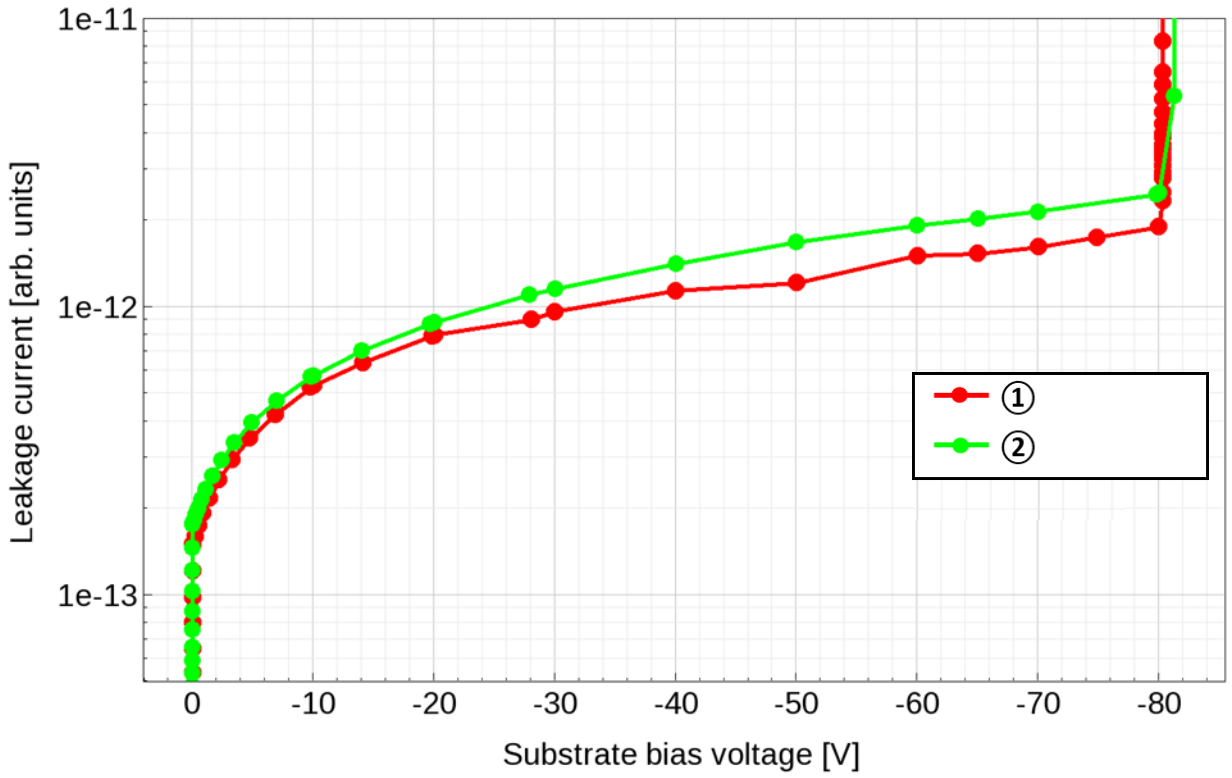
- PSUB layer can be added to further reduce lateral depletion



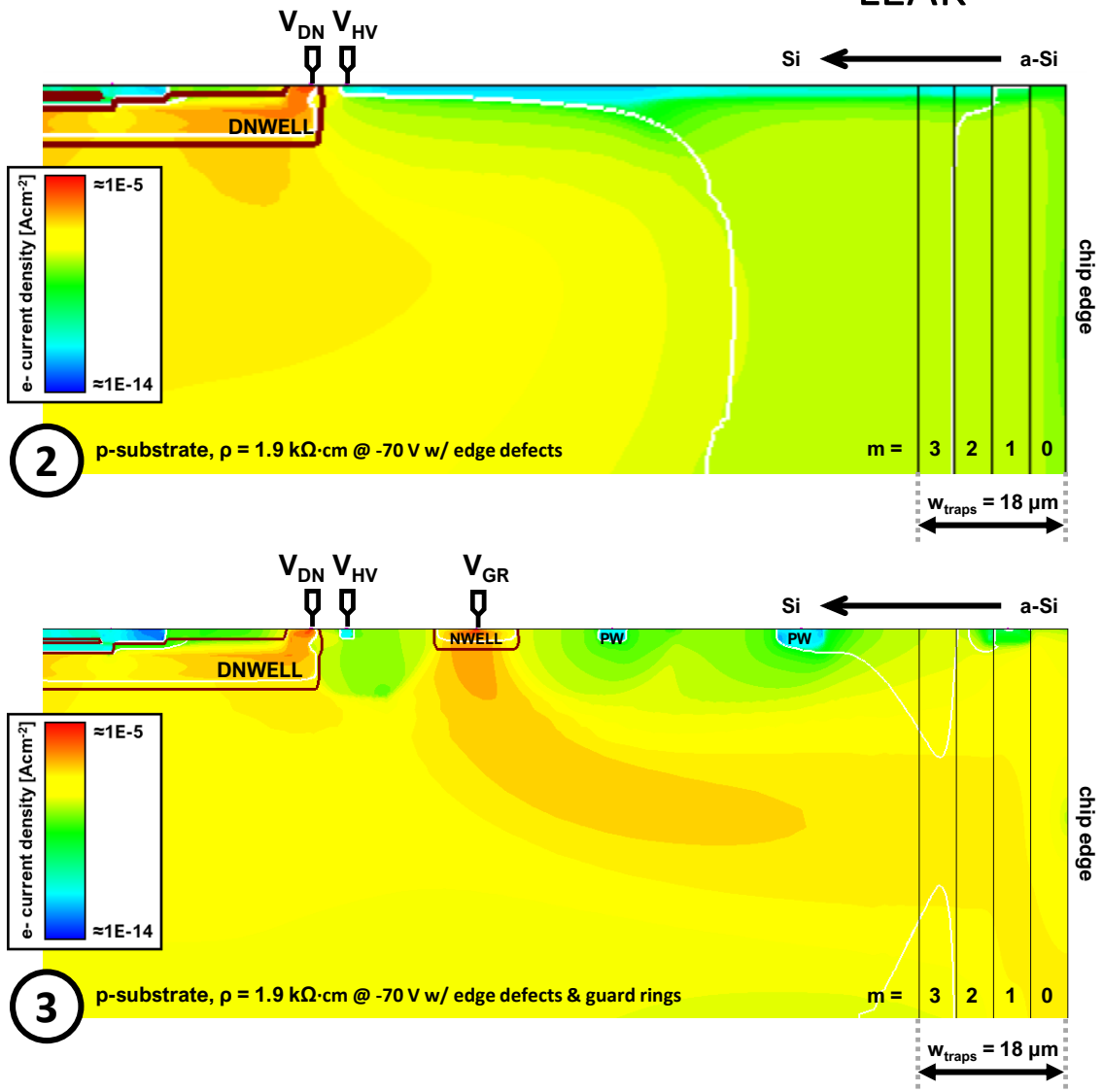
RD50-MPW1 leakage current due to edge defects



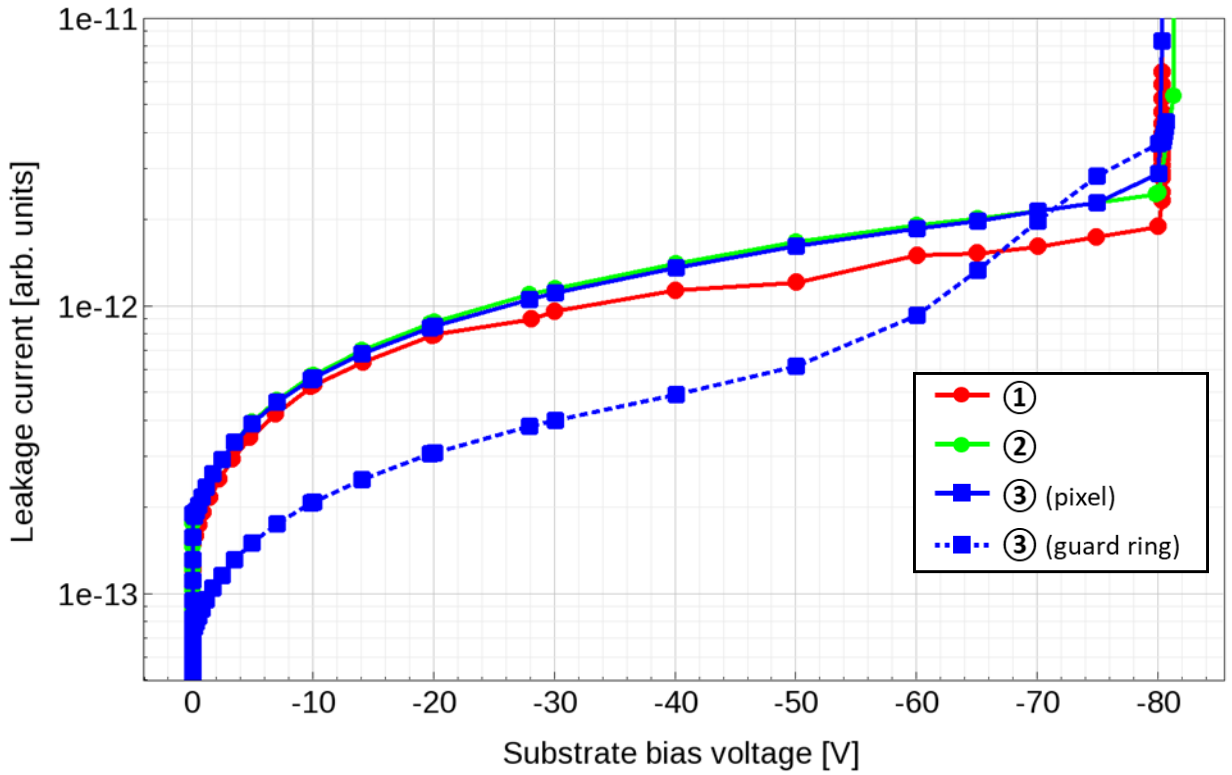
- Two simulations, with and without edge defects (Damage modelled as amorphous silicon (*Noschis et al. 2007*))
- Simulated I_{LEAK} higher when edge defects are present



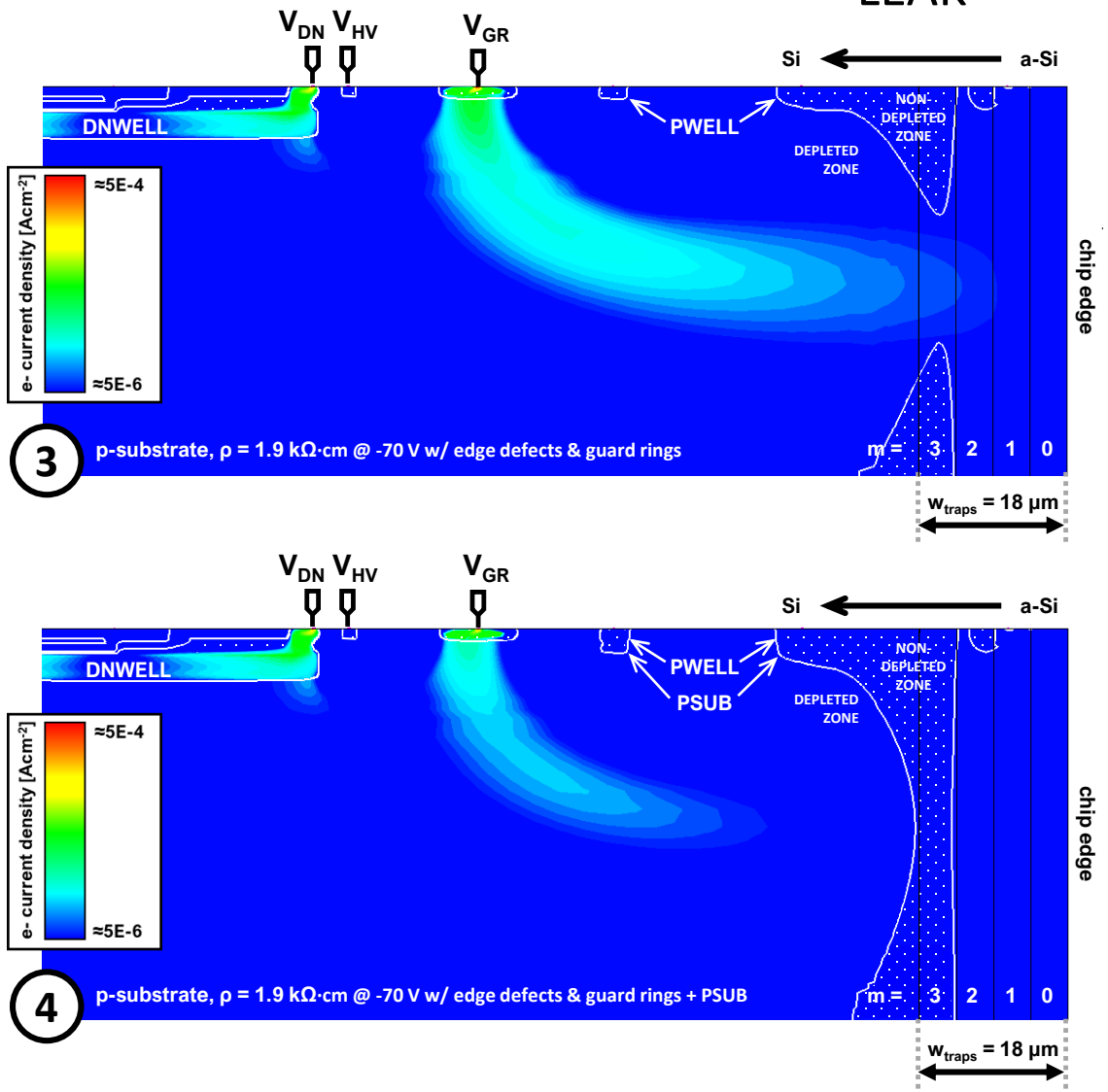
RD50-MPW2 reducing I_{LEAK} due to edge defects with guard rings



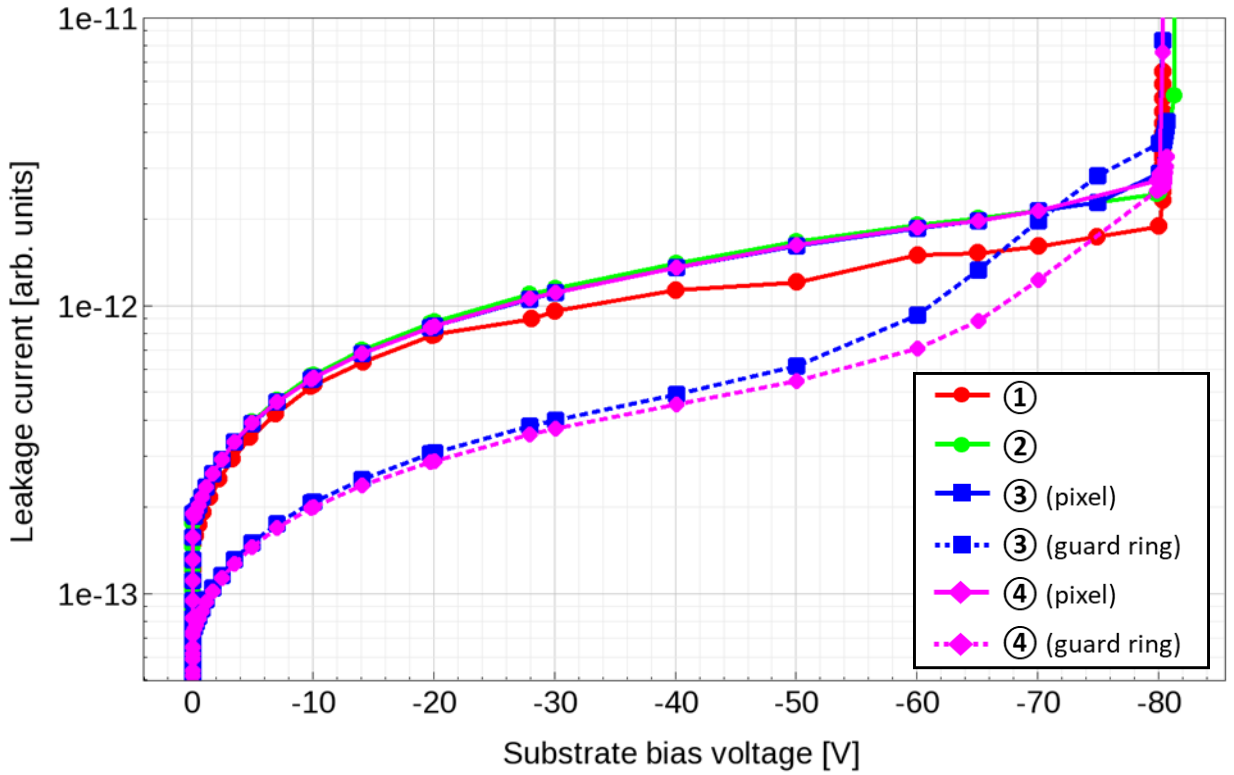
- Similar I_{LEAK} measured at both pixels
- n-type guard ring acts as another diode, increasing lateral depletion into defect region, but collects additional current



RD50-MPW2 reducing I_{LEAK} due to edge defects with guard rings



- Additional deep p-type well PSUB under guard rings reduces lateral depletion
- This reduces simulated I_{LEAK} further



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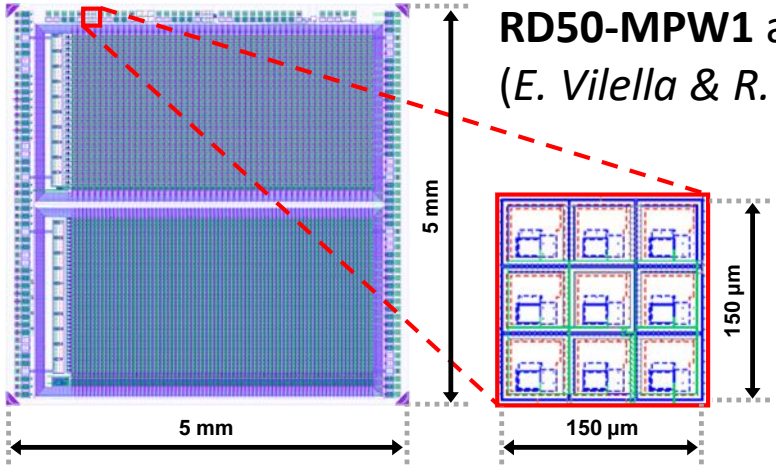

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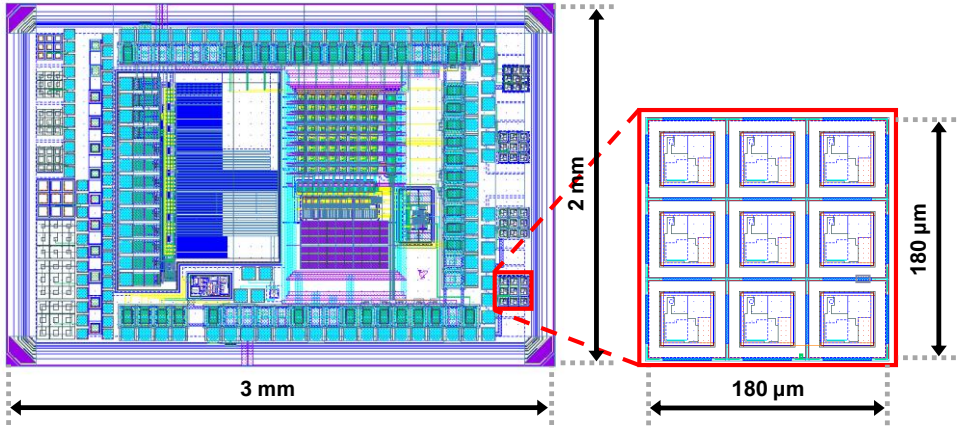
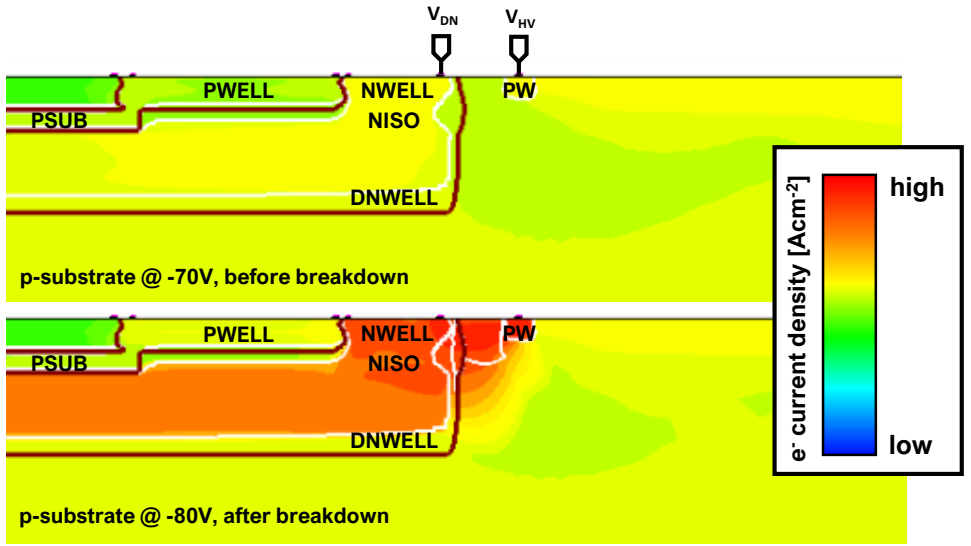
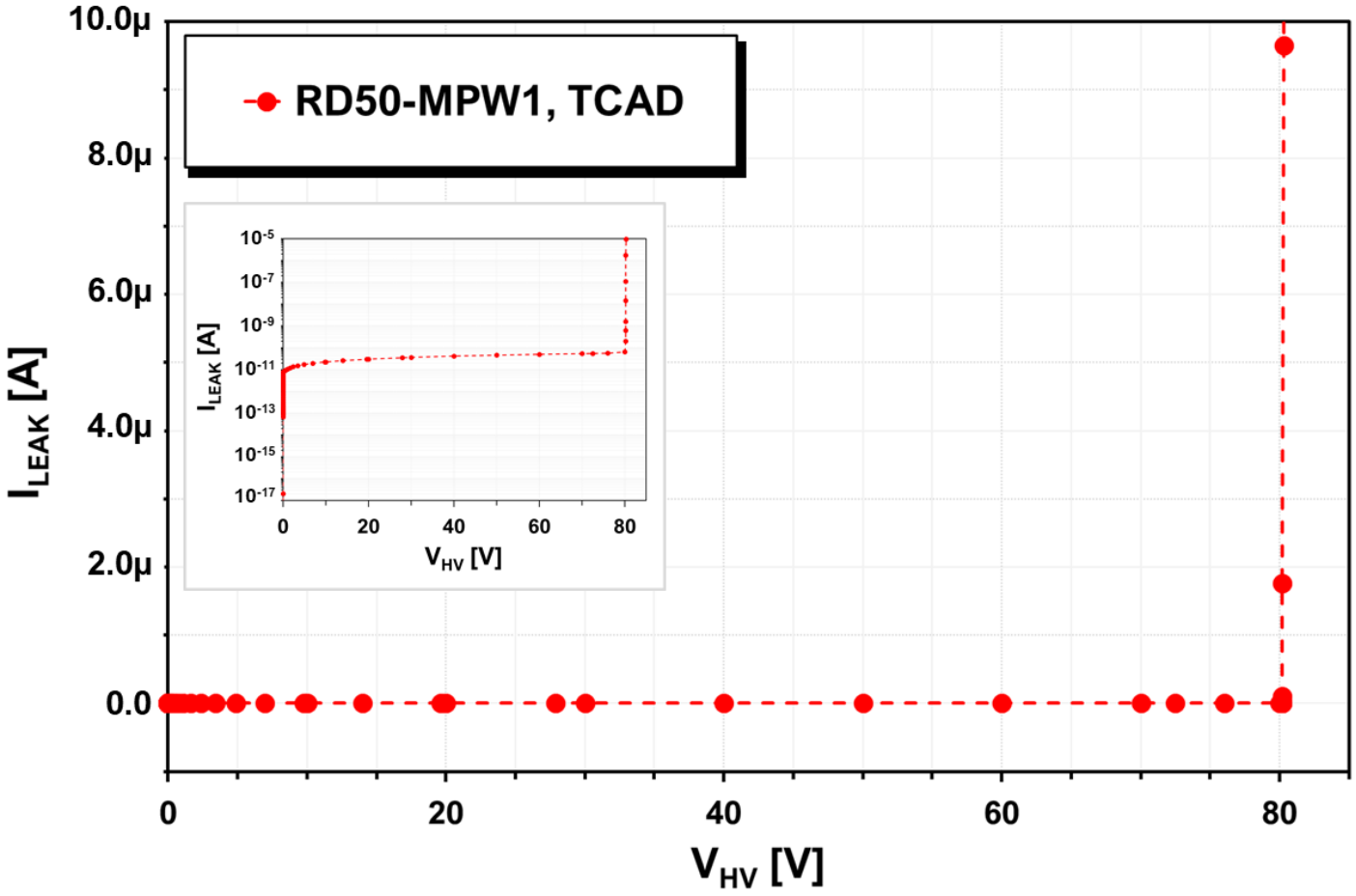


RD50-MPW1 pixel breakdown

- Breakdown simulation
  - $I_{LEAK} \approx 50$ pA pixel^{-1}
  - $V_{BD} \approx -80$ V
- Current flow between diode electrodes (V_{HV} and V_{DN}) at breakdown

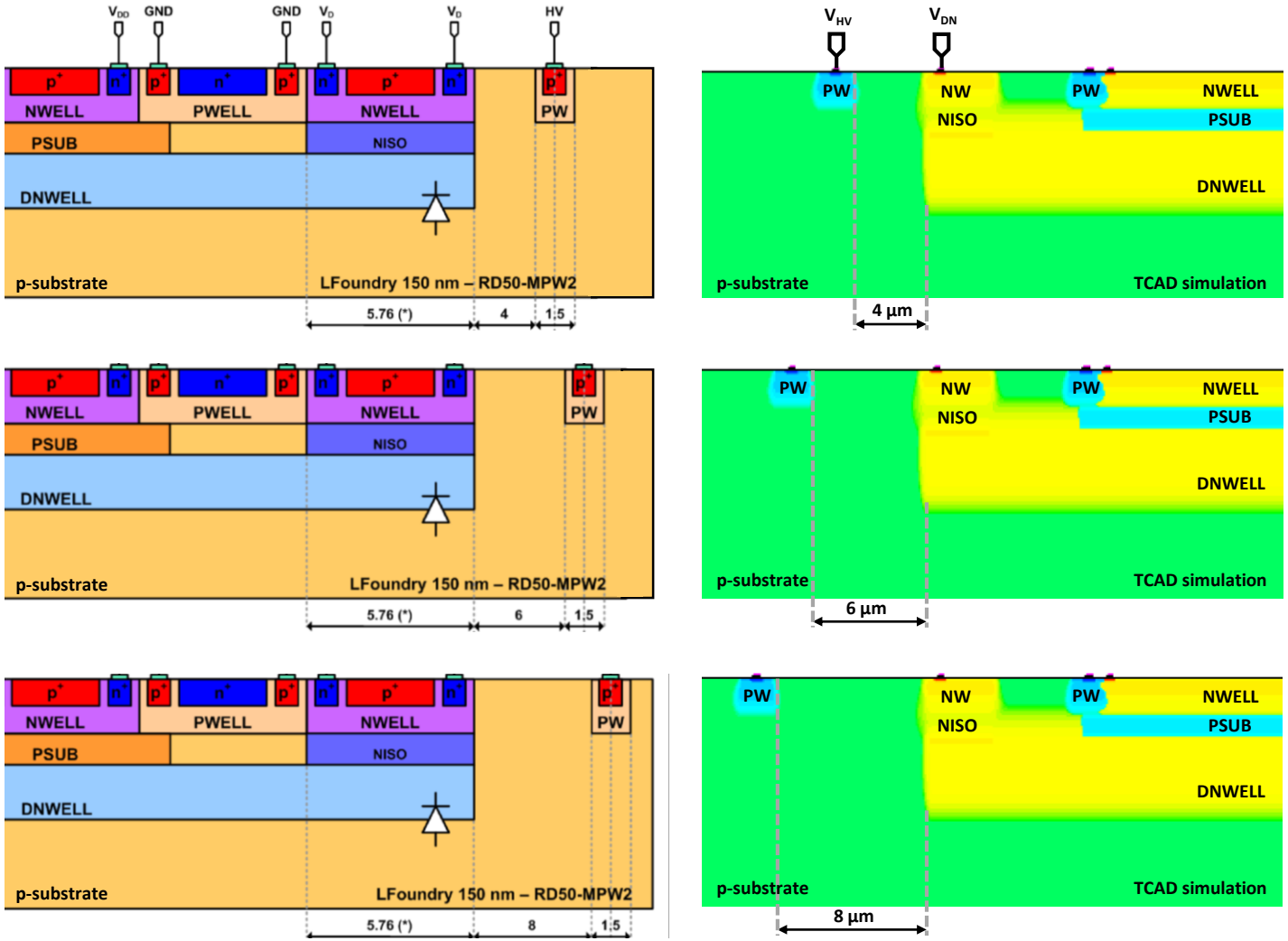




(left-top) current density plot of one pixel before breakdown **(left-bottom)** and after breakdown **(above)** I-V curve of one 2D pixel. Logarithmic scale shown inset

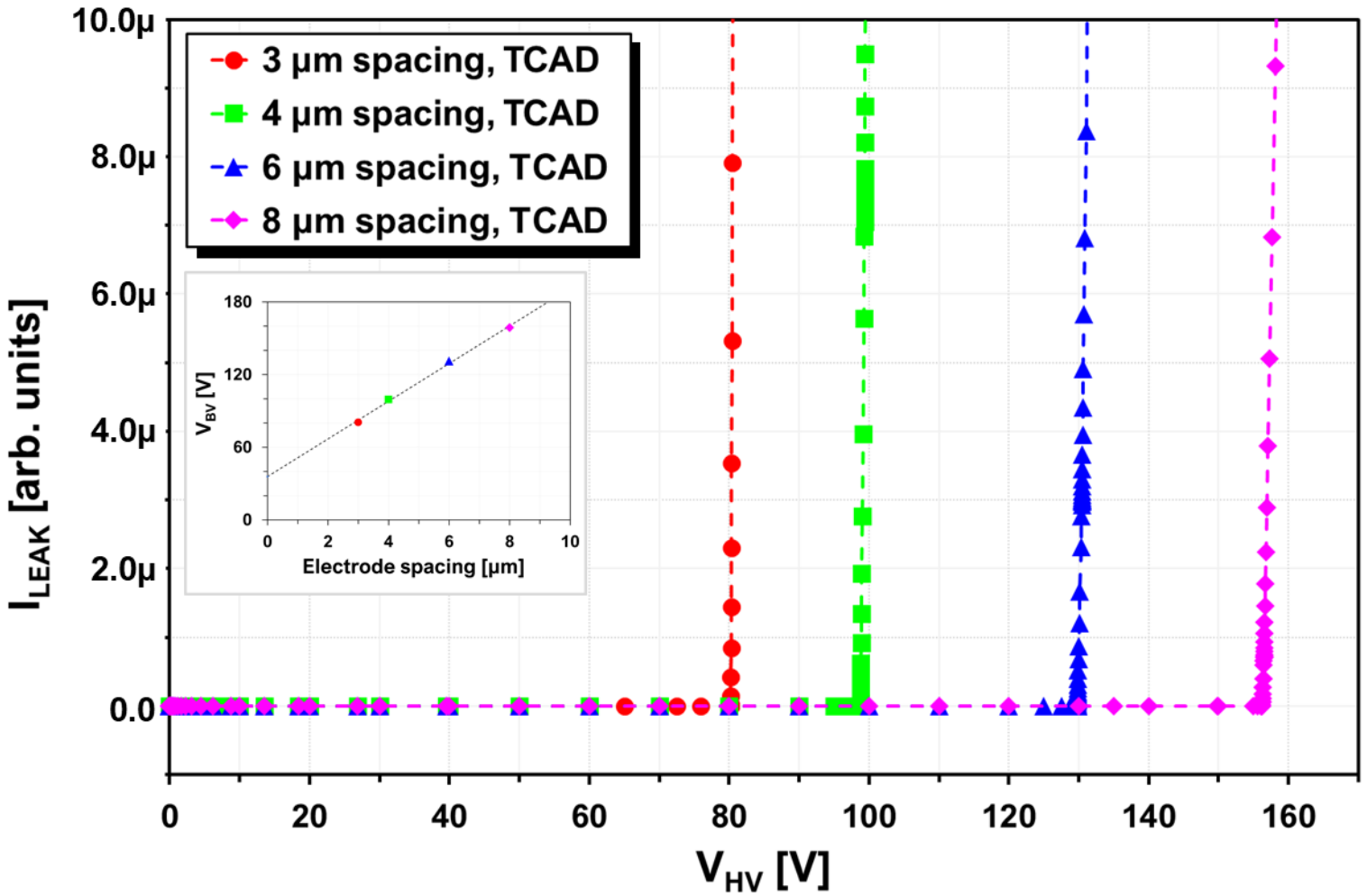
RD50-MPW1 pixel: Electrode spacing

- Spacing between electrodes was increased from 3 µm (in **RD50-MPW1**) to:
  - 4 µm
  - 6 µm
  - 8 µm (in **RD50-MPW2**)
- Same breakdown simulations were performed to compare with 3 µm spacing



(left) E. Vilella, RD50-MPW2 planning presentation **(right)** TCAD simulations investigating the effect of increasing distance between sensing diode electrodes

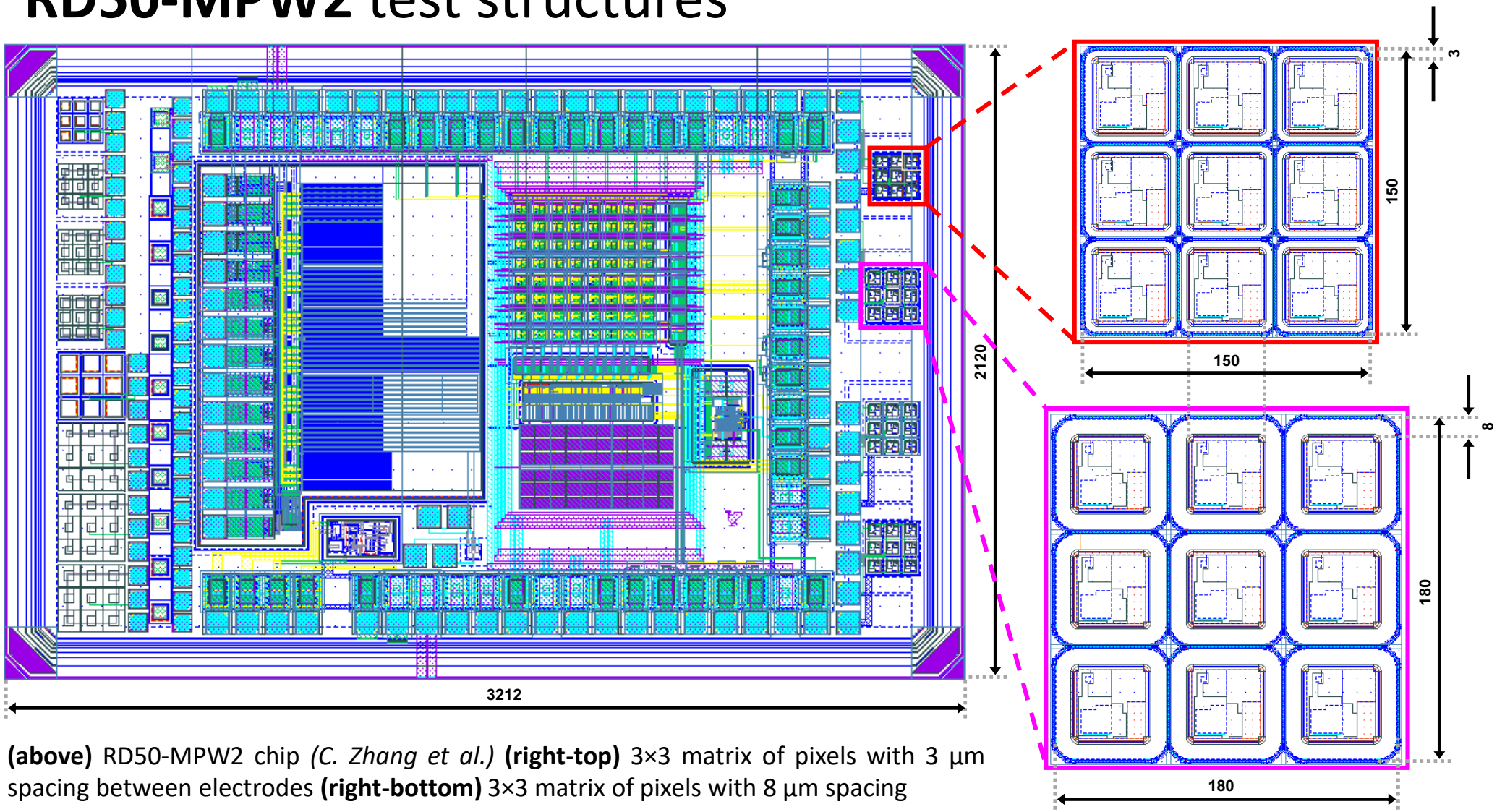
RD50-MPW1 pixel electrode spacing: I-V curves



Comparison of I-V curves of **3 µm**, **4 µm**, **6 µm**, and **8 µm** electrode spacing:

- **3 µm** spacing:
  - $V_{BD} \approx -80$ V
- **4 µm** spacing:
  - $V_{BD} \approx -99$ V
- **6 µm** spacing:
  - $V_{BD} \approx -130$ V
- **8 µm** spacing:
  - $V_{BD} \approx -156$ V

RD50-MPW2 test structures



(above) RD50-MPW2 chip *(C. Zhang et al.)* **(right-top)** 3×3 matrix of pixels with 3 µm spacing between electrodes **(right-bottom)** 3×3 matrix of pixels with 8 µm spacing

3 × 3 matrix of pixels for edge-TCT

- 50 µm × 50 µm pixel area
- **3 µm electrode spacing**
- Rounded corners (see next section)
- No readout electronics

3 × 3 matrix of pixels for edge-TCT

- 60 µm × 60 µm pixel area
- **8 µm electrode spacing**
- Rounded corners (see next section)
- No readout electronics

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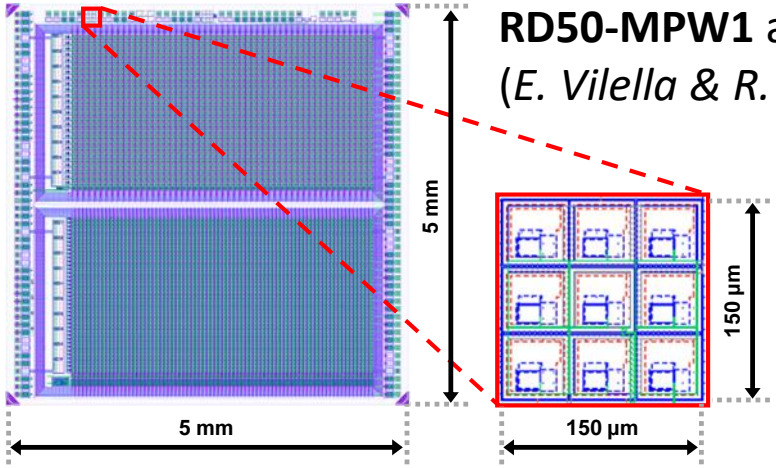

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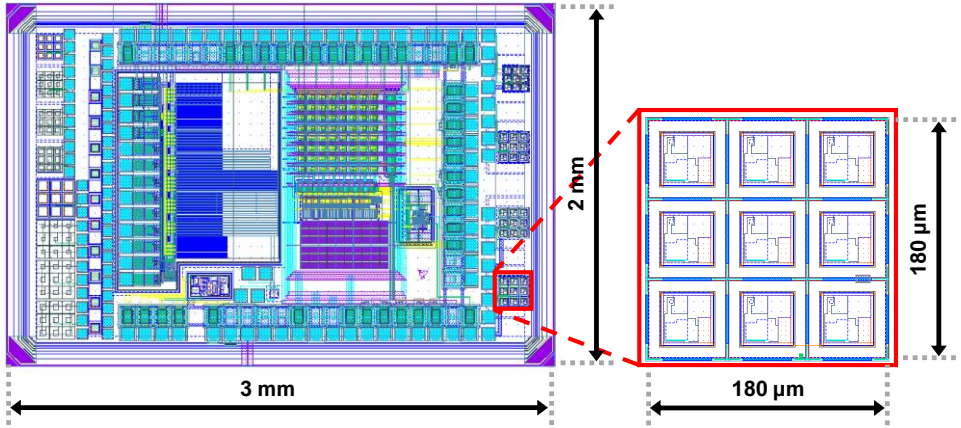
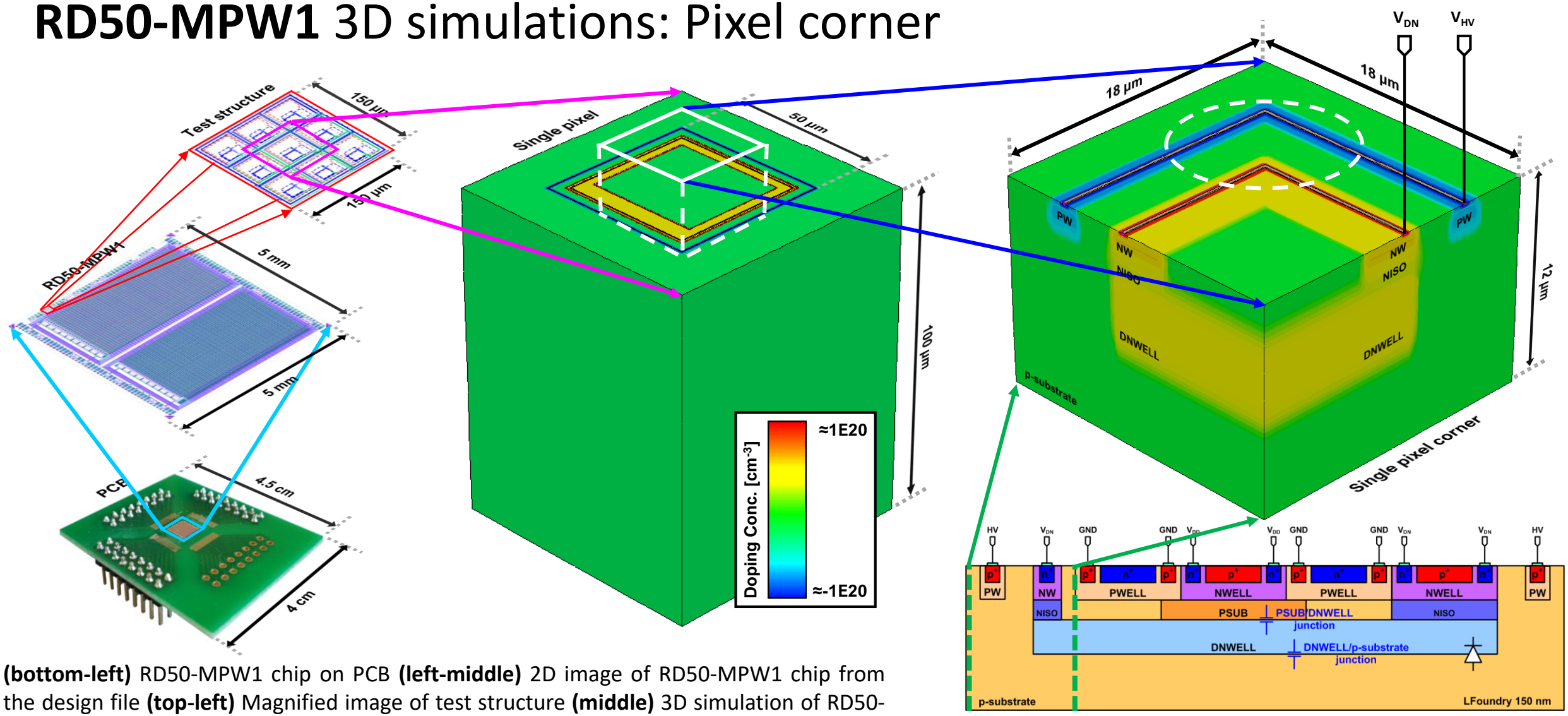


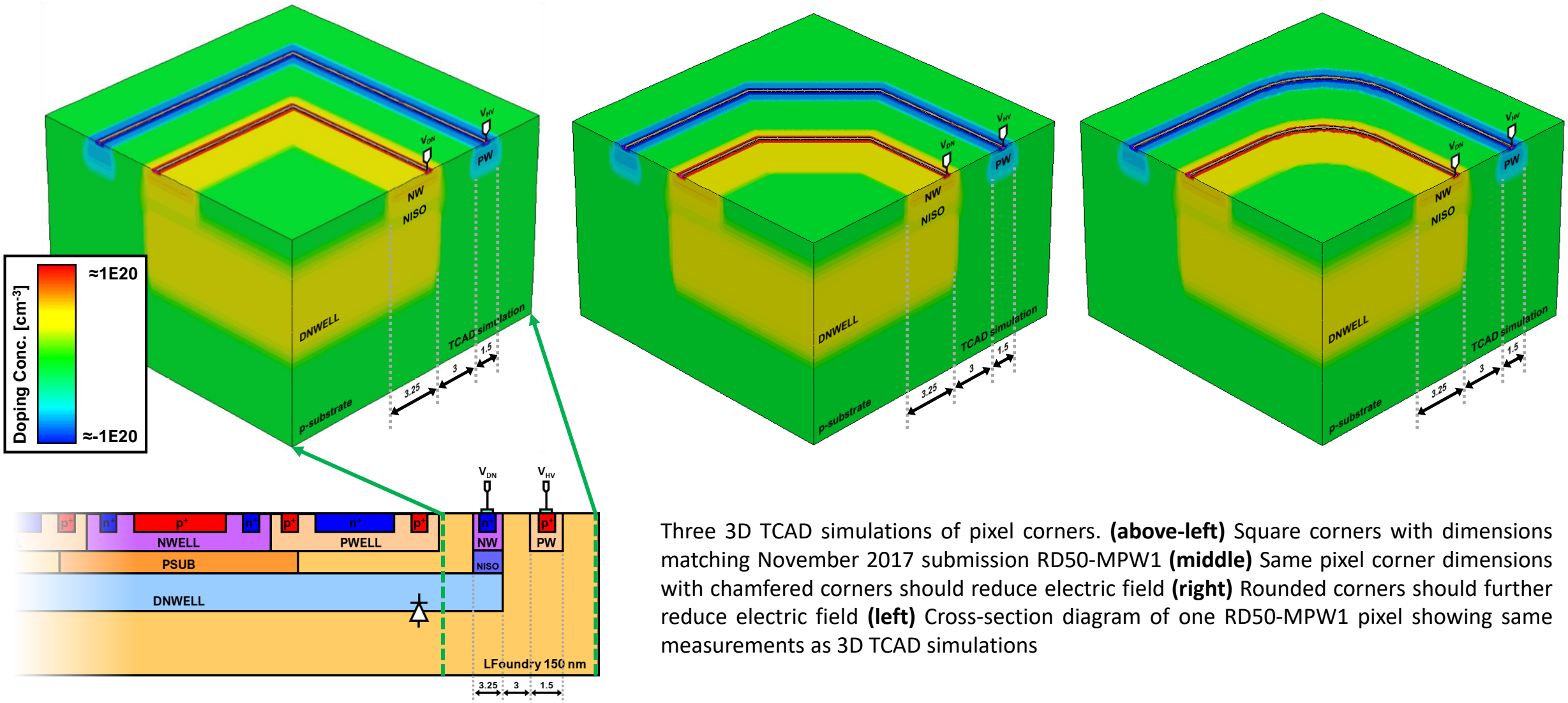
RD50-MPW1 3D simulations: Pixel corner



(bottom-left) RD50-MPW1 chip on PCB **(left-middle)** 2D image of RD50-MPW1 chip from the design file **(top-left)** Magnified image of test structure **(middle)** 3D simulation of RD50-MPW1 pixel. **(top-right)** Smaller 3D simulation of pixel corner **(bottom-right)** Cross-section diagram of RD50-MPW1 pixel

Single pixel cross-section (not to scale)

RD50-MPW2 3D simulations: Corner geometries



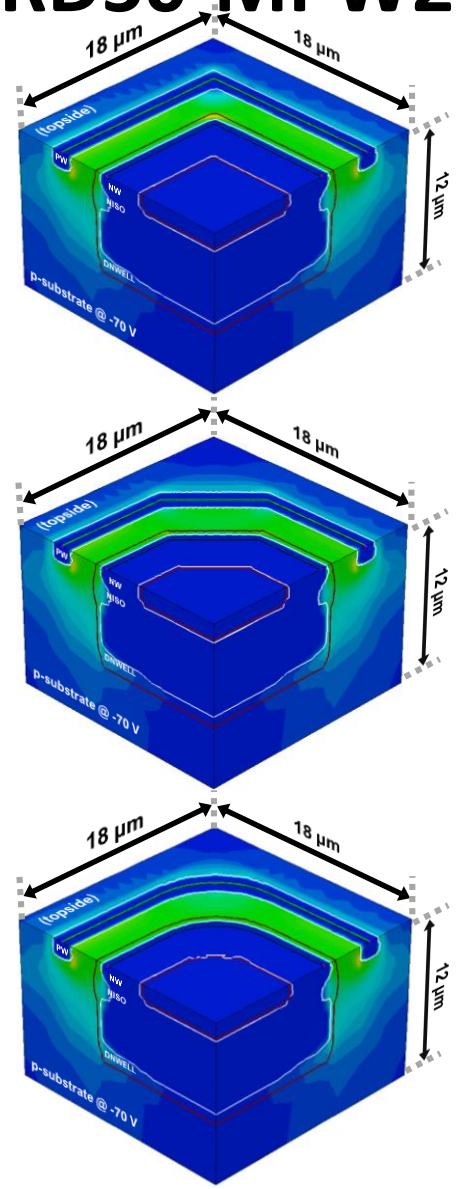
Three 3D TCAD simulations of pixel corners. **(above-left)** Square corners with dimensions matching November 2017 submission RD50-MPW1 **(middle)** Same pixel corner dimensions with chamfered corners should reduce electric field **(right)** Rounded corners should further reduce electric field **(left)** Cross-section diagram of one RD50-MPW1 pixel showing same measurements as 3D TCAD simulations

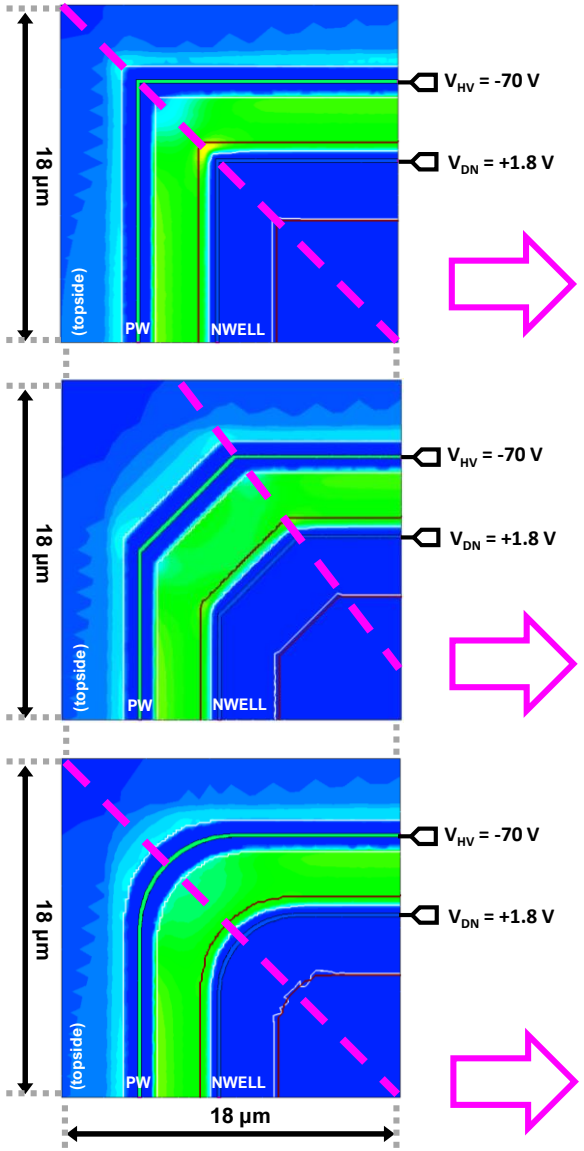
RD50-MPW2 3D simulations: Electric field

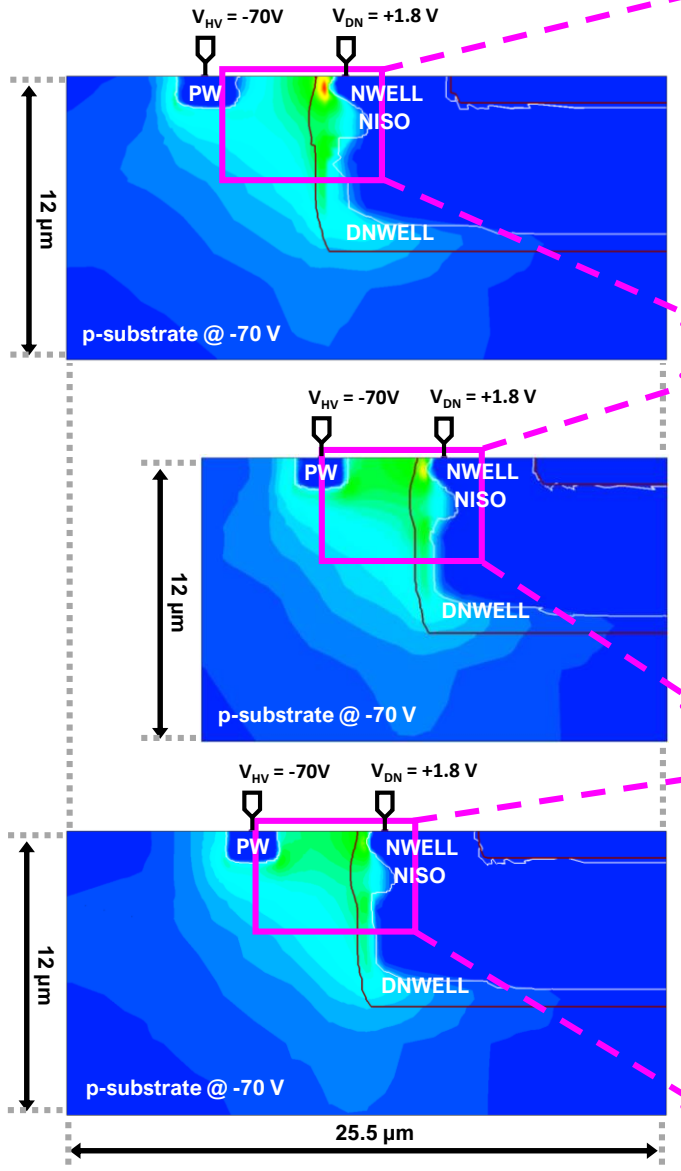
Square

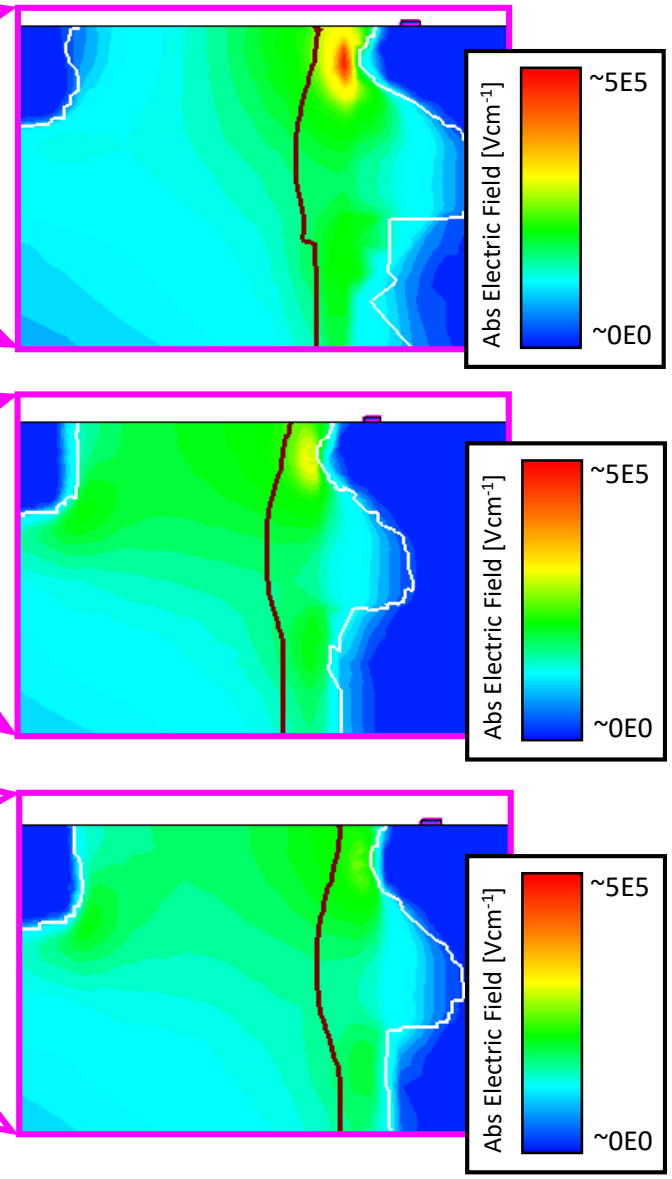
Chamfer

Round









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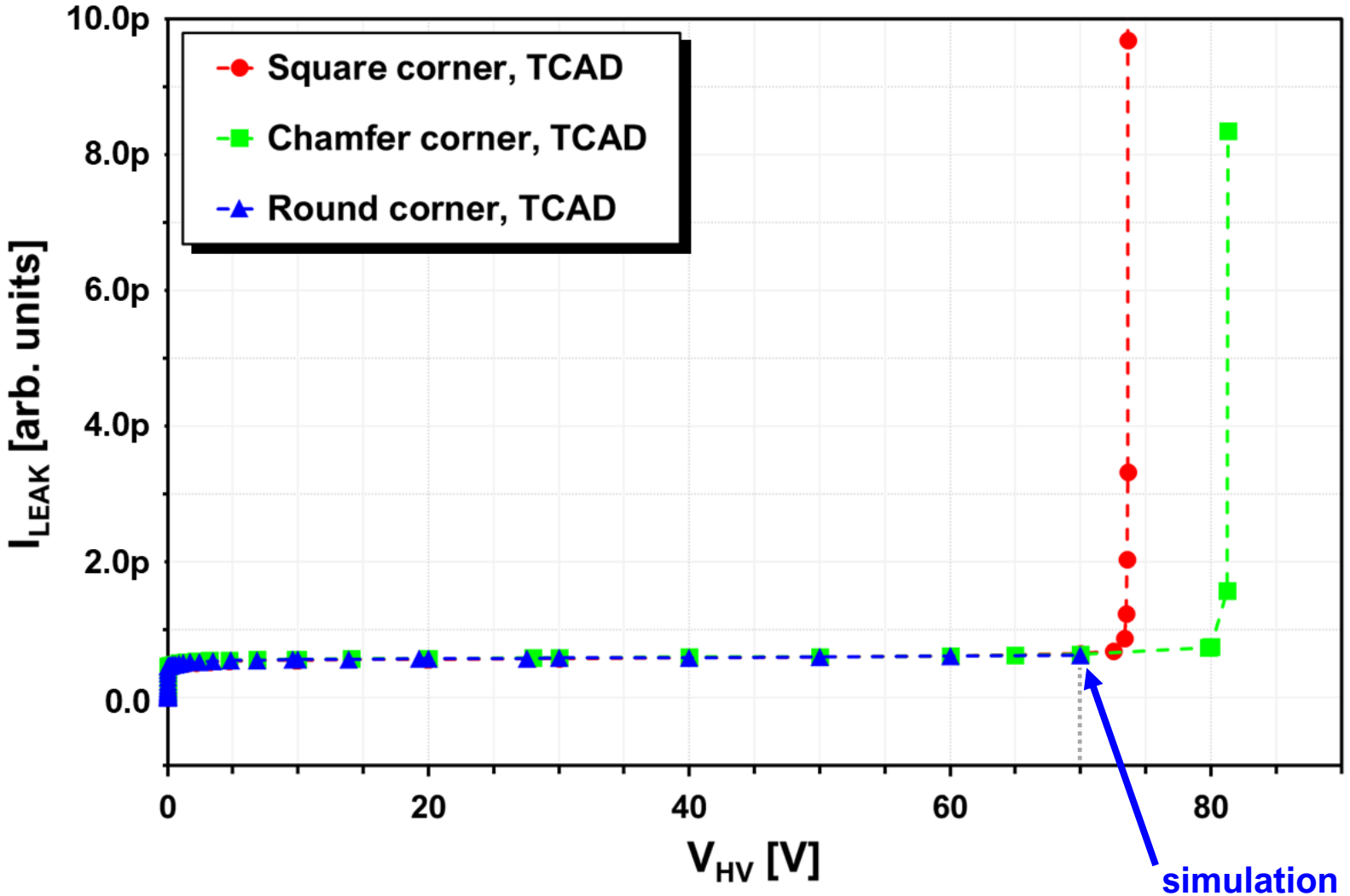
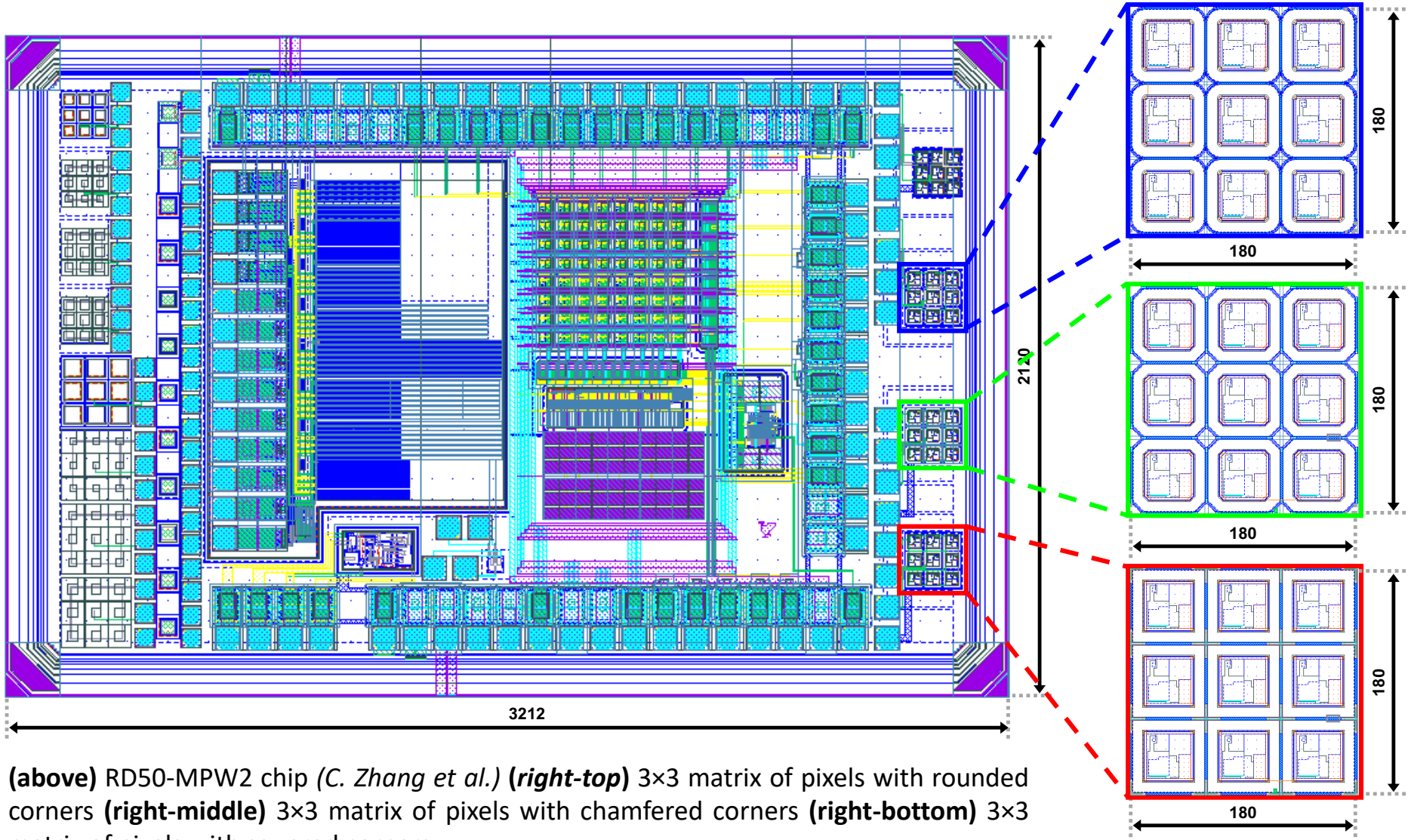
RD50-MPW2 3D simulations: Corner geometries



Comparison of I-V curve of **square**, **chamfer**, and **round** corners:

- **Square** corners:
  - $V_{BD} \approx -70V$
- **Chamfer** corners:
  - $V_{BD} \approx -80V$
- **Round** corners:
  - $V_{BD} \approx$ **?**

RD50-MPW2 test structures



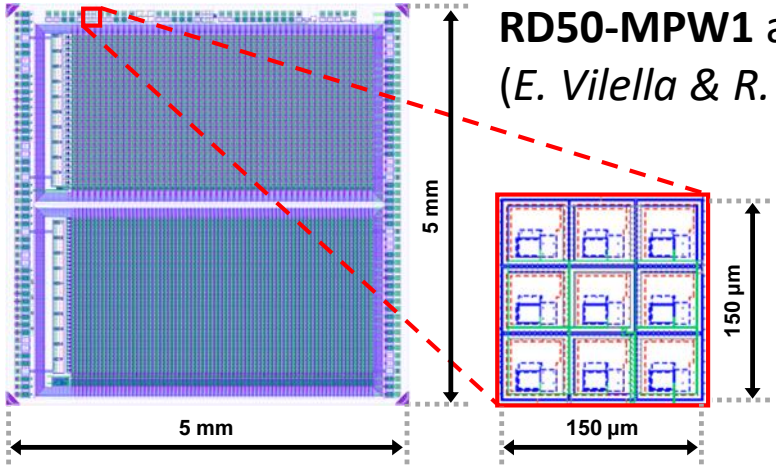
(above) RD50-MPW2 chip *(C. Zhang et al.)* **(*right-top*)** 3×3 matrix of pixels with rounded corners **(right-middle)** 3×3 matrix of pixels with chamfered corners **(right-bottom)** 3×3 matrix of pixels with squared corners

3 × 3 matrix of pixels for edge-TCT
- 60 µm × 60 µm pixel area
- 8 µm electrode spacing
- **Rounded corners**
- No readout electronics

3 × 3 matrix of pixels for edge-TCT
- 60 µm × 60 µm pixel area
- 8 µm electrode spacing
- **Chamfered corners**
- No readout electronics

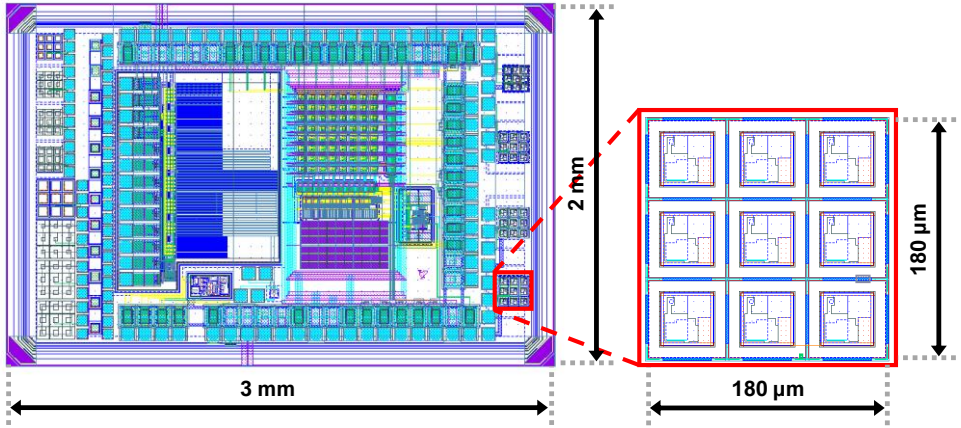
3 × 3 matrix of pixels for edge-TCT
- 60 µm × 60 µm pixel area
- 8 µm electrode spacing
- **Squared corners**
- No readout electronics

Contents



RD50-MPW1 and test structure (*E. Vilella & R. Casanova*)

RD50-MPW2 and test structure (*C. Zhang,* et al.)



RD50-MPW2 future plans

- General
  - We expect fabricated chips sometime in **July 2019**
  - Test areas to be prepared at FBK and UoL while we wait
- Extensive test structure measurements (for ρ = 10, 100, 1900, 3000 Ω·cm)
  - **Irradiation** campaign (already planned with Institut Jožef Stefan in Ljubljana, to fluences Φ up to 2E16 $n_{eq} \cdot cm^{-2}$)
  - **I-V**s for all ρ's and Φ's (for extracting V_{BD}, I_{LEAK})
  - **edge-TCT** measurements for all ρ's and Φ's (to extract depletion depth W_D)
- More measurements (see yesterday's talk by C. Zhang)
  - Bias block functionality
  - Output of the analog readout (SFOUT)
  - Output of the comparator (COMPOUT)
  - Matrix power consumption

Summary

Work is part of R&D into HV-CMOS devices in particle physics experiments

Leakage current (I_{LEAK}) studies

- Post-processing (Measurements of **RD50-MPW1** devices show high I_{LEAK})
  - TCAD simulations of LFoundry post-processing filling layers show high I_{LEAK} (**RD50-MPW1**)
  - TCAD simulations of filling layers in PWELLs reduces I_{LEAK} (**RD50-MPW2**)
- Edge defects
  - TCAD simulations of edge defects show increased I_{LEAK} (**RD50-MPW1**)
  - TCAD simulations with guard rings show reduced current at pixel (**RD50-MPW2**)

Breakdown voltage (V_{BD}) TCAD simulations

- Electrode spacing
  - Increasing the spacing between diode electrodes increases V_{BD}
- Corner geometry
  - Rounding corners of DNWELL increases V_{BD}

14th Trento Workshop on Advanced Silicon Radiation Detectors

25th – 27th February 2019

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Thank you

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Edge defect model (Noschis et al. 2007)

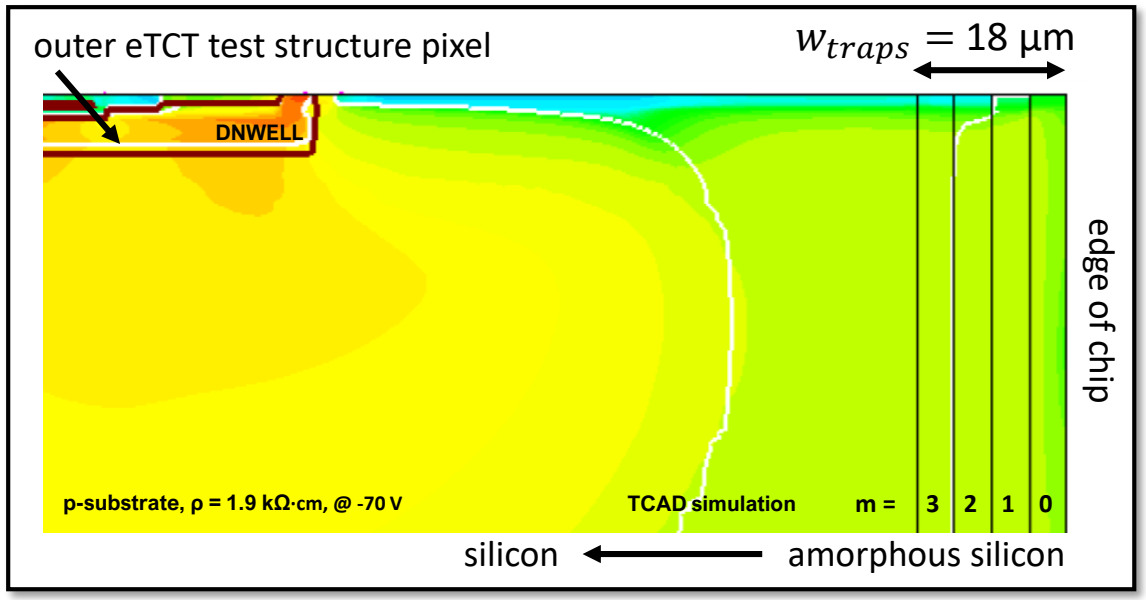

Figure: *(above)* "Noschis method" implemented into RD50-MPW1 geometry

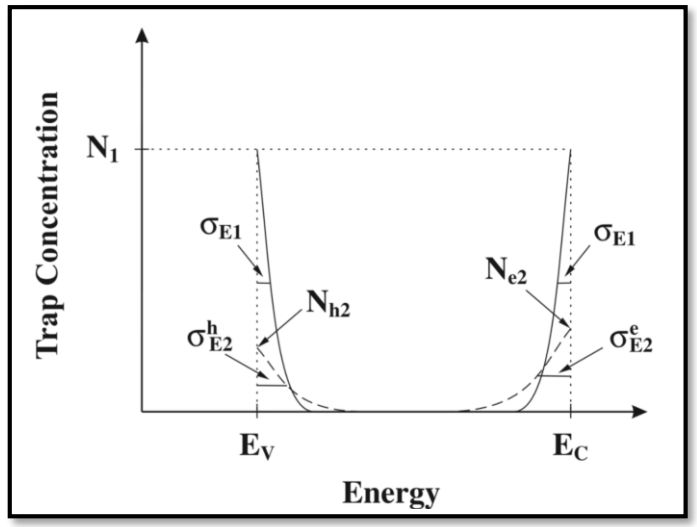

Figure: Energy spectrum for traps in bandgap of amorphous silicon (Noschis, E. et al. 2007)

Parameter	Value
$(N_1)_0$	10^{21}cm^{-3}eV^{-1}
$(N_{e2})_0$	4×10^{16}cm^{-3}eV^{-1}
$(N_{h2})_0$	0.25×10^{16}cm^{-3}eV^{-1}
σ_{E1}	0.035 eV
σ^e_{E2}	0.1 eV
σ^h_{E2}	0.08 eV
w_{traps}	18 µm

Table: Parameters (Noschis, E. et al. 2007)

Type	Trap conc. (cm^{-3}eV^{-1})
Acceptor	10^{21}
Acceptor	4×10^{16}
Donor	10^{21}
Donor	0.25×10^{16}

Table: *(left)* Four trap levels modelled in Sentaurus TCAD

$$f_t(E) = N_1 e^{-\left|\frac{(E-E_V)}{\sigma_{E1}}\right|} + N_1 e^{-\left|\frac{(E-E_C)}{\sigma_{E1}}\right|} + N_{e2}\, e^{-\left|\frac{(E-E_C)}{\sigma^e_{E2}}\right|} + N_{h2} e^{-\left|\frac{(E-E_V)}{\sigma^h_{E2}}\right|}$$

$$\left(N_{1,e2,h2}\right)_m = \left(N_{1,e2,h2}\right)_0 \times 10^{-m}, m = 0, \ldots, 3$$

Equation: Noschis (2007)