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Design optimisation of depleted CMOS detectors using TCAD simulations within the CERN-RD50 collaboration

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In this work we report the main TCAD simulation results of a depleted CMOS detector designed in the 150 nm HV-CMOS process from LFoundry. These results have been used in the design of a test chip, the second prototype developed by the CERN-RD50 collaboration (RD50-MPW2), recently submitted for fabrication. The main aim of this study is to optimise the leakage problem seen in laboratory measurements of the first prototype developed by the collaboration (RD50-MPW1).

In order to minimize the leakage current in the second prototype, two design choices have been made. Firstly, particular attention has been paid to blocking the generation of certain filling layers added by the foundry during the post-processing stage. Secondly, a series of guard rings have been included around the device to prevent the sensor depletion region from coming into contact with the edge of the chip. These investigations will be presented. In addition, TCAD simulations have also been used to identify the best conditions for increasing the voltage applied to the sensor thus improving its radiation tolerance. The analysis takes into account the effect of the distance between the pixel bias ring and the sensing diode, and different shapes of the sensing diode.

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