Fully depleted monolithic sensors in 110 nm CMOS

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The evolution of the species

- First ALICE ITS: 6 layers, three “hybrid” technologies (SPD, SDD, SSD)

- ALICE ITS upgrade: 7 layers, one CMOS sensor (ALPIDE)
Fully depleted CMOS

- Fast charge collection by drift:
  - Better radiation hardness
  - Improved timing

- Deeper collection depth
  - Better SNR
  - Lower analog power

- With 150 $\mu$m depletion, 5 fF collection capacitance $\rightarrow \frac{Q}{C} \approx 0.4$ V
  $\rightarrow$ could be detected by a digital gate (zero analog static power)

- Analog power can be limited by time resolution
- Digital power determined by rate
Opportunities for CMOS sensors

- CMOS radiation sensors are relevant for many applications, but...

<table>
<thead>
<tr>
<th></th>
<th>Scalable to large area architecture</th>
<th>Extra low-power mode</th>
<th>Fully depleted sensor (sensitivity)</th>
<th>Fully depleted sensor (speed)</th>
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<tbody>
<tr>
<td>High Energy Physics</td>
<td>Scale economy in large detectors</td>
<td>Reduced material</td>
<td>dE/dx capability (equiv. to Si-strips)</td>
<td>Cost-effective timing layers, pile-up reduction</td>
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<tr>
<td></td>
<td></td>
<td>budget (no cooling)</td>
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<tr>
<td>Space applications</td>
<td>Reliability for space-born large</td>
<td>High spatial resolution</td>
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<td></td>
<td>detectors</td>
<td>space-born detectors</td>
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<tr>
<td>X-ray and UV Imaging</td>
<td>Reduced dead area in imaging panels</td>
<td></td>
<td>Broad spectrum imaging (0.5 eV to 10 keV)</td>
<td>Counting mode possible</td>
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<td>Medical imaging and tracking</td>
<td>Self-supporting sensors to avoid scattering</td>
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<td></td>
<td>Accurate timing for PET, particle tracking matching</td>
</tr>
</tbody>
</table>

- There is not an optimal electronics design that can serve all applications
- There isn’t even an unique sensor optimization
- What about sensor technology?
A versatile technology

It would be interesting to have a sensor platform that allows for:

- Active sensor thickness in the range 50 \(\mu\text{m}\) to 500 \(\mu\text{m}\) or more;
- Operation in full depletion with fast charge collection only by drift;
- Small charge collecting electrode for optimal signal-to-noise ratio;
- Scalable readout architecture with ultra-low power capability (O(10 mW/cm\(^2\)));

- **Easy compatibility with standard CMOS fabrication processes**

- Two steps approach: concept study with small-scale test structure (**SEED**) followed by large area sensors (**ARCADIA**)
The technology in a nutshell

- Goal: full depletion in 50-500 μm.
- Technology: 110 nm CMOS technology, high-resistivity bulk
- Both NMOS and PMOS transistors
- Custom backside process developed (collab. LFoundry)
- The depletion starts from the backside
- At the backside, the main diode is surrounded by a guard-ring
- Pixel capacitance lower than 20 fF
SEED: first silicon prototyping

Complete monolithic sensor

Test chip

<table>
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<tr>
<th>Technology</th>
<th>110 nm double side CMOS technology</th>
</tr>
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<tbody>
<tr>
<td>Metal layers</td>
<td>6</td>
</tr>
<tr>
<td>Size</td>
<td>2 X 2 mm²</td>
</tr>
</tbody>
</table>

- Wafers with small different epitaxial layer thickness have been used for the production

◊ SEED: Sensor with Embedded Electronics Development
The MATISSE chips

- Die area $2 \text{ mm} \times 2 \text{ mm}$
- Matrix of $24 \times 24$ pixels organised in 4 sectors
- Analogue readout with CDS
- In-pixel digital electronics for control and noise tests
- Use of one threshold flavour
In-pixel electronics

- Analog gain = 1/C_f
- Analog buffer based on a switched op-amp amplifier → high dynamic range
- The calibration system: test pulse injection and baseline regulation
Sensor architecture

- In pixel two level analog buffers
- Global shutter plus serial readout
- 4 analog output ports
Several test structures with different guard-ring design
Inversion layer may compromise guard-rings
Can be partially cured with irradiation
Cause understood and fixed in the next release just delivered by the foundry
Depletion studies: matrix

- In full depletion, total matrix capacitance is 2.7 pF
- I-V cure: few nA up to 180 V
- Maximum voltage before breakdown 240 V
Biasing 100 $\mu$m sensors

**Graph**: Current [A] vs. Voltage [V] for different values of $V_{NW}$.

- $V_{NW} = 0$ mV
- $V_{NW} = 400$ mV
- $V_{NW} = 800$ mV
- $V_{NW} = 1000$ mV

**Legend**: Thickness = 100 $\mu$m
Biasing 300 $\mu$m sensors

![Graph showing biasing characteristics of 300 $\mu$m sensors with different voltages](image)
Biasing 400 $\mu$m sensors

![Graph showing current vs voltage for different thicknesses and voltages.](image-url)
Depletion at work-1

100 V

110 V saturation

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TREDI 2019

FBK, 2019-02-26

16 / 24
Depletion at work-2

120 V

140 V

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Uniformity

CMIV distribution

<table>
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<tr>
<td>Entries</td>
</tr>
<tr>
<td>Mean</td>
</tr>
<tr>
<td>RMS</td>
</tr>
<tr>
<td>$\chi^2$ / ndf</td>
</tr>
<tr>
<td>Constant</td>
</tr>
<tr>
<td>Mean</td>
</tr>
<tr>
<td>Sigma</td>
</tr>
</tbody>
</table>

CMIV 2D MAP

All sectors

Noise sector # 0

Entries 144
Mean 10.18
RMS 0.9102

More samples

Noise [ADC]

Sample
Very good isolation between analog and digital circuits
The metal fillers of the channel has been designed so that left free the pixel centre for optical measurements.
A laser of with a **wavelength 1060 nm** has been used for the measurements.
The laser spot has been focused up to reach a diameter 8 um.
Laser sent to 16 pixels in the matrix.

**Non focused pulse**

**Focused pulse**

\[ Q = (7.01 \pm 0.08) \text{ fC} \]
Towards system-grade prototypes

**ARCADIA Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays**

- Dedicated mask set: reticle size 2.6 cm × 3.2 cm
- Engineering run by summer 2020

- Pixel size between 10 µm and 100 µm;
- embedded electronics with sparsified readout;
- binary readout modality for **maximum rate capability**, or
- analogue sampling on-pixel, digitisation on periphery;

- **data-driven readout** and **low-power digital architecture** for data and control signal transmission;
- **modular architecture** for a straightforward **scaling of the design to a reticle-size sensor**
Outlook

- R&D effort on DMPAS taking momentum within INFN
- Direct cooperation with a silicon foundry
- Large scale demonstrators planned for mid-2020
- Take as much profit as possible for the existing in the meanwhile

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The team

Bologna, Milano, Padova, Perugia, Pavia, TIFPA, Torino

\[ ENC \propto v_n \frac{C_d}{\sqrt{T_p}} \]
\[ v_n = \sqrt{\frac{4 \gamma k_B T}{g_m}} \]
\[ I_C = \frac{I_D}{2 \mu C_{ox} \frac{W}{L} \phi_T^2} \]

- For the same ENC

\[ C_D \rightarrow C_D/2 \Rightarrow I_D \rightarrow I_D/4 \]

- Difficult to beat pixels in binary mode
Figure 4. Current-voltage curves measured on a pseudo-pixel array with different pixel bias voltage. The horizontal axis represents the absolute value of the backside voltage. n-type regions and the top guard ring. This current is reduced by more than 4 orders of magnitude at the onset of full depletion, that depends on the pixel voltage. At voltages larger than 220V, the current starts increasing again, due to the onset of punch through between the backside junction and the front-side pwell/substrate junction. The operation range for the backside voltage thus depends on the applied pixel voltage. In a pixel array this voltage can be chosen to be larger than 0.6V, to ensure an operation range larger than 50V.

To explore the charge collection dynamics, the pseudo-pixel array was connected to a voltage amplifier with 1GHz bandwidth, as shown in Figure 5. A fast pulsed laser (λ=1064nm, pulse width < 100ps FWHM) was focused on the sensor surface and the signal was recorded with a fast oscilloscope. The signal is shown in Figure 6 for two different illumination intensities, corresponding to a collected charge of $1.2 \times 10^5$ e-/pixel and $3 \times 10^5$ e-/pixel. During the measurement, the test structure was biased at 160V and the pixels were biased at 0.8V. The experimental results show that a complete collection of the generated charge can be obtained within 50ns, thus making this approach suitable for the detection of events with high repetition rate.

Conclusion

In this work, we have presented a modified deep submicron CMOS process with thick fully depleted substrate for the sensing of particles and radiation with large absorption length. The characterization results obtained on test structures from a first run with 300 µm substrate thickness demonstrated the feasibility of the approach. Test structures and pixel arrays from a second run with different substrate thickness, 100 µm and 400 µm, are currently undergoing characterization.

Acknowledgments

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Example of DMAPS

- Modification of the TJ process used in ALPIDE
  W. Snoeys et al., NIM A871 (2017) pp. 90-96

- SOI pixels
  T. Miyoshi et al., NIM A824 (2016) pp. 439-42

- HV-CMOS
  N. Wermes NIM A824 (2016) pp. 483-86