Test results of irradiated monolithic CMOS pixel circuits in LFoundry 150 nm technology for the ATLAS Inner Tracker Upgrade

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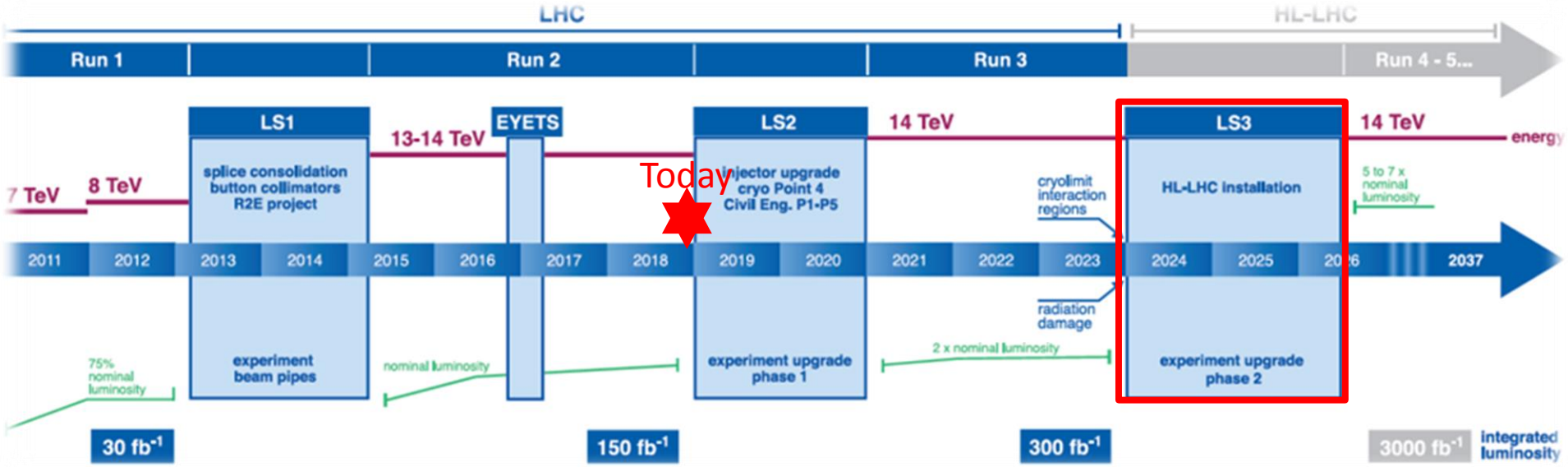
Outline

- ATLAS Inner Tracker (ITk) upgrade
- CMOS sensor option for pixels
- LF-Monopix1 characterization and beam measurement
- Conclusion

LHC / HL-LHC Plan



- The High Luminosity Large Hadron Collider (HL-LHC) is foreseen to switch on by 2026 with a center of mass energy of 14 TeV and a peak instantaneous luminosity of 7.5×10^{34} $cm^{-2}s^{-1}$, five times higher than at present.

- The increased luminosity will result in ~ ten times higher radiation levels and ten times higher data rates.

ATLAS ITk upgrade for HL-LHC

- To match the requirements in terms of radiation hardness, readout speed and granularity at the HL-LHC, the replacement of the present Inner Tracker (ITk) is needed.
- The new tracker will consist of silicon only technologies.

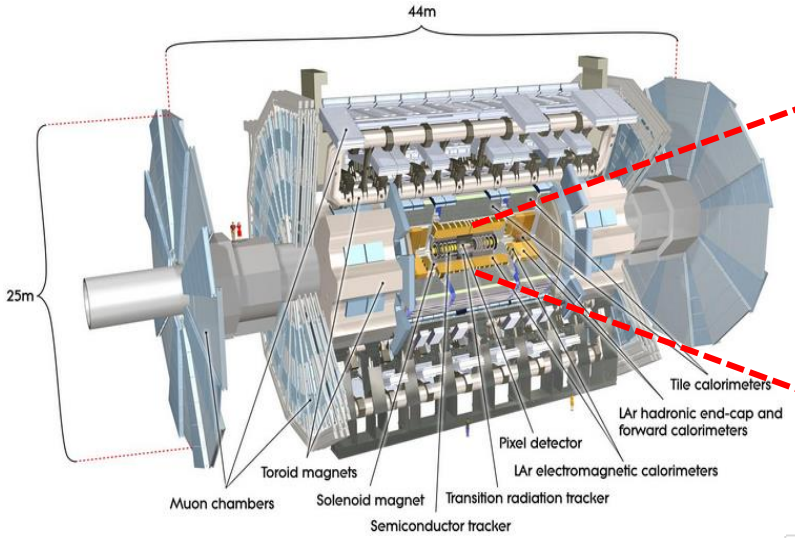
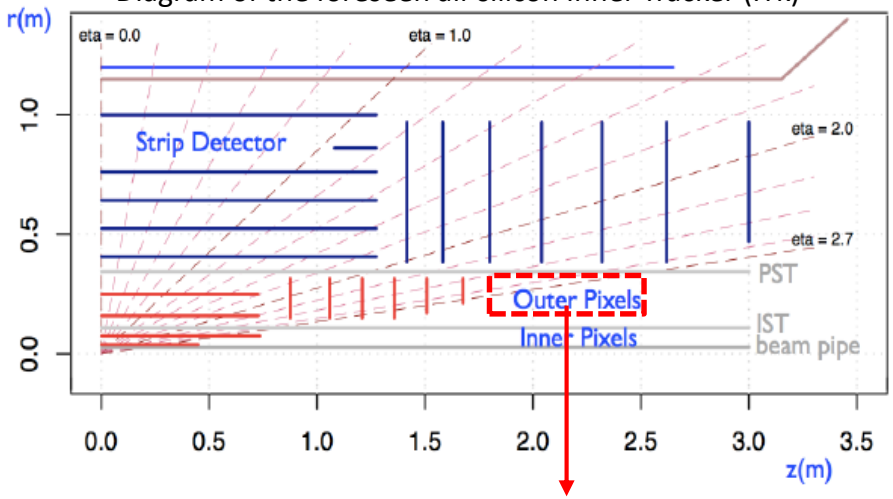


Diagram of the foreseen all-silicon Inner Tracker (ITk)



	ATLAS-ITK	
	Outer	Inner
Fluence [n_{eq}/cm^2]	10^{15}	10^{16}
Ion. Dose [Mrad]	80	1000
Total area [m^2]	10	1

- **<u>Outer pixel layers (two official possibilities*)</u>**:
  - Classical hybrid pixel as the baseline. (Planar sensor + RD53 readout IC).
  - Full monolithic CMOS chip with integrated readout .

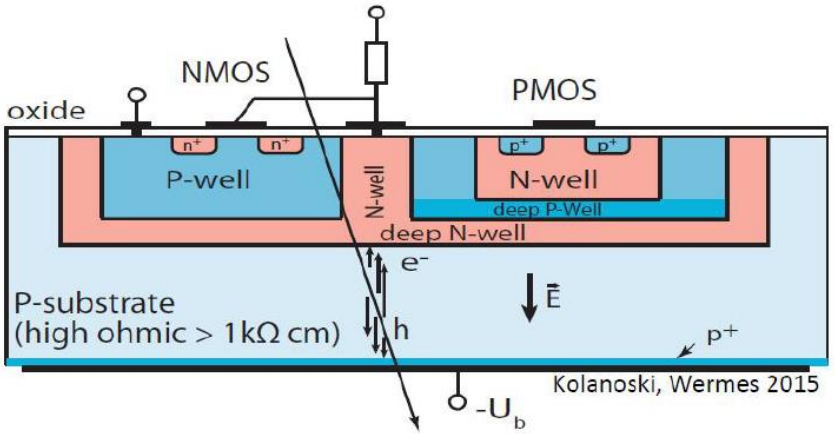
* Technical Design Report for the ATLAS Inner Tracker Pixel Detector

Monolithic CMOS Sensor

- Commercial process (mass production technology).
- No hybridization (reduced material budget and costs, easier procurement).
- Considerable depleted regions in high resistive substrates, fast charge collection by drift.

Two design approaches

"Large Collection Diode"



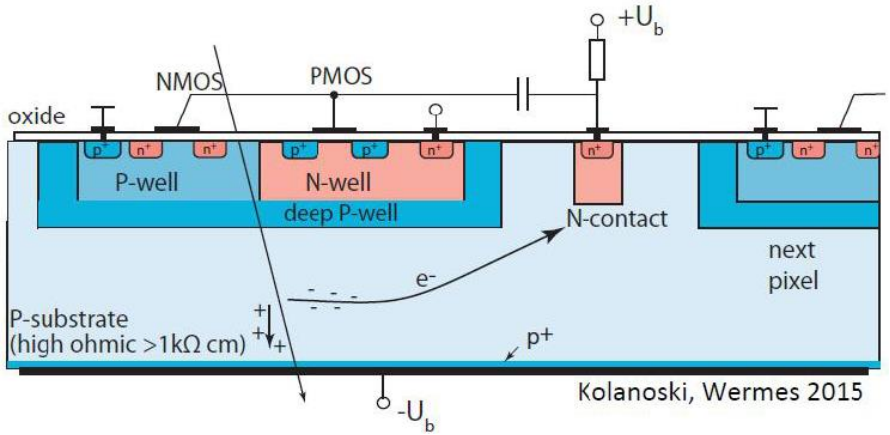
PROS: Short drift distances→ radiation tolerant

CONS: Large sensor capacitance →noise & speed (power) penalties

$$ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{C_d^2}{\tau} \qquad \tau_{CSA} \propto \frac{1}{g_m}\frac{C_d}{C_f}$$

LFoundry technology

"Small Collection Diode"



PROS: Small sensor capacitance → low power consumption

CONS: Long drift distances → Less radiation hard

LF technology development line

- The process:
  - DeepNW/DeepPW 150nm LF process
  - 7 metal layers
  - High resistivity (> 2kΩ.cm)

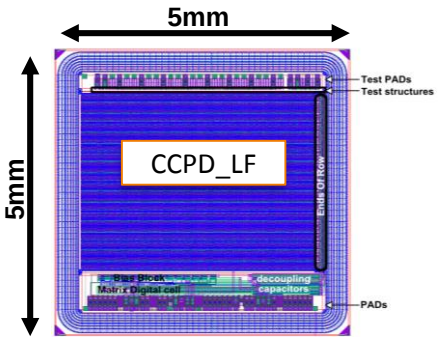
Characterization results (today !)

2014~2015
Small size demonstrator

2016~2017
Large size demonstrator

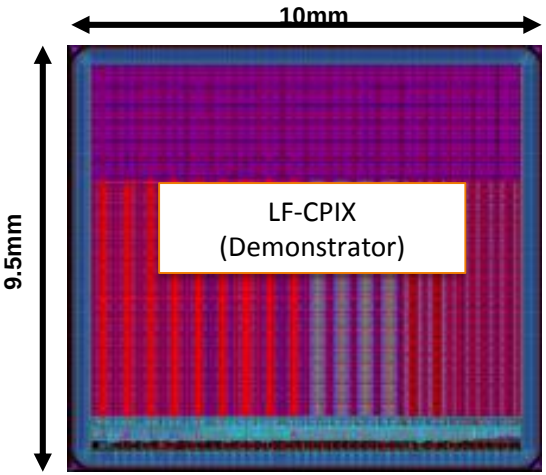
2017~Present
Large Monolithic demonstrator

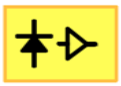
CCPD_LF:
33×125µm² pix ; 6pix → 2 FEI4 pix
5×5 mm² IC, **bondable to FE-I4**
Bonn / CPPM / KIT



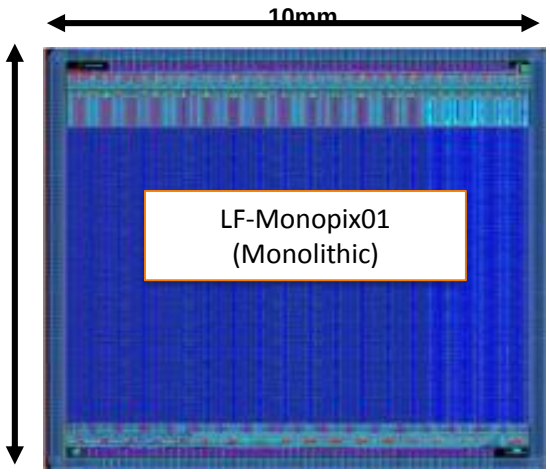

Diode + preamp

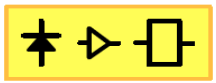
LF-CPIX:
50×250µm² pix ; diff. pix flavors
10×10 mm²; 2 versions -Guard-Ring-
Bonn / CPPM / IRFU



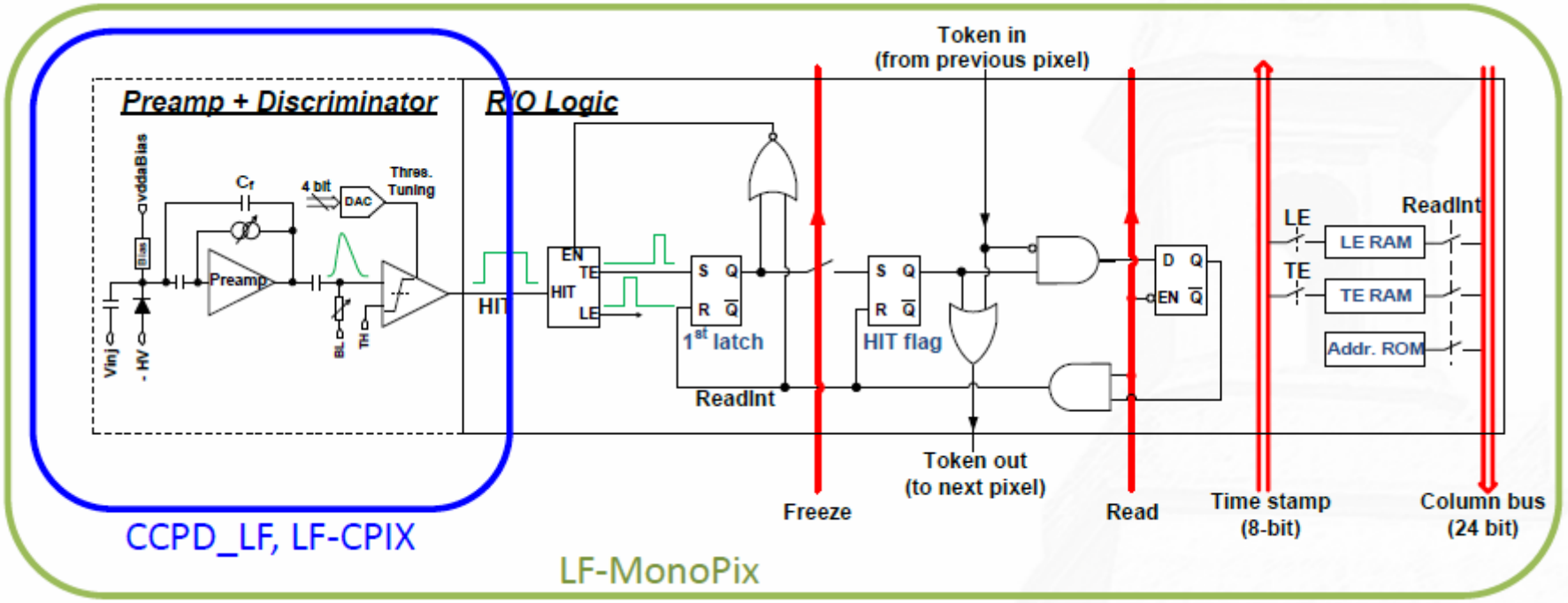

Diode + preamp

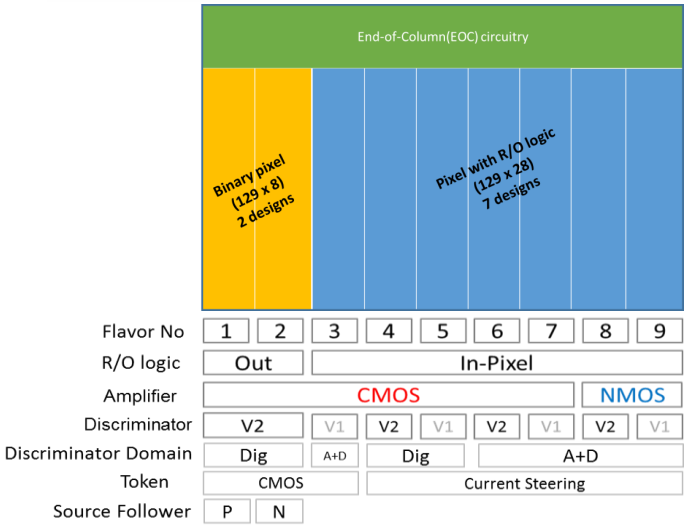
LF-Monopix1:
50×250µm² pix
10×10 mm² IC
1st full monolithic demonstrator!
Bonn / CPPM / IRFU




Diode + Amp + Digital

LF-Monopix1: Pixel design

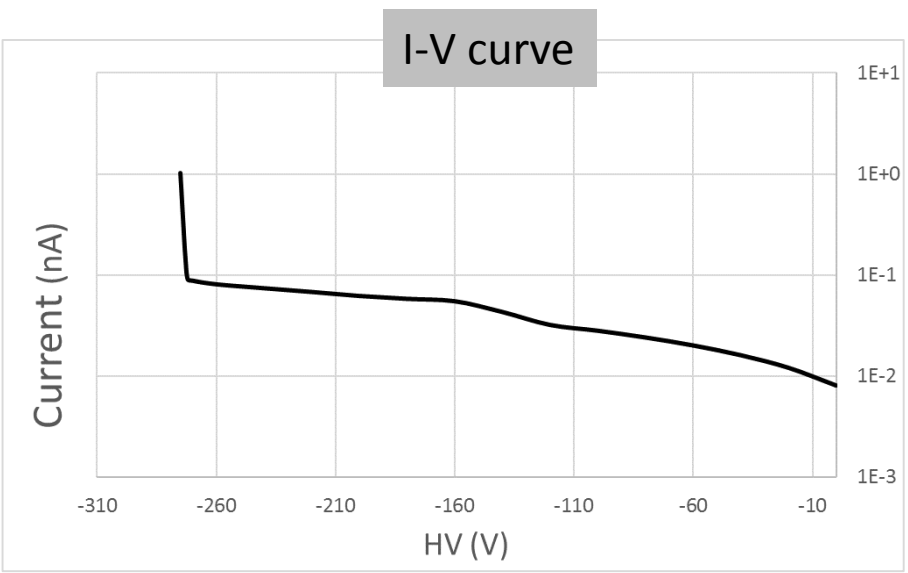


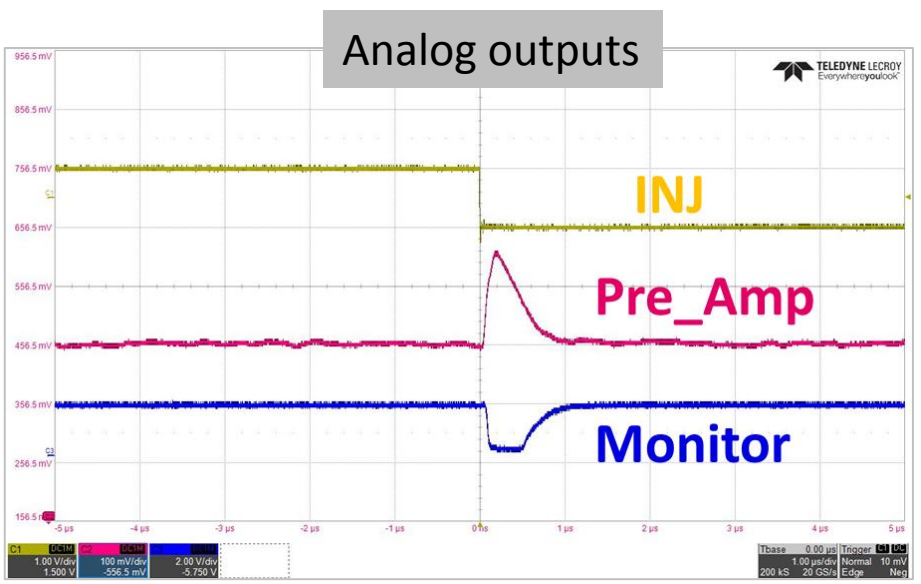


- 150nm CMOS process, LFoundry (Resistivity >2kΩ.cm).
- Similar diode and analog front end circuitry design as in LF-CPIX.
- 129 x 36 pixel array (9 sub matrices with different pre-amplifiers, discriminators, R/O concepts …).
- Column-drain R/O logic (FE-I3 like).
- 40 MHz (up to 160MHz by design) LVDS serial output.

LF-Monopix1: Laboratory results

- The breakdown voltage is around -280V at room temperature, which is an improved value with respect to previous prototype in this technology and matches simulation results.
- Both the preamplifier and discriminator have good response with external test injection



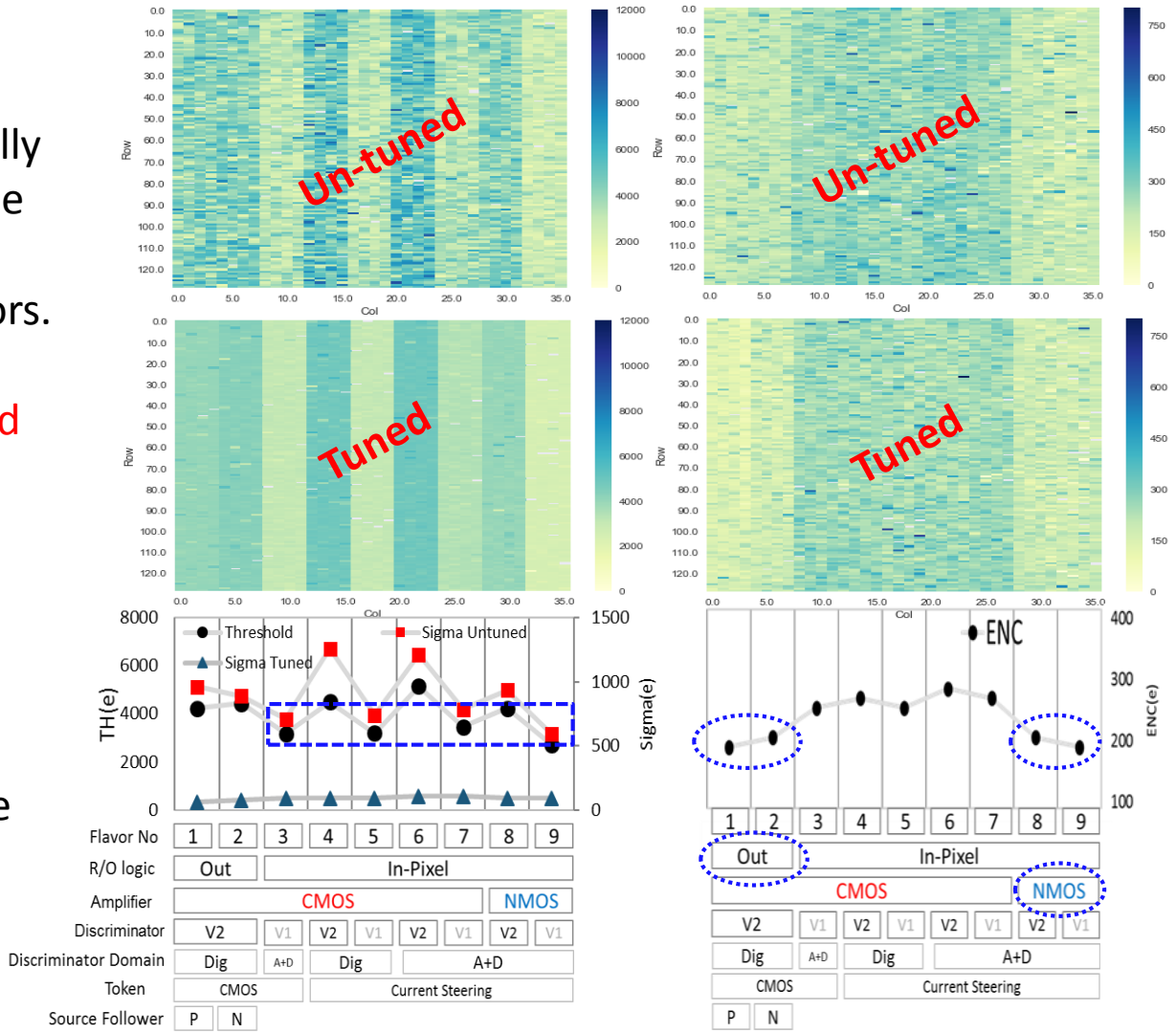


Breakdown ~ -280 V

Responses of the preamplifier and discriminator

LF-Monopix1: Laboratory results

- All the flavors of pixels with fully integrated read-out logic can be tuned with a dispersion within 110e~148e depending on flavors. The noise value for different flavors falls between 190 e- and 280 e-.
- V1 discriminator shows better performance on dispersion;
- the NMOS input transistor preamplifiers show lower noise than CMOS flavors.

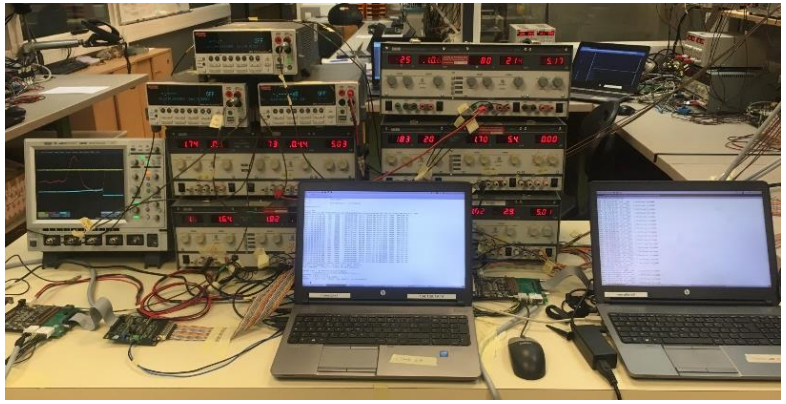


Threshold mapping

Noise mapping

LFMONOPIX IRRAD SETUP @PS CERN

Control Room



Control Room Setup

Power Supplies (Burndy cable)

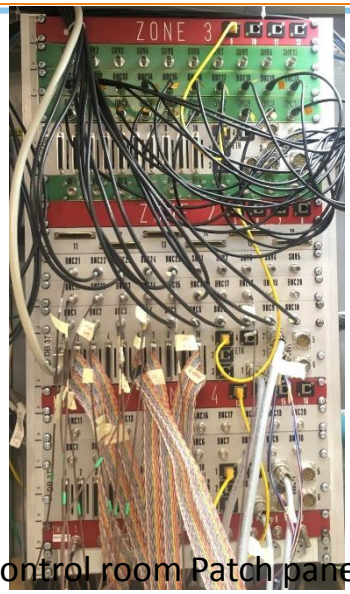
LF_MONOPIX LVDS signals

LEMO Inj

LEMO HV

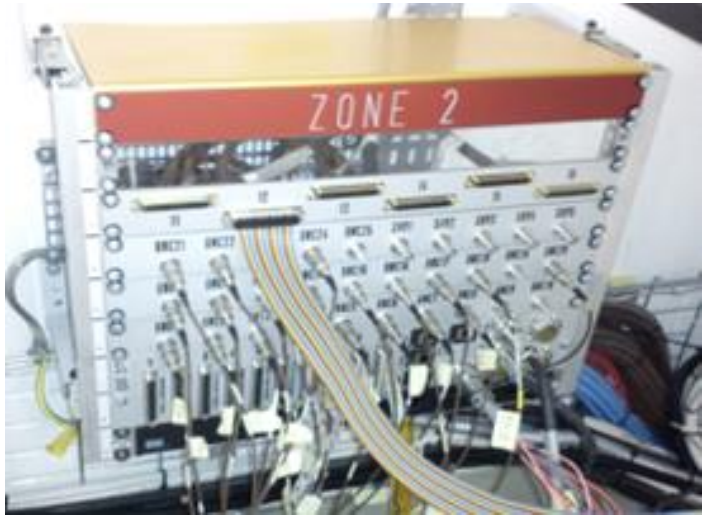
LEMO Disc_out

LEMO Amp_out



Control room Patch panel

IRRAD Zone



IRRAD Zone Patch panel

Power Supplies (Burndy cable)

LF_MONOPIX LVDS signals

LEMO Inj

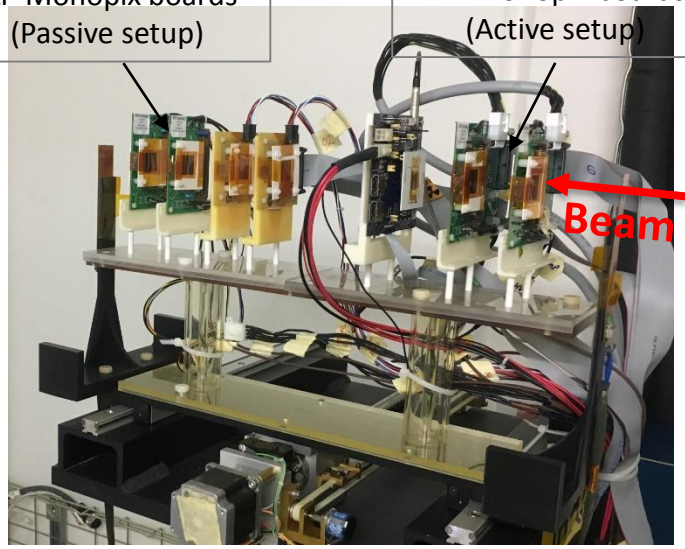
LEMO HV

LEMO Disc_out

LEMO Amp_out

2 LF-Monopix boards (Passive setup)

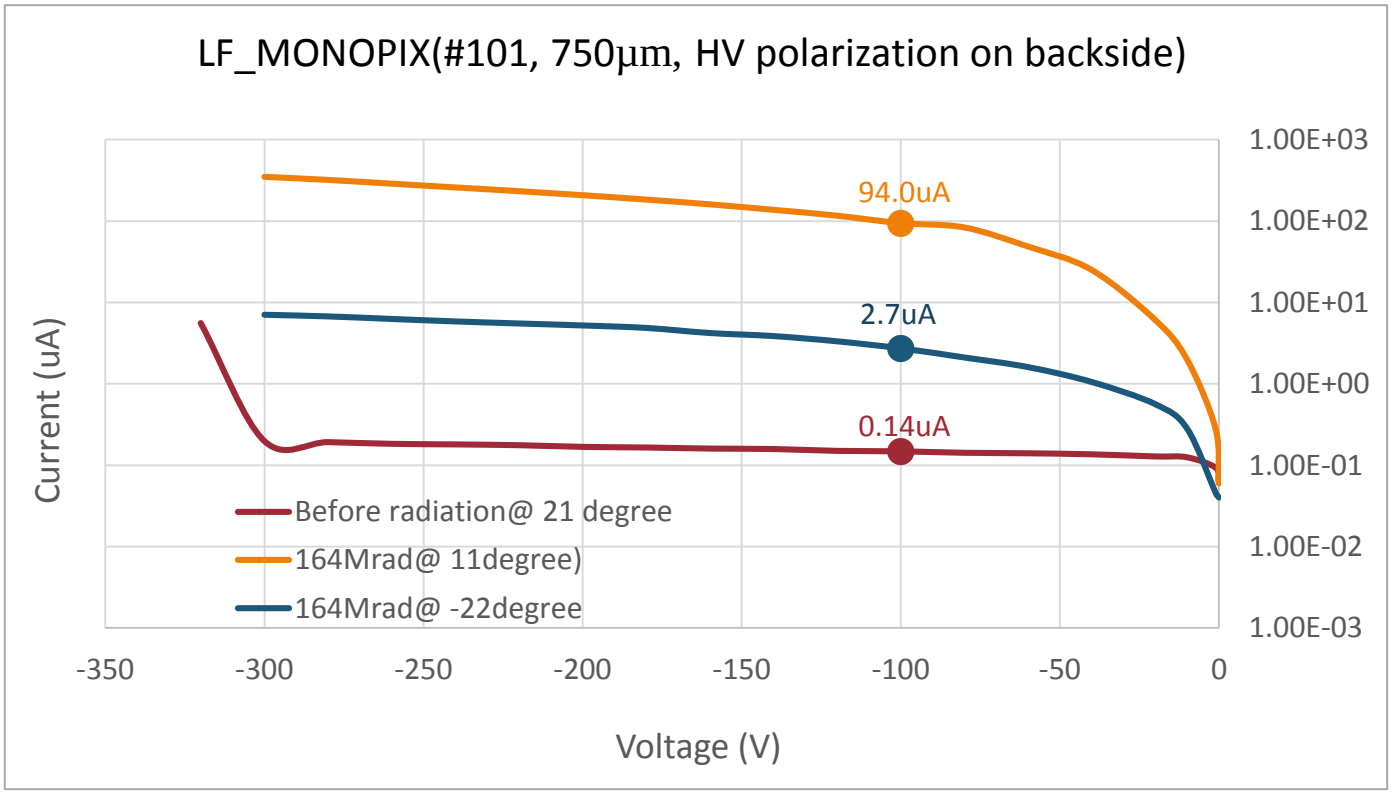
2 LF-Monopix boards (Active setup)



Leakage Current: Radiation under PS@CERN

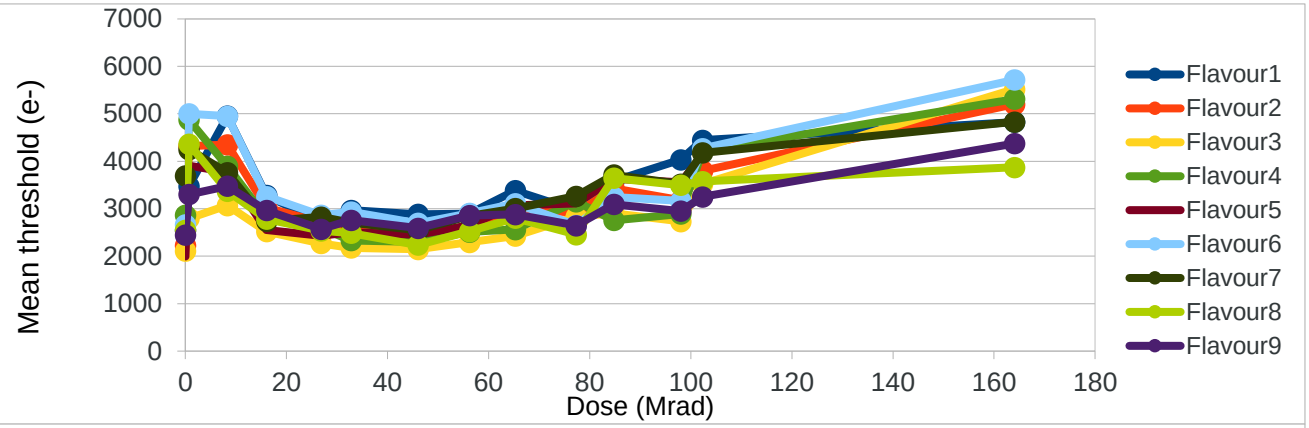
Proton beam @ CERN PS

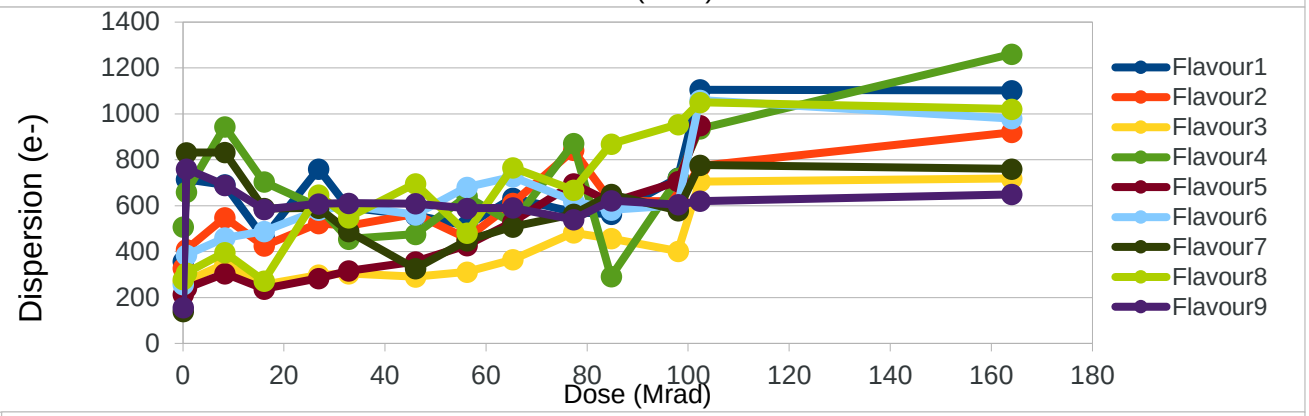
- Oct → Nov 2018 :
- 24 GeV protons irrad
- TID~164 MRad reached (roughly 2 times the dose expected for the 4th layer)
- NIEL=3.7× 10^{15} $n_{eq}\cdot cm^{-2}$

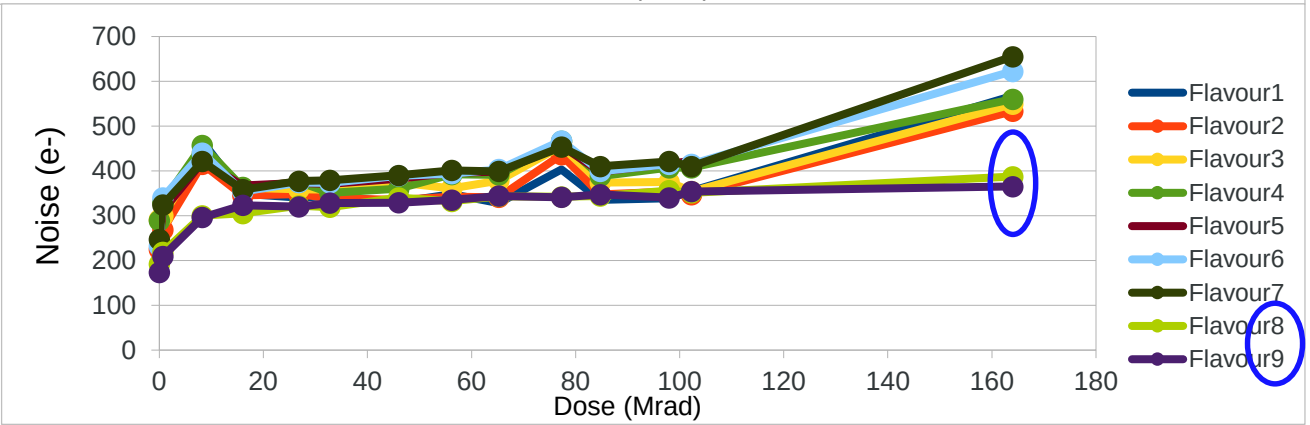


The leakage current increase after irradiations seems acceptable

Mean th, dispersion and noise VS Dose (temp=21°C)







LF_MONOPIX #101 (750um)

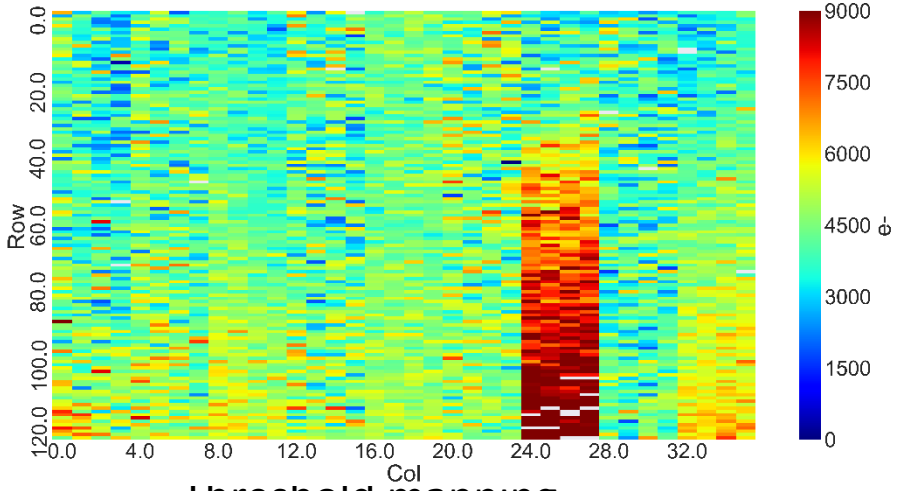
Mean threshold versus dose
(Load the tuned TDAC
One column each flavor)

Dispersion versus dose
(Load the tuned TDAC
One column each flavor)

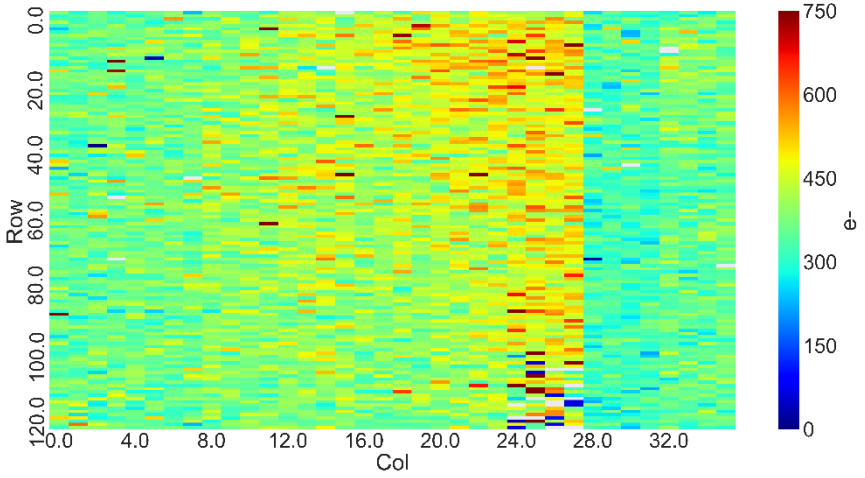
Noise versus dose
(Load the tuned TDAC
One column each flavor)

Threshold & Noise mapping (TID=164Mrad)

Room temp (10 degree)

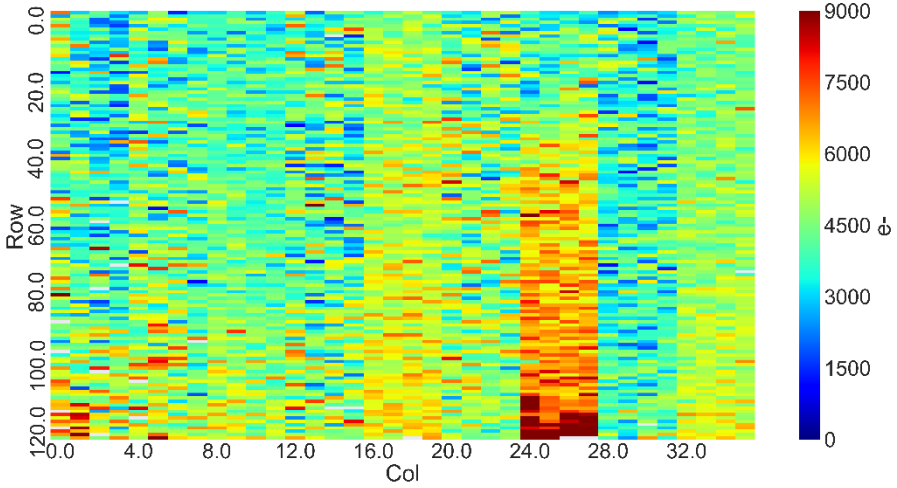


Threshold mapping

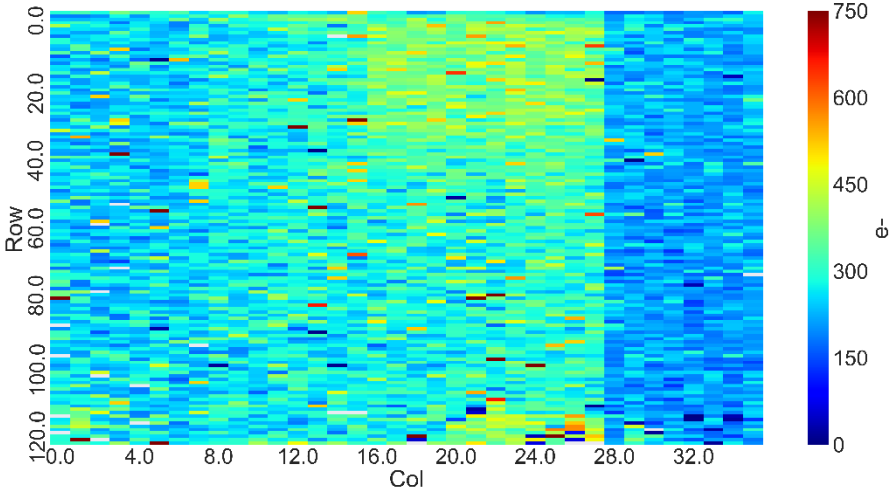


Noise mapping

Low temp (-22 degree)



Threshold mapping

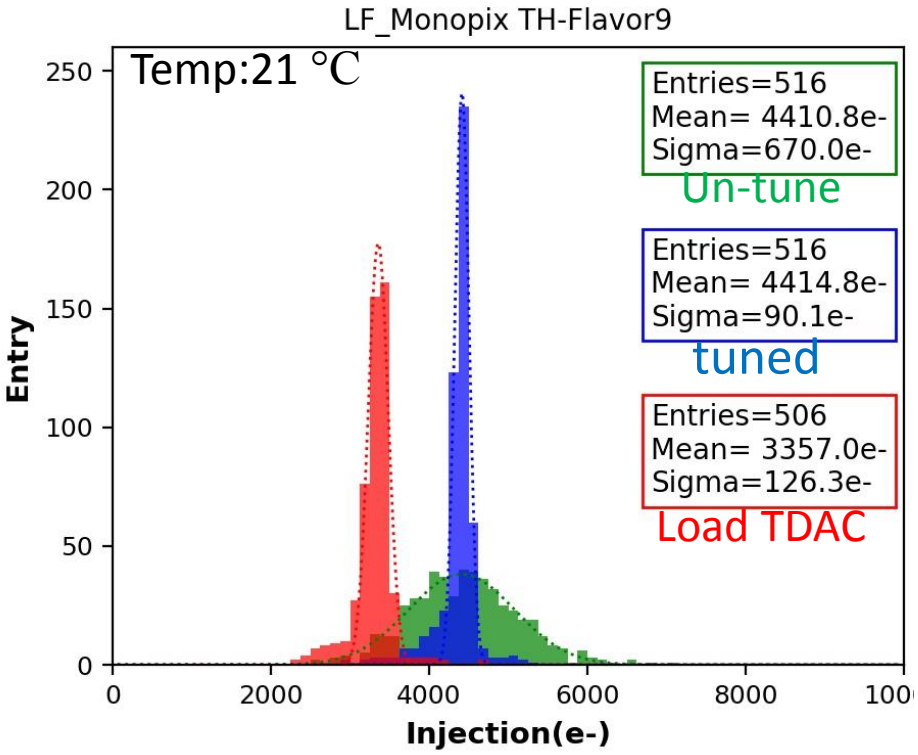


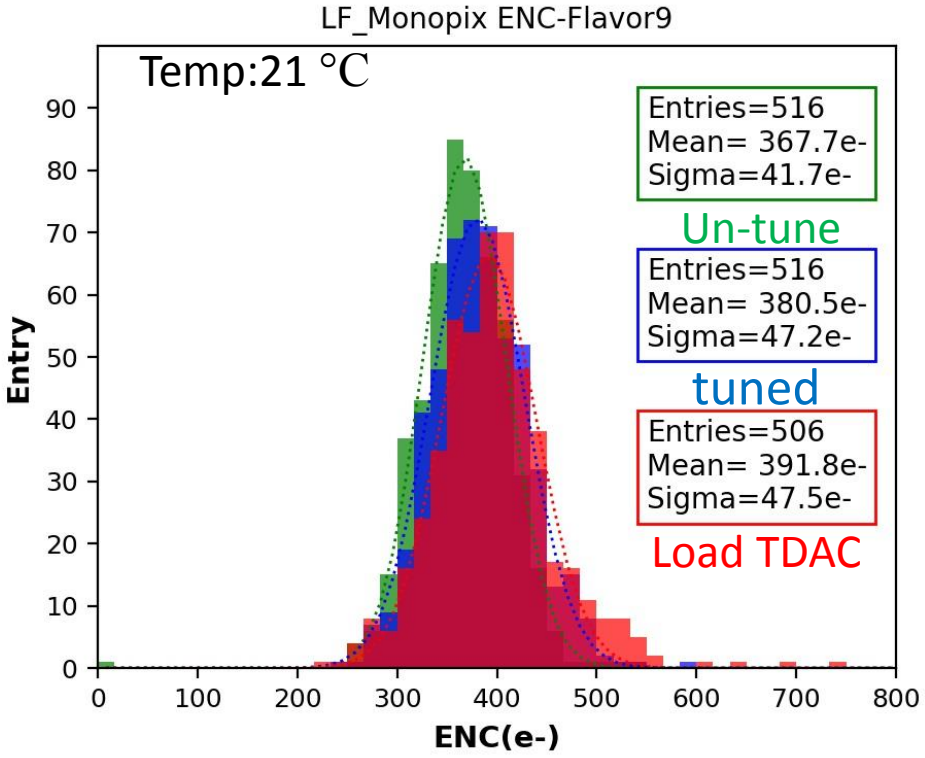
Noise mapping

LF_MONOPIX1 threshold tuning (TID=164Mrad)

- Tested at the end of radiation campaign (Total dose=164Mrad)
- **Flavor9: NMOS CSA + V1 Disc**

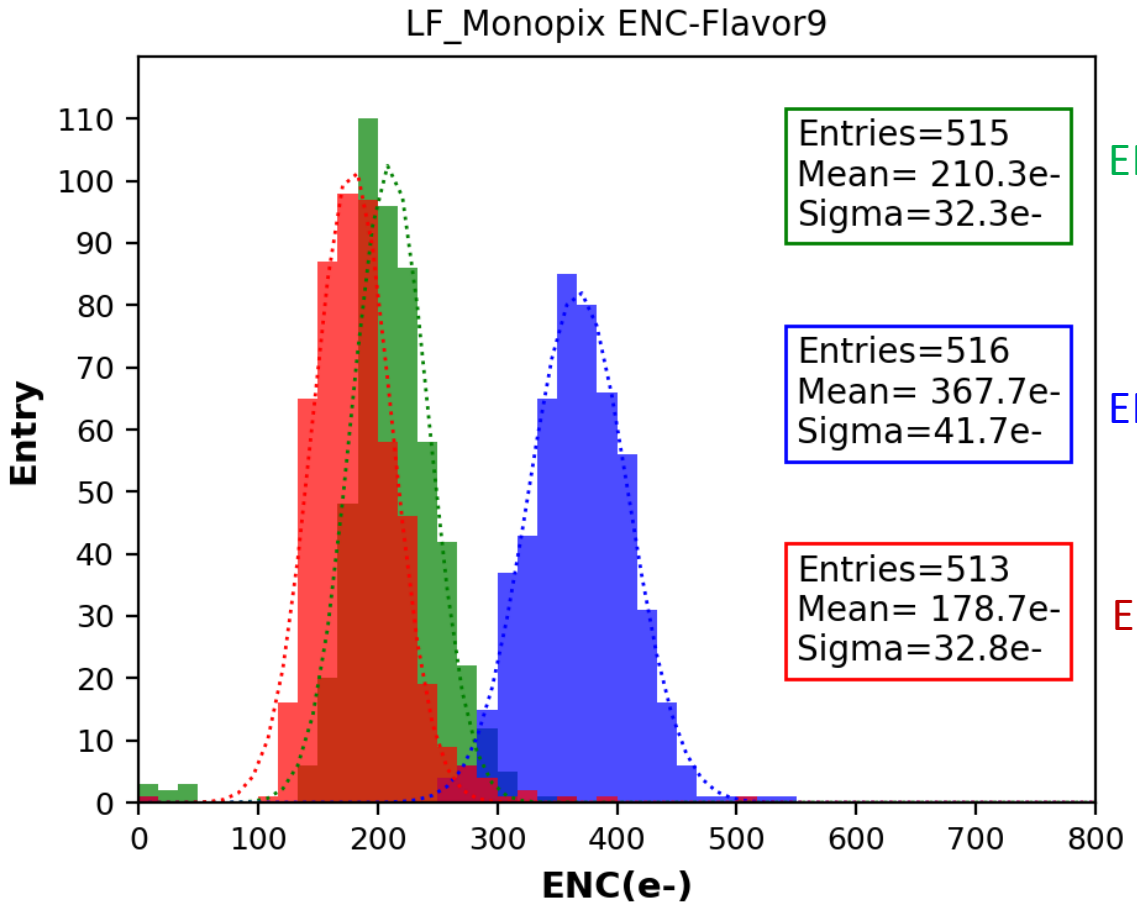
1. Simple threshold scan with global TH → Un-tune
   Pixel masked (0.0%)
2. TDAC tuning with same global TH → Tuned
   Pixel masked (0.0%)
3. Load the TDAC values with lower global TH → Load TDAC
   Pixel masked (1.9%)





LF_MONOPIX1 ENC @TID=164Mrad

- Flavor9: NMOS CSA + V1 Disc
- The ENC value is around 210e- @-22°C, TID=164Mrad, which is just slightly higher than the value @10°C before radiation.



ENC@-22°C, TID=164Mrad

ENC@10°C, TID=164Mrad

ENC@10°C, TID= 0 Mrad

Conclusion & outlook

- **LF-Monopix1**: fully functional demonstrator chip with column drain readout.
  - Good breakdown voltage characteristics (BV below -280V).
  - Limited threshold dispersion (can be tuned within 110e~148e depending on flavor).
  - ENC for different flavors is between 190e- to 280 e-.
  - Good irradiation performances:
    - TID=164 MRad and NIEL=3.7× 10^{15} $n_{eq}\cdot cm^{-2}$ reached
    - Limited leakage current increase after 164MRad.
    - Limited ENC increase.
    - The threshold can be tuned down to 3357e- with a dispersion 126e-.

- **Next step and Outlook**.
  - Need to understand the radiation effect on different parts of the chip.
  - Need to reduce the pixel size and leakage current (layout optimization).
  - Based on the results of the LF-MONOPIX1, find best strategy for the next demonstrator.

The collaboration works on an improved full size LF_MONOPIX2 that could be used in ATLAS ITk layer 4 → target: summer in 2019

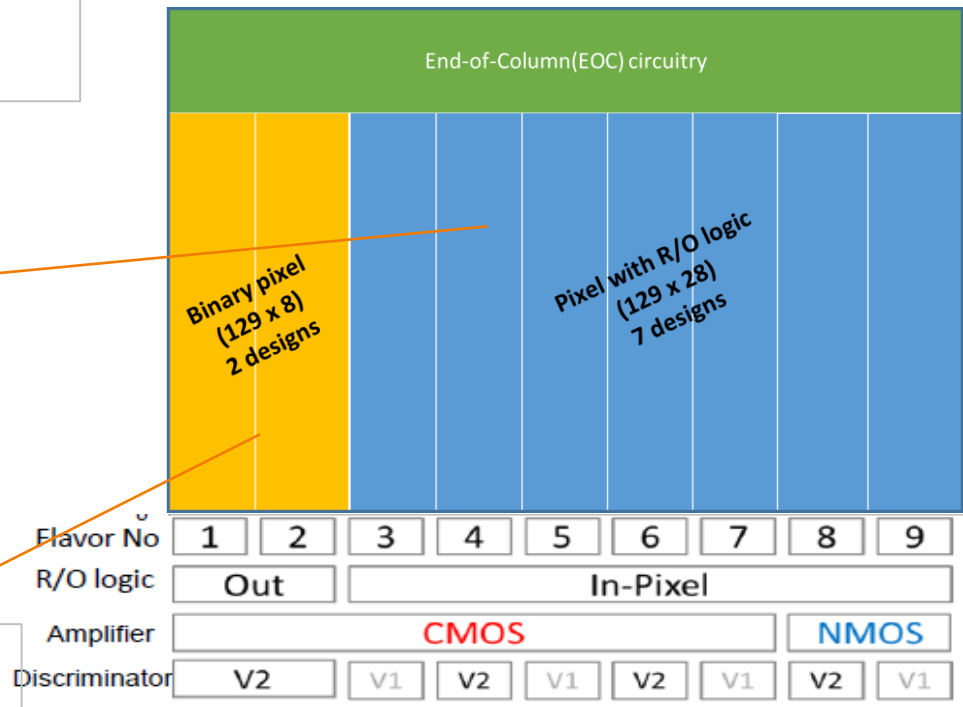
Thanks for your attention!

General description of the LF-MONOPIX

- 150nm CMOS (Resistivity **>2 kOhm-cm**)
- **129 x 36** pixel array
- 40 MHz (160MHz by design) LVDS serial output

- 7 flavors with “in-pixel”R/O logic: NMOS or CMOS amplifier, “V1” or “V2”discriminators, current steering or CMOS token transmission.

- 2 flavours with off-matrix(“external”) R/O logic: CMOS amplifier, “V2” discriminator, NMOS or PMOS source followers.



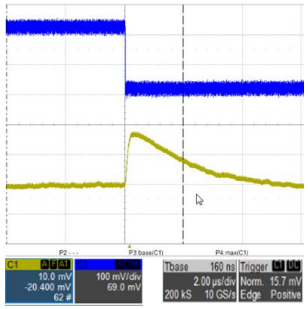
V1: two stage open-loop structure
V2: self-biased differential amplifier with a CMOS output stage

Calibration of the capacitance (LF-Monopix)

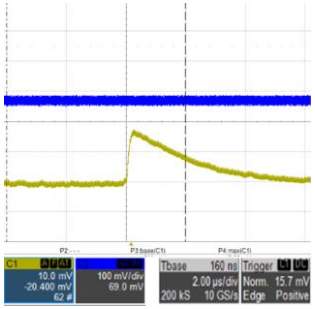
Calibration of the Capacitance Setup

$$Cinj = Q/V = N*e/V$$

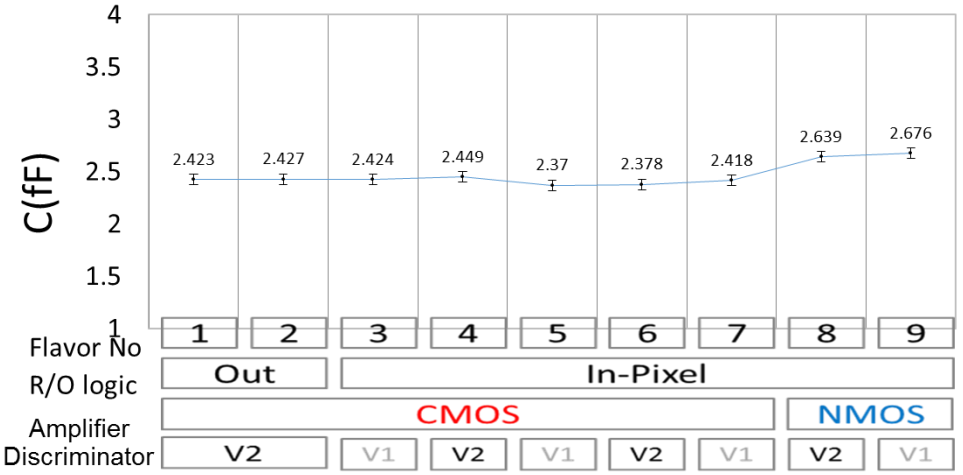
Cinj: Injection Capacitance
N: Number of 55Fe electrons (1619e-)
e: elementary charge
V: external injection



External Injection

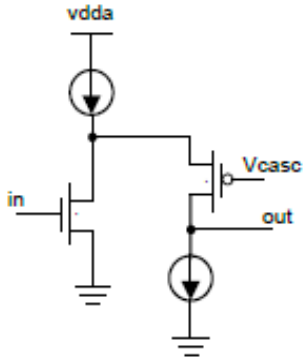


55Fe Source Signal

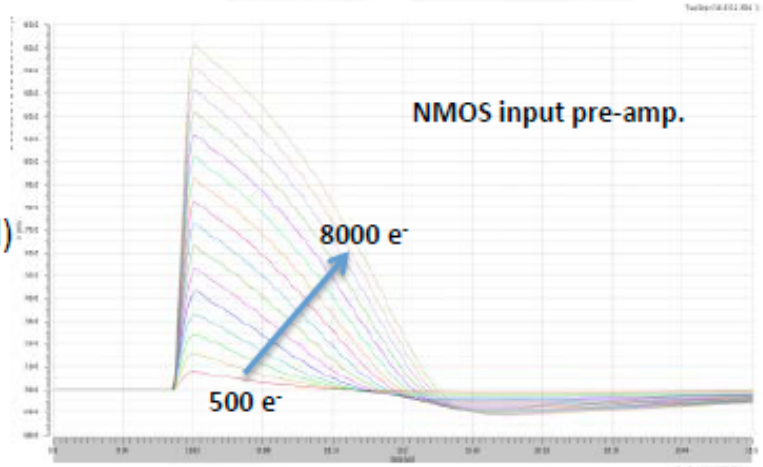


LF-Monopix01: Pixel design

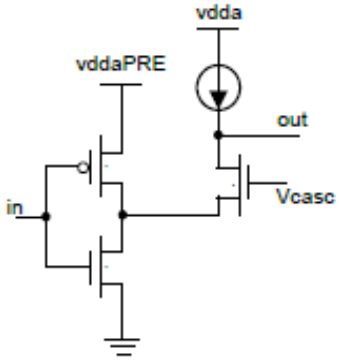
- Pre-amplifiers => aimed at peaking time $\lesssim$ 25 ns with 400 fF C_d
  - NMOS input: modified from LF-CPIX in order to deal with the increased C_d



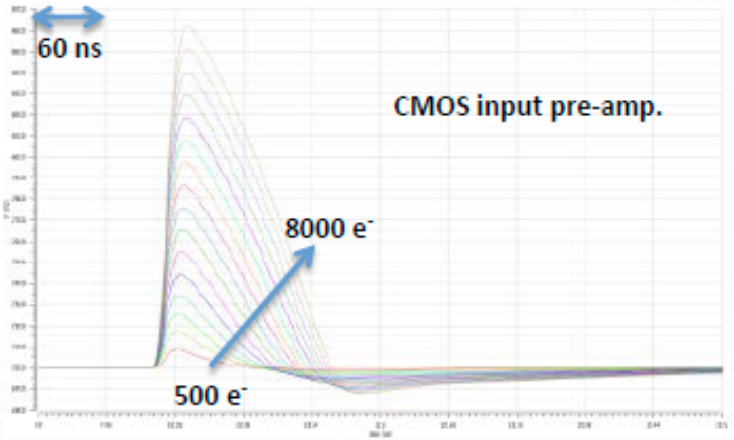
- ❑ Bias current ~ 17 µA
- ❑ peaking time ~ 20 ns (4 ke⁻ signal)
- ❑ ENC ~ 170 e⁻



  - CMOS input: same as LF-CPIX

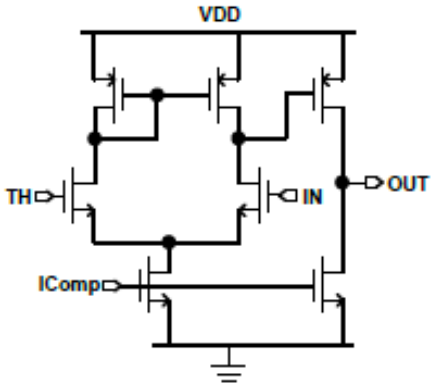


- ❑ Bias current ~ 15 µA
- ❑ peaking time ~ 25 ns (4 ke⁻ signal)
- ❑ ENC ~ 135 e⁻

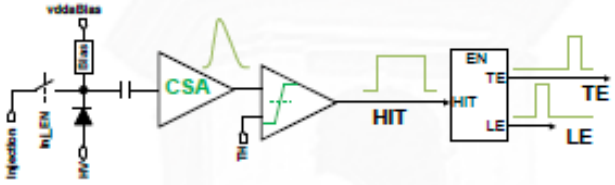


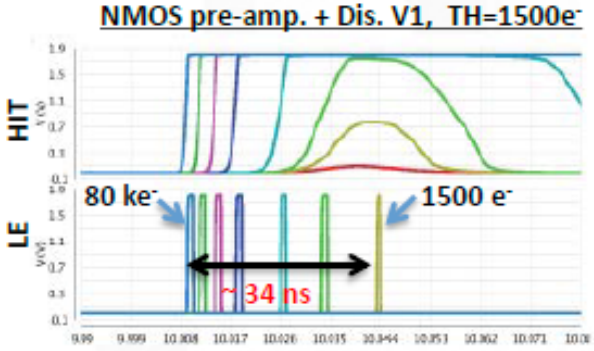
LF-Monopix01: Pixel design

- Discriminator => influence on the time walk
  - Discriminator V1: same as LF-CPIX

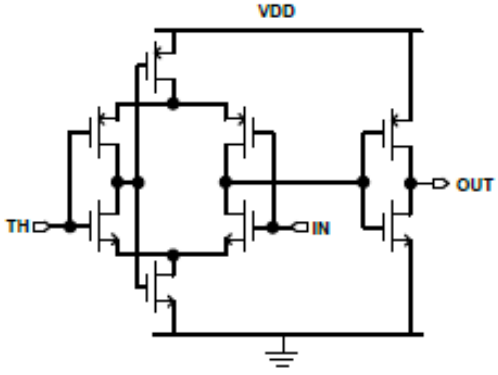


- ❑ 2-stage amplifier as comparator
- ❑ bias current: 4.5 µA
- ❑ slow at threshold edge

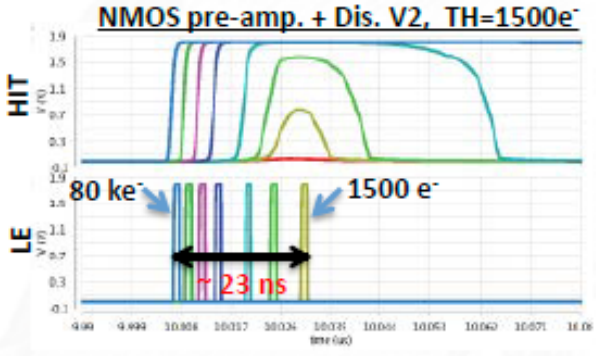




  - Discriminator V2:

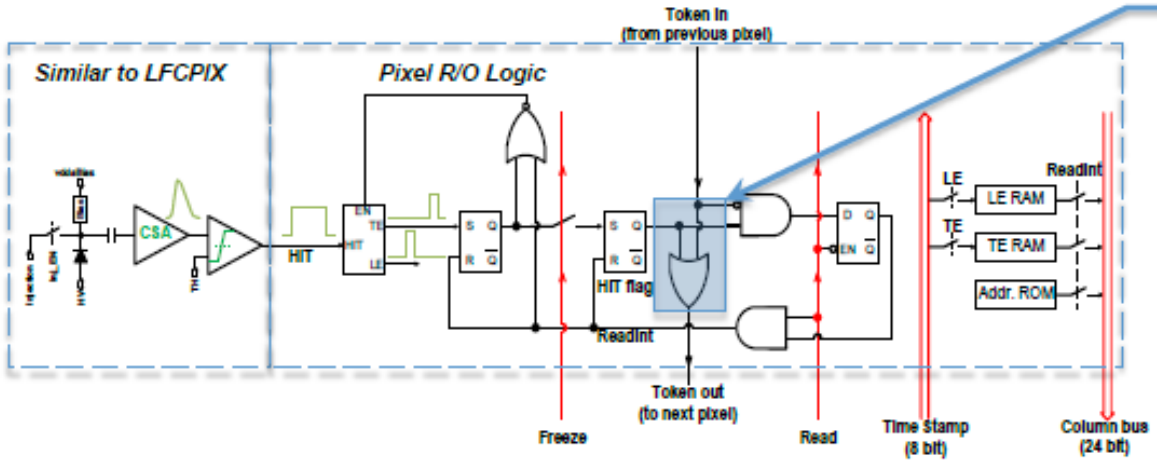


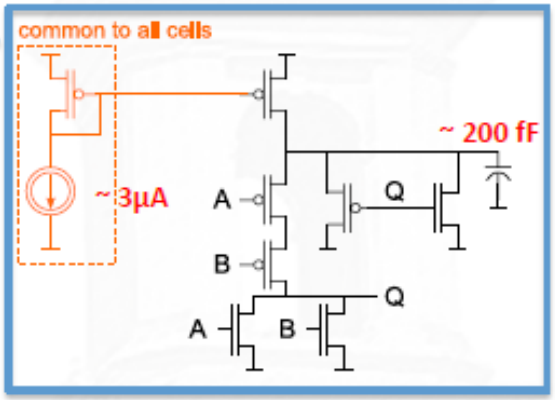
- ❑ Two amplifiers load each other
- ❑ self biased: < 4µA
- ❑ CMOS inverter as 2nd stage



LF-Monopix01: Pixel design

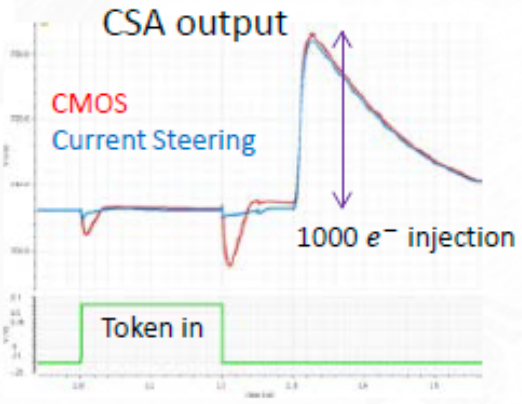
- Low noise is critical for some digital blocks





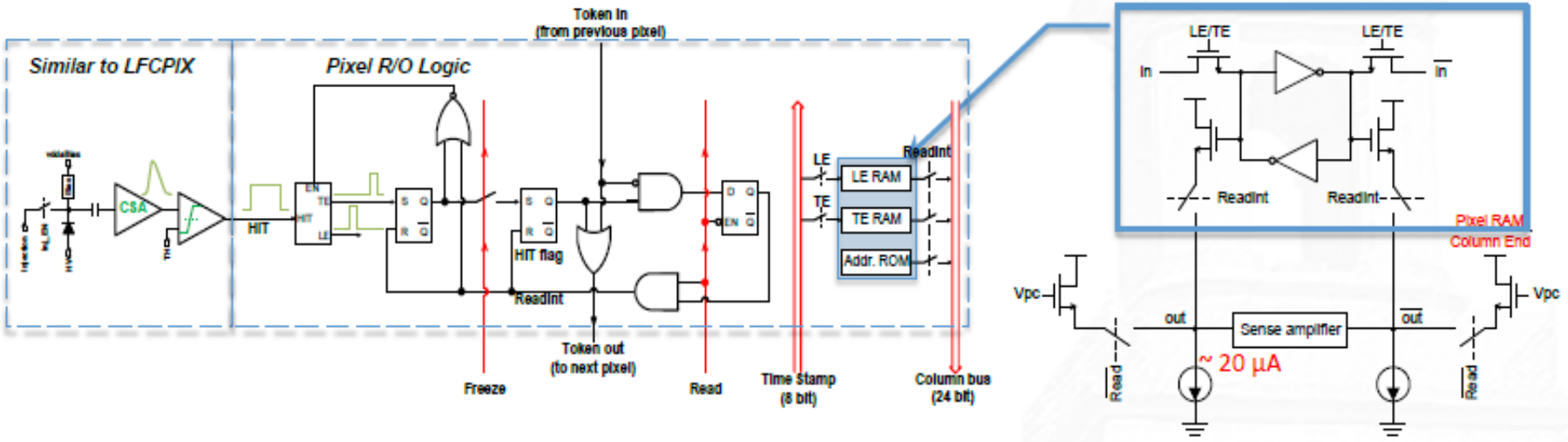
- Token propagates while pixels are sensitive
  - Current Steering (CS) logic

    => constant current => less noise



LF-Monopix01: Pixel design

- Low noise is critical for some digital blocks



- Data R/O with source follower
  => avoids high current injection into the PW during high to low transition
- SF bias at column end ~20µA
  - 24 pairs per column => LE, TE, Addr.