Main developments at CPPM

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CPPM, Marseille
ESR-02

Outline

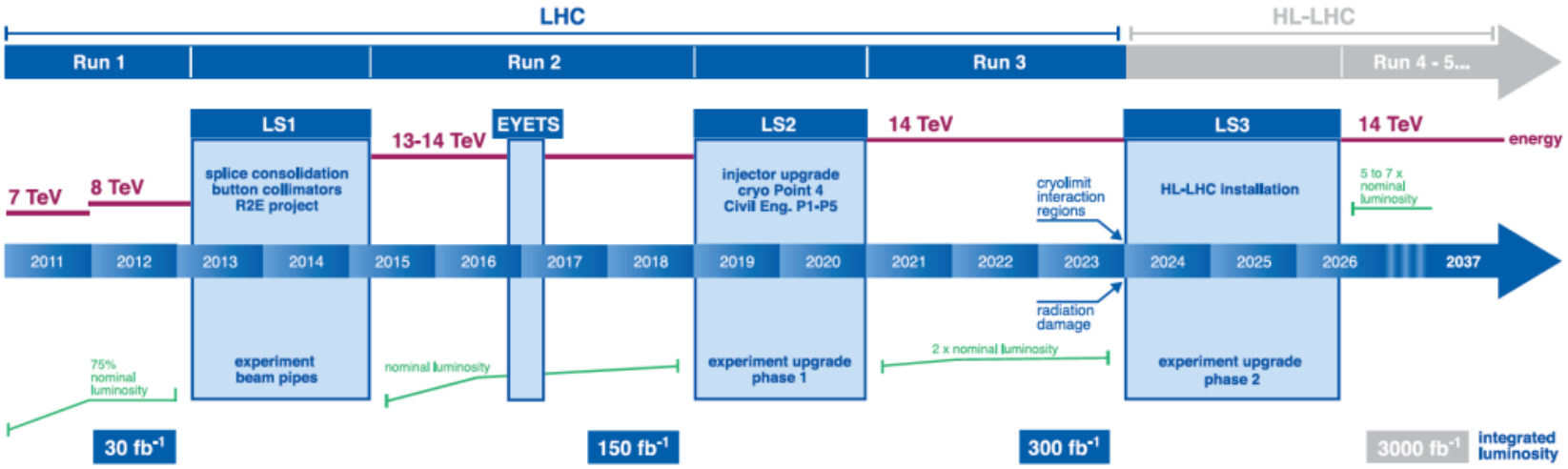
- **Milestone 1**

→ Developments towards a **Serial Powering** implementation in a monolithic CMOS technology for a ATLAS ITk upgrade.

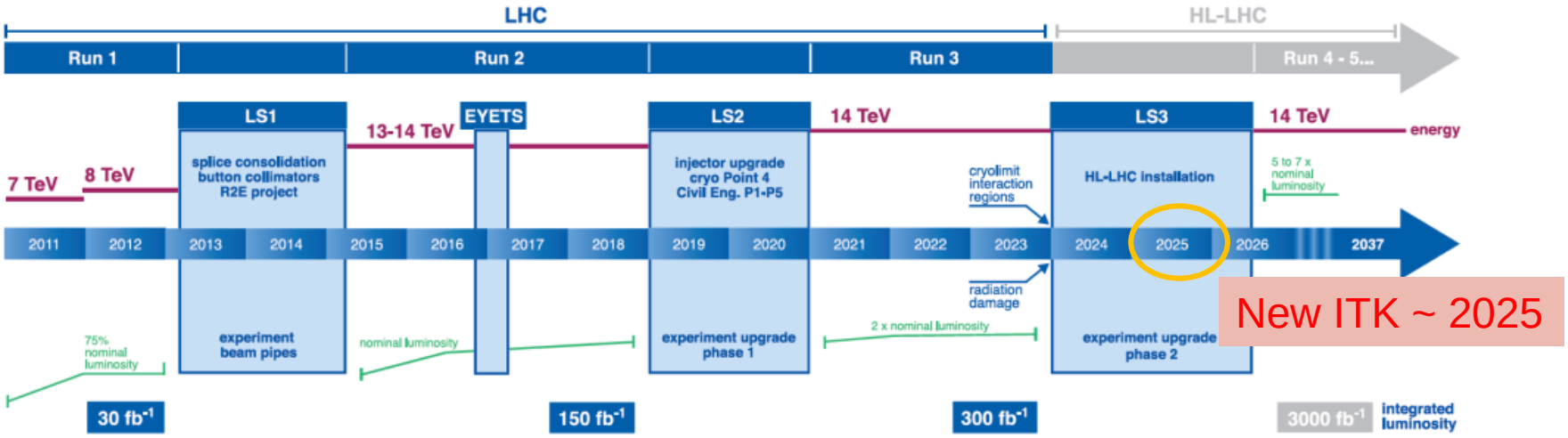
- **Milestone 2**

→ Design and measurements of **Single Event Upsets (SEU) tolerant** memories for the ATLAS ITk upgrade.

ITk tracker

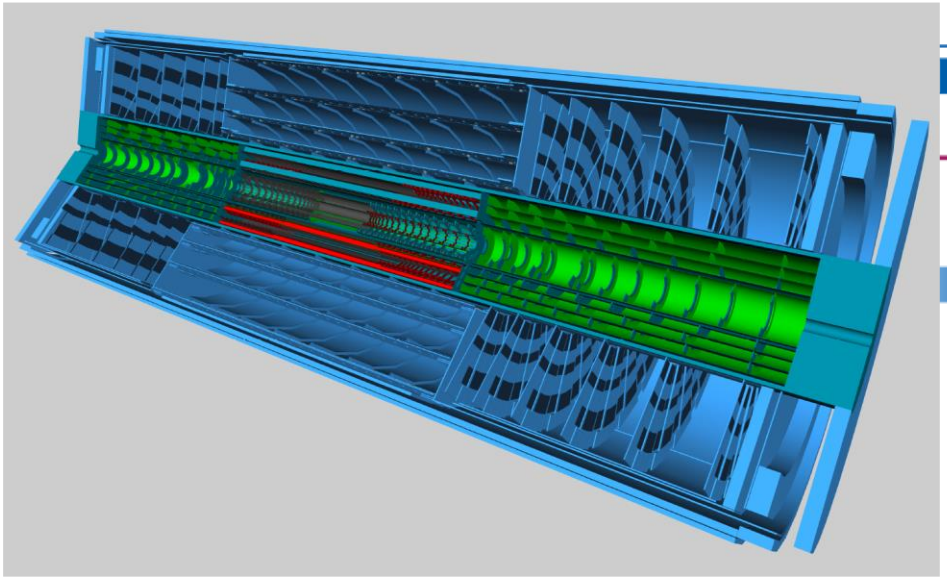

LHC
HL-LHC
Run 1
Run 2
Run 3
Run 4 - 5...
LS1
EYETS
LS2
LS3
7 TeV
8 TeV
13-14 TeV
14 TeV
14 TeV
energy
splice consolidation
button collimators
R2E project
injector upgrade
cryo Point 4
Civil Eng. P1-P5
cryolimit
interaction
regions
HL-LHC installation
5 to 7 x
nominal
luminosity
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2037
radiation
damage
75%
nominal
luminosity
experiment
beam pipes
nominal luminosity
experiment upgrade
phase 1
2 x nominal luminosity
experiment upgrade
phase 2
30 fb-1
150 fb-1
300 fb-1
3000 fb-1
integrated
luminosity

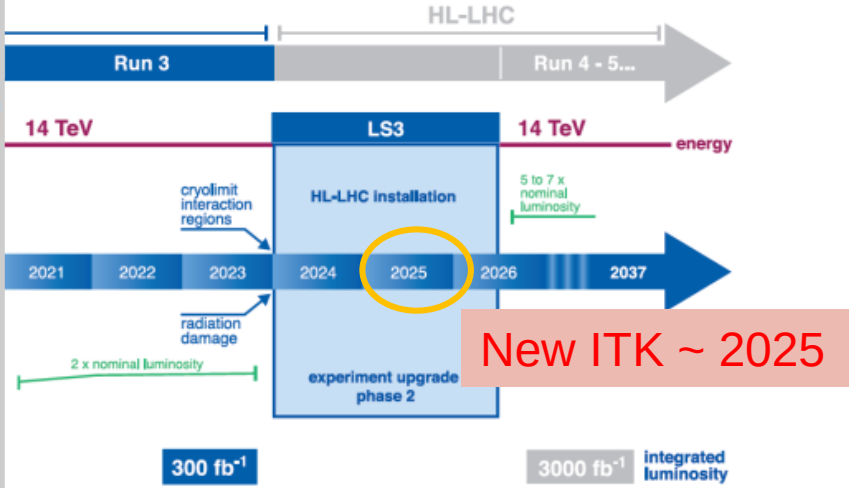
ITk tracker



New ITK ~ 2025

ITk tracker





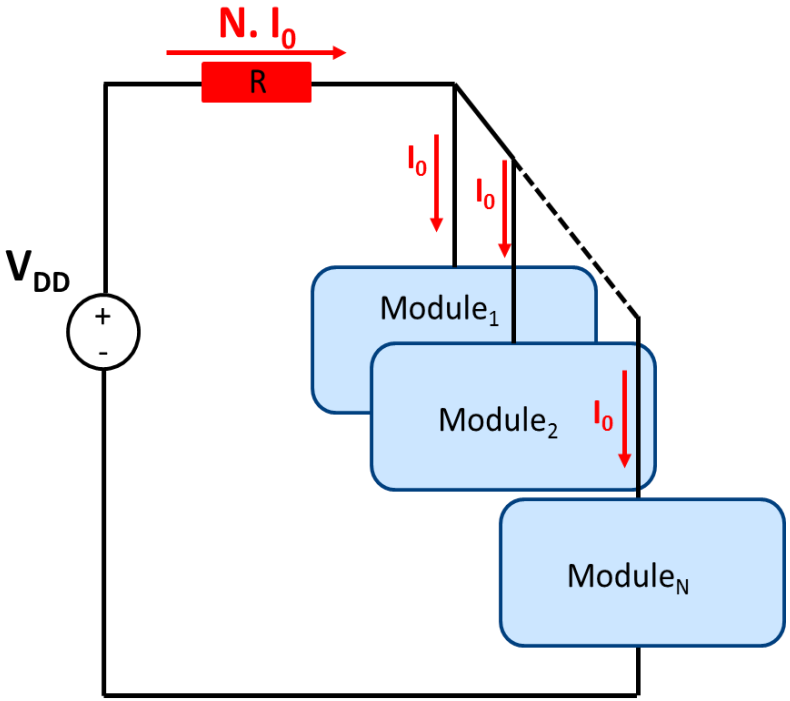
- New tracker for HL-LHC based on **silicon only technologies**.
- The new pixel detector will have **5 layers (Lo to L4)**.
- Upgraded hybrid detectors using **RD53 IC** will be used for the first 4 layers.
- Possibility of using **CMOS Depleted Monolithic Active Pixel Sensors** in L4: on-going discussion.
- Finalizing and preparing for **production**.

	ATLAS-HL-LHC	
	Outer	Inner
Required Time Res. [ns]	25	25
Particle Rate [kHz/mm^2]	1000	10 000
Fluence [n_{eq}/cm^2]	10^{15}	10^{16}
Ion. Dose [Mrad]	80	1000

Why choose Serial Powering?

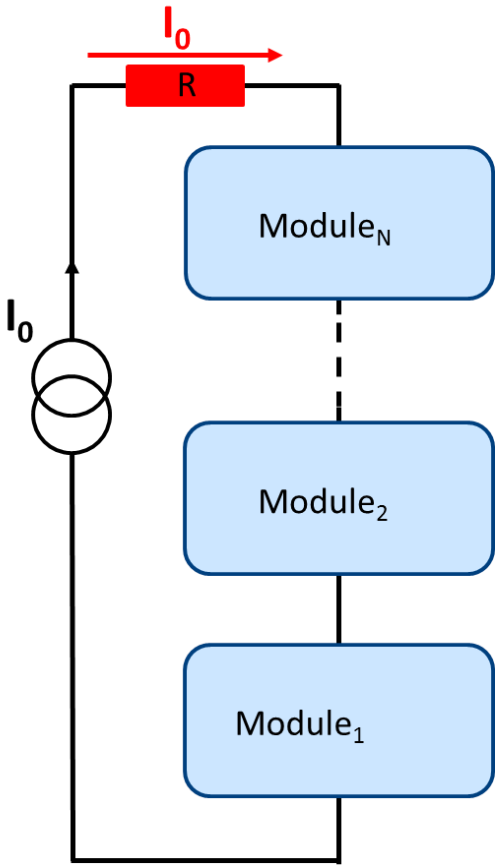
Traditional: Parallel Powering

Big power loss in cables!!!



In ITk: Serial Powering

Small power loss in cables!!!



In the present ATLAS pixel detector, the power efficiency is around 20%

Increases power efficiency and reduces material budget

Why choose Serial Powering?

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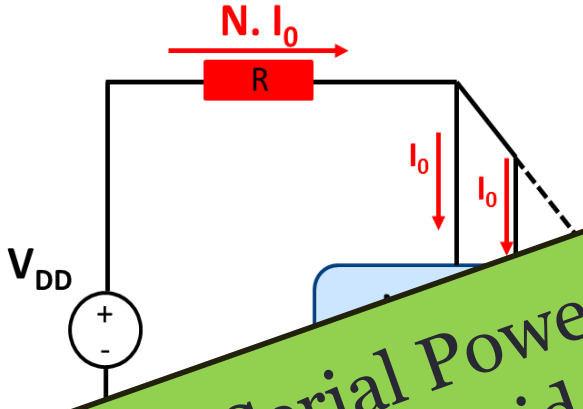
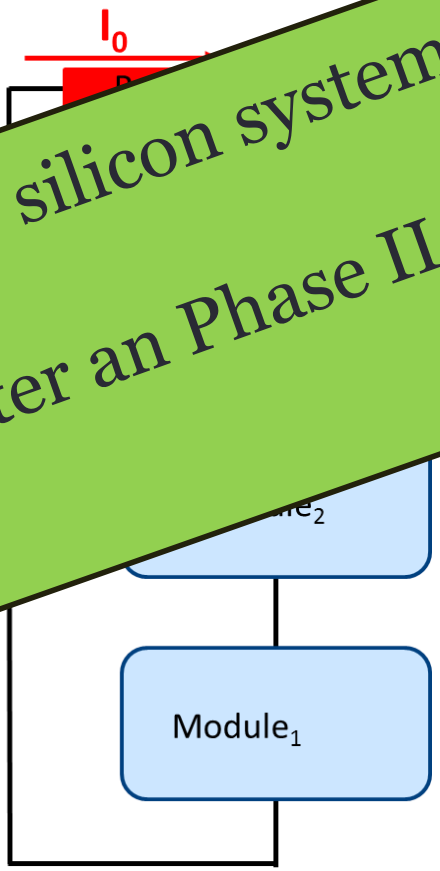


In ITk: Serial Powering

Small power loss in cables!!!



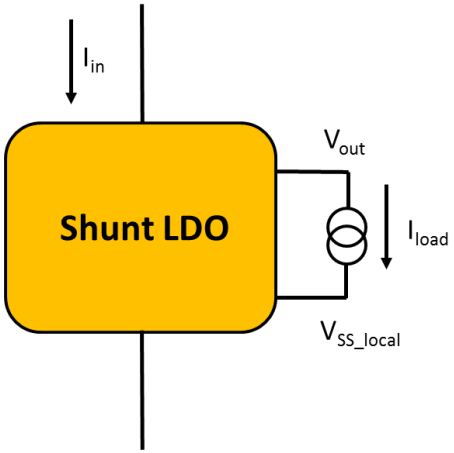
Need for Serial Powering for HL-LHC silicon systems considered self evident.
Parallel Powering no longer used after an Phase II upgrade.

…e present ATLAS pixel detector, the power efficiency is around 20%

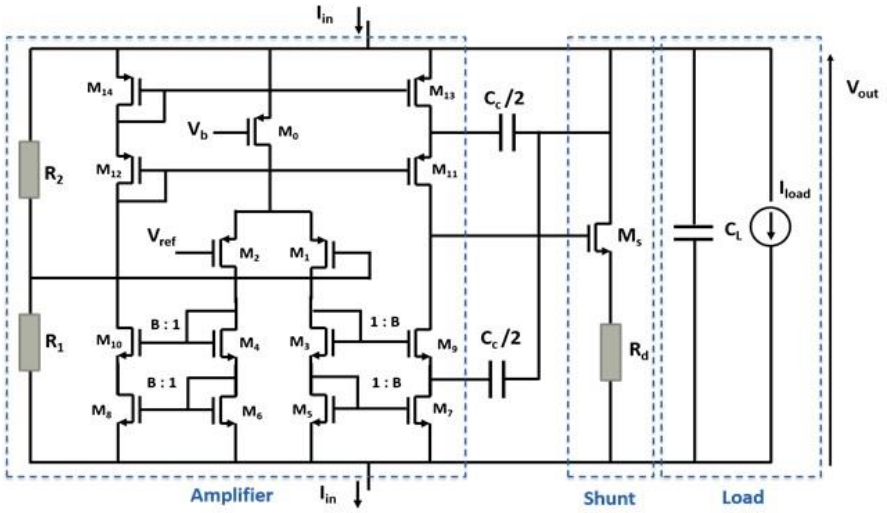
Increases power efficiency and reduces material budget

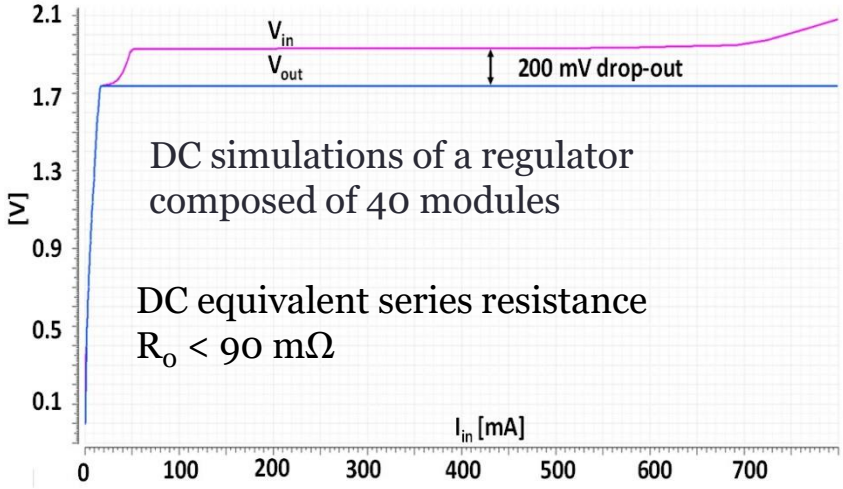
Shunt-LDO : to power electronics

Main idea

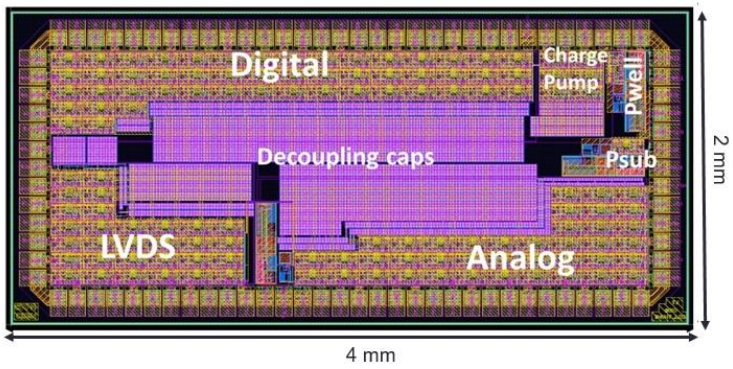


A. Habib, CPPM





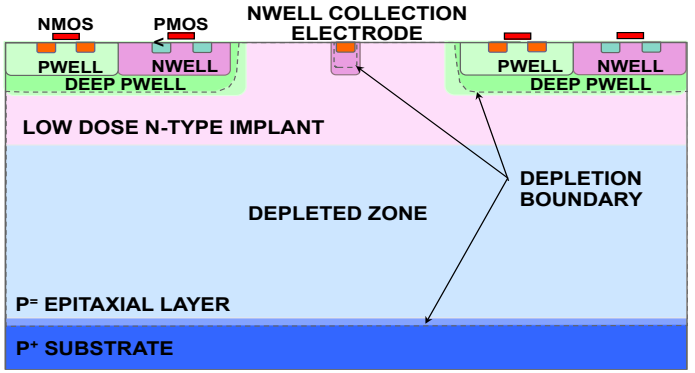
S.Bhat & A. Habib, CPPM



Submitted in August 2018!

TJ initial modified process

- Novel modified process developed in collaboration with the foundry.
- Adding a planar **n-type layer** significantly improves depletion under deep pwell.
- Pixel dimensions:
- 36 x 42 µm^2 pixel size
- 3 µm diameter electrodes
- Measured capacitance < 5fF

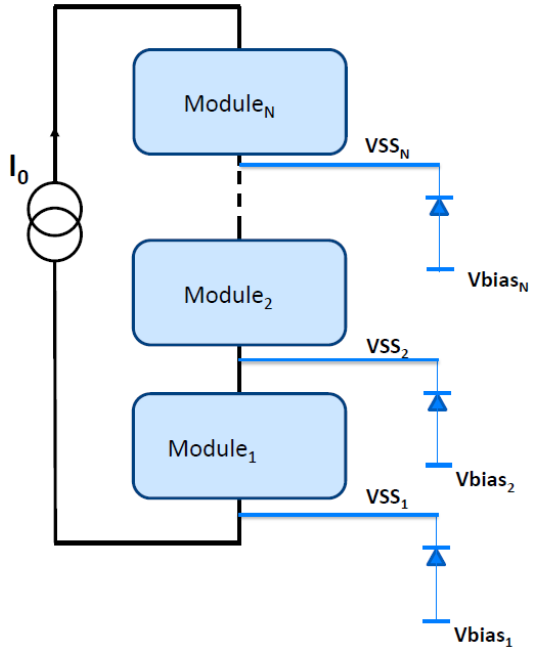


W. Snoeys et al., NIM A871 (2017) 90 – 96.

In order to polarize the sensor in same way

- (VSS_N – $Vbias_N$) must be constant.
- Since VSS_N is shifted every module

We cannot use the same bias for all modules.



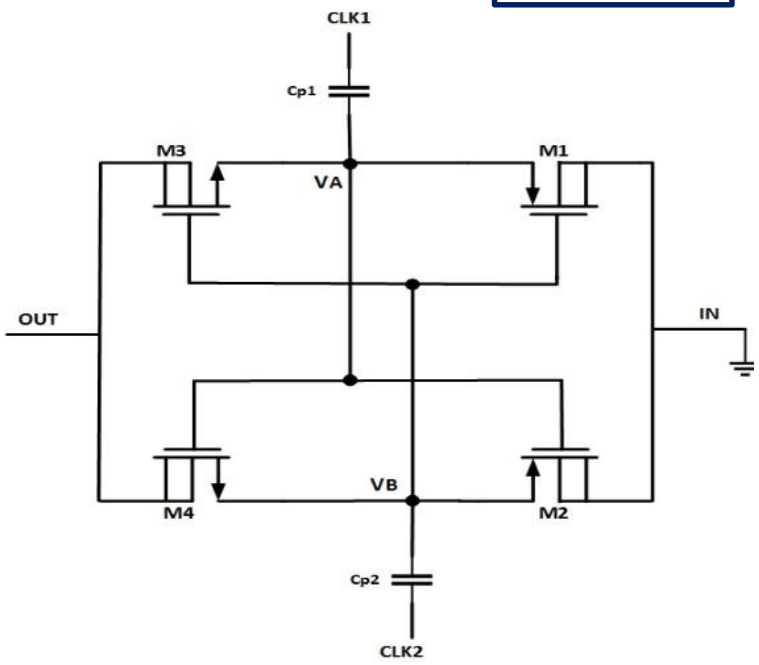
Requirements for Sensor

- HV to pwell = -6 V
- HV to substrate = -20 V

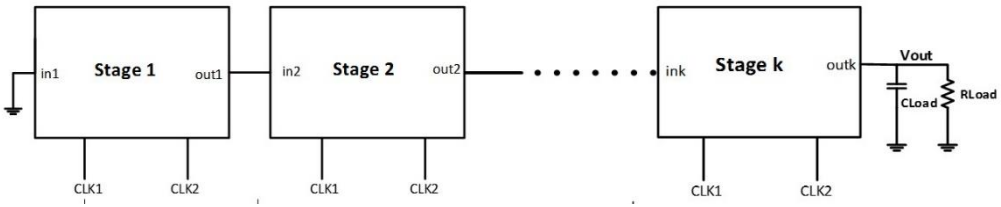
Charge Pump : to power sensor

S. Bhat, CPPM

- Cross-coupled architecture of charge pump.
- Two parallel, complementary cross-coupled parts operate in opposite phases.
- The charge pump has several stages.
- The operating frequency is 640 MHz.



Generating higher voltages



$$Vout = N * Vdd - N\frac{I_L}{f * Cp}$$

# of stages

Pumping frequency

Simulation results

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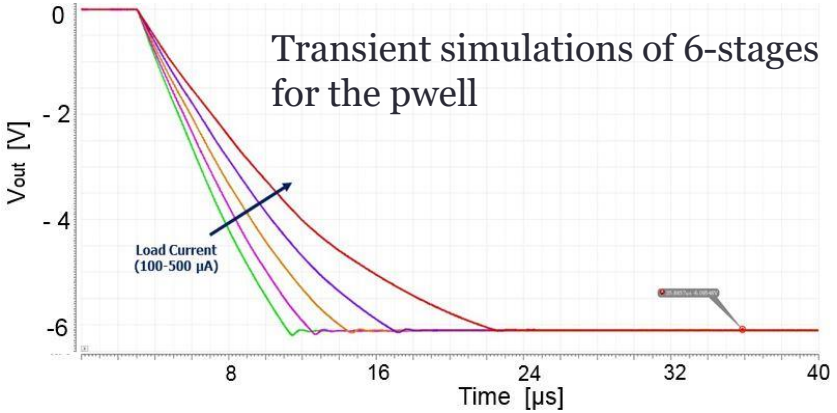
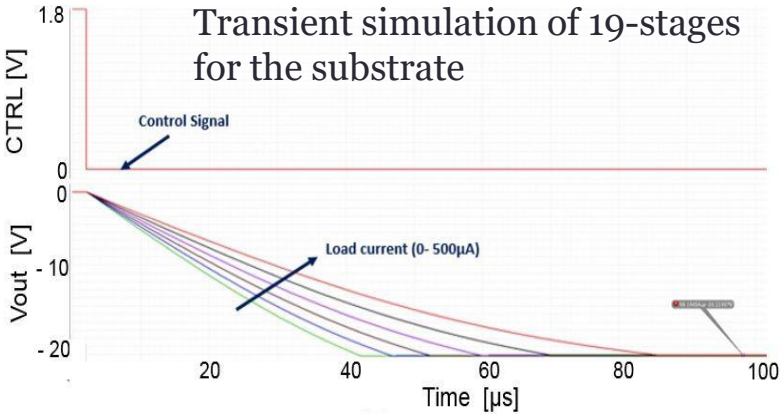
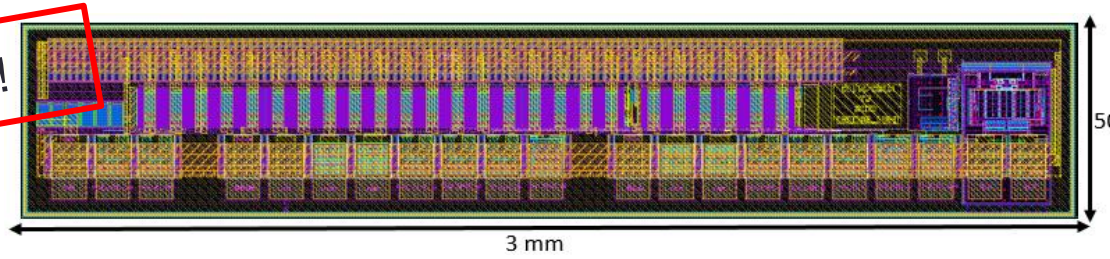
Three test structures:

- 6-stages charge pump
- 19-stages charge pump
- SWITCH





Submitted in August 2018!



Milestone 2

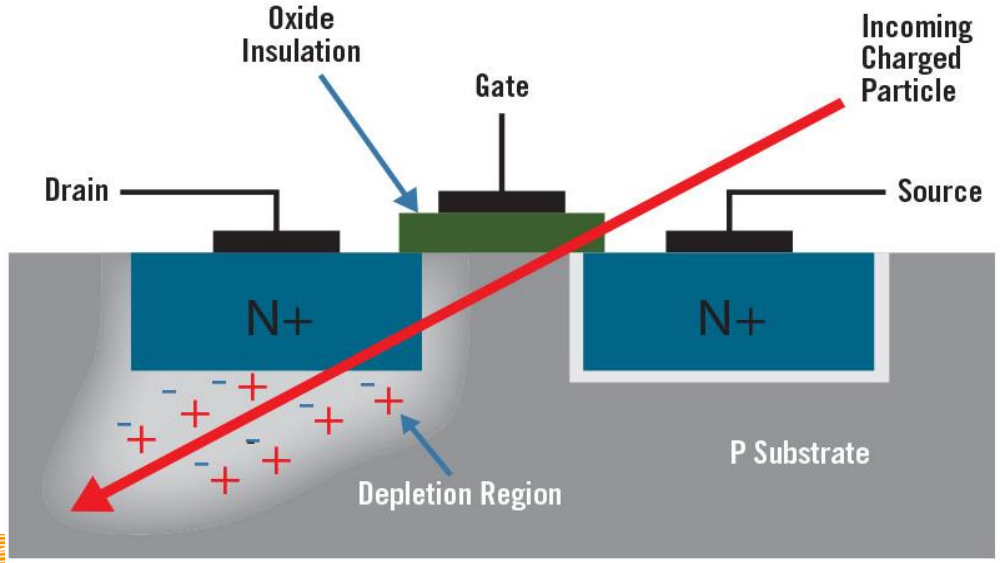
Single Event Upset (SEU) mechanism

- Energetic particle strikes ⟶ Creates ionization path with free e^- and holes

↓

Creates single event transient (SET)

"Change in memory state"



https://www.lanl.gov/science/NSS/issue1_2012/story4full.shtml

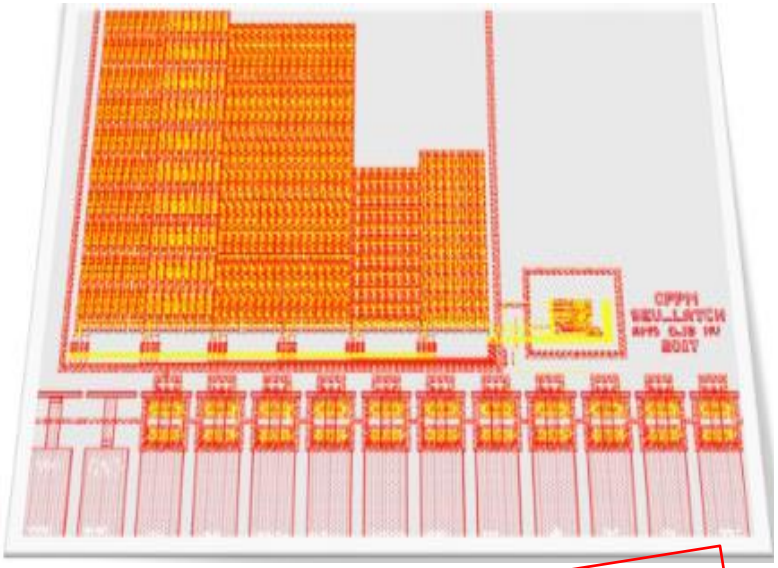
SEU tolerant memories in AMS 0.18 µm

- Block size : 1.3 mm × 1 mm

Different flavors of latches:

- Col6 : DICE Latch "Dual Interlocked Storage Cell"
- Col5 : Standard Cells "LHX1_HV"
- Col4 : SPLIT Triple redundancy with standard cells
- Col3 : SPLIT Triple redundancy with standard cells
- Col2 : Triple redundancy standard cells
- Col1 : Triple redundancy DICE latch

P. Pangaud & S. Bhat, CPPM



Received end of Sep 2018!

- **Additional Functions**
  - Columns selector
  - Digital buffer output
  - DeepNwell and HV

SEU tolerant memories in TowerJazz 0.18 µm

- Block size : 1 mm × 1.3 mm

Different flavors of latches:

- Col6 : DICE Latch "Dual Interlocked Storage Cell"
- Col5 : Standard Cells
- Col4 : SPLIT Triple redundancy with DICE cells
- Col3 : SPLIT Triple redundancy with standard cells
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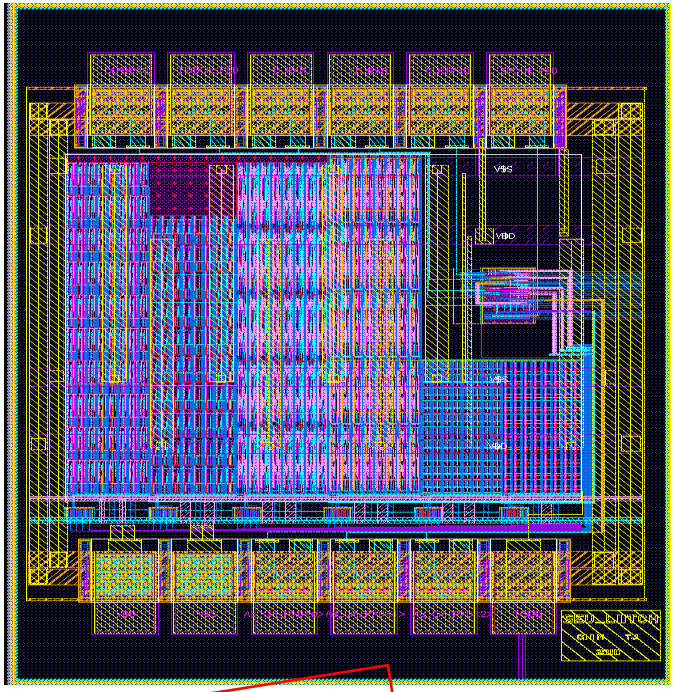
S. Bhat & P. Pangaud, CPPM



Submitted end of Aug 2018!

- **Additional Functions**
  - Columns selector
  - Digital buffer output

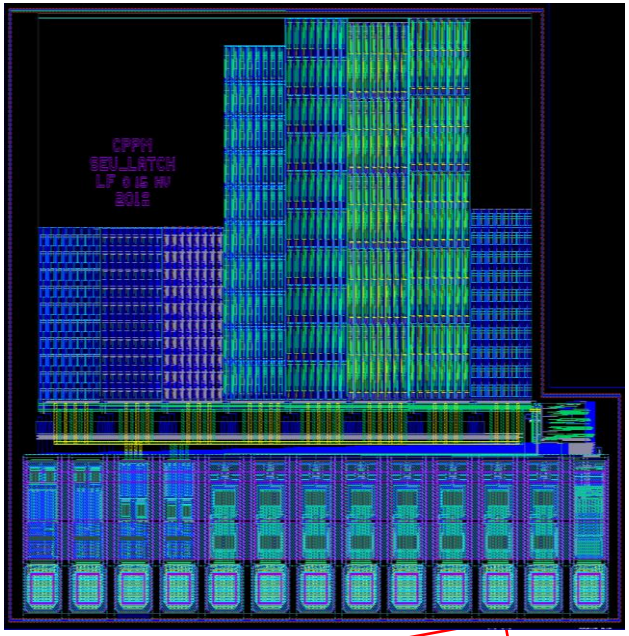
SEU tolerant memories in LFoundry 0.15 µm

- Block size : 1.3 mm × 1 mm

Different flavors of latches:

- Col8 : SRAM
- Col7 : SPLIT Triple redundancy with DICE cells
- Col6 : SPLIT Triple redundancy with standard cells
- Col5 : Triple redundancy with DICE cells
- Col4 : Triple redundancy with standard cells
- Col3 : Enhanced DICE Latch
- Col2 : DICE Latch "Dual Interlocked Storage Cell"
- Col1 : Standard Cells

S. Bhat & P. Pangaud, CPPM

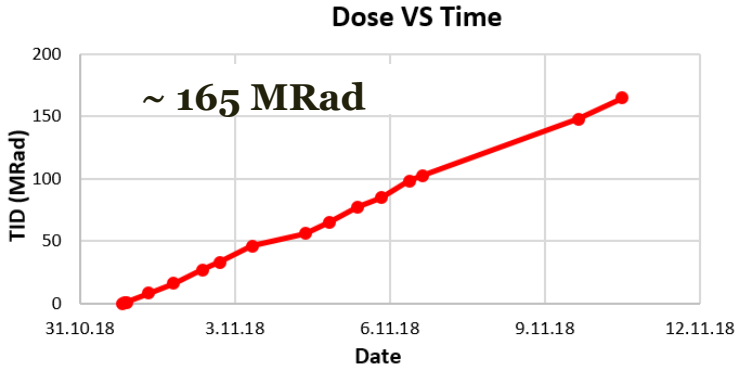


Submitted 21th Jan 2019!

- **Additional Functions**
  - Columns selector
  - Digital buffer output

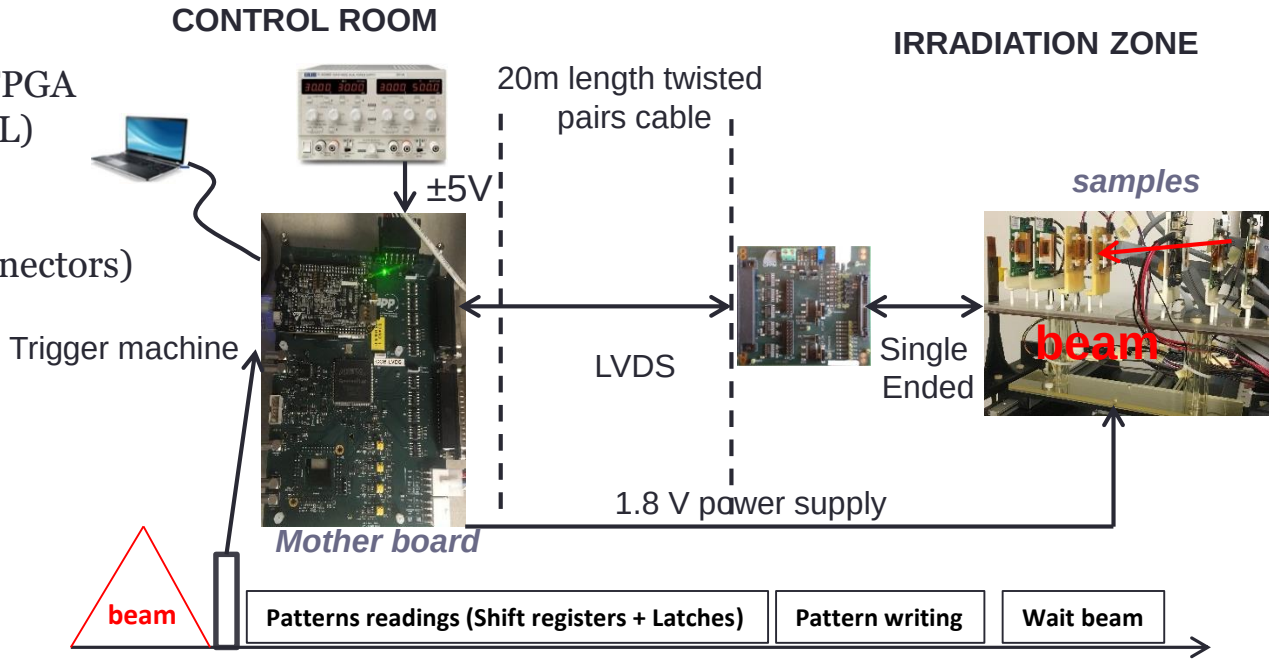
Experimental Setup

- **24 GeV protons beam line at CERN (east zone PS)**
  - beam size 1cm²
  - mean dose rate 1.1 MRad/hr
  - TID: 165Mrad
  - exposure time 10 days
  - 2 AMS chips were installed



Dose does not affect the behavior of the AMS SEU chip

- **Mother board V2**
  - Collaboration with LAPP
  - nanoPC BeagleBone card + FPGA
  - Flexible programming (VHDL)
  - Digital signals
    - 40 TTL signals
    - 32 LVDS signals (DB-37 connectors)
  - Analog channels
    - 4 SAR ADC (16 bits)
    - 10 DAC (16 bits)
  - Lab tests + irradiation tests



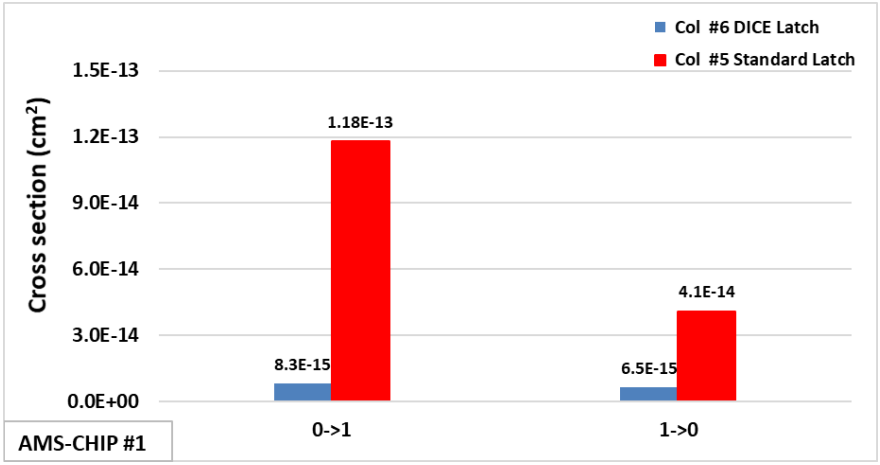
- **Test sequence:**

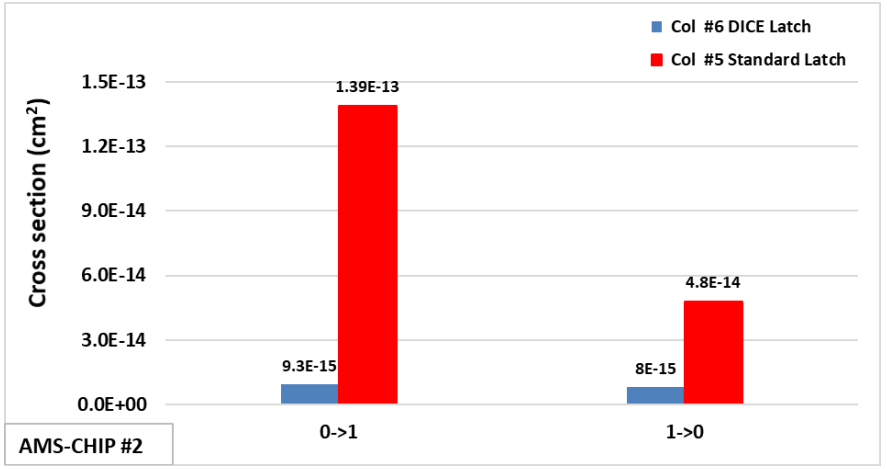
DICE test results

- We stored enough data to extract an acceptable statistic for SEU.

  - 80 cells per type of latch and we reached a spill number > 10000.

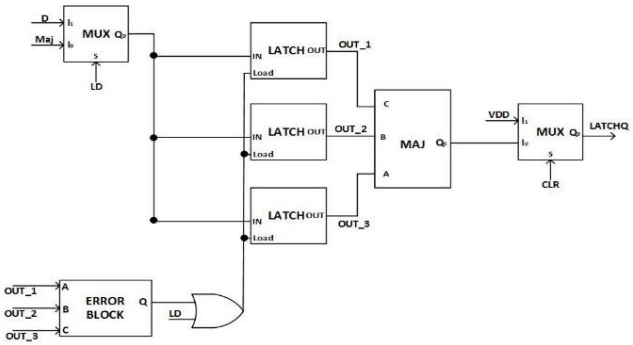
- Both the chips show similar behavior under the beam.
- Cross section of the standard latch **~ 66.5 E-15 cm²**
- Cross section of DICE latch **~ 4.7 E-15 cm²**



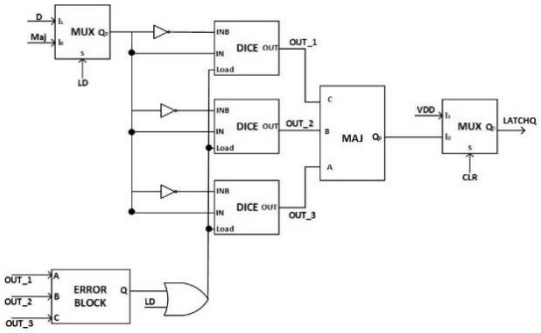


DICE is x 15 more robust than the Standard Latch

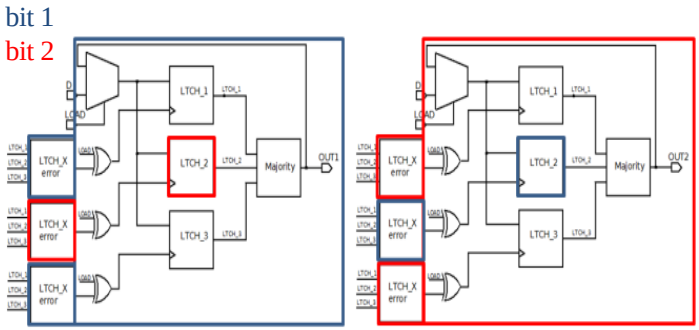
TRL versions



TRL with standard latch

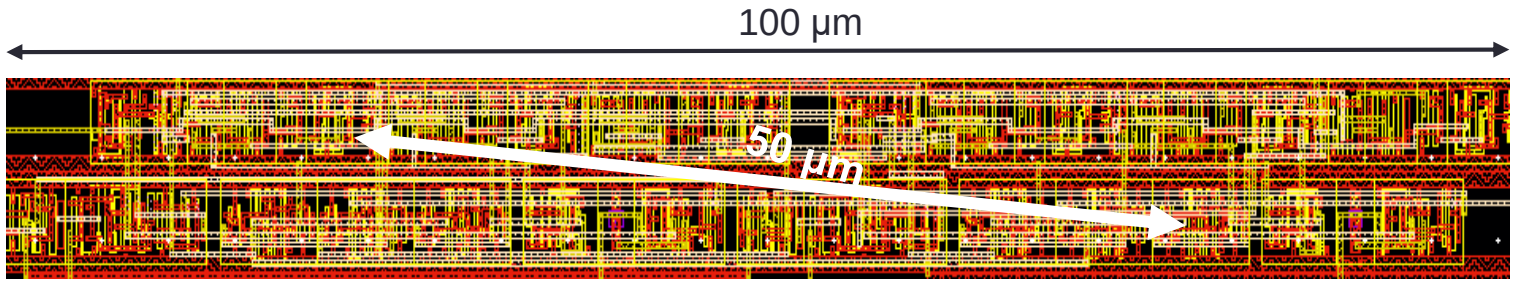


TRL with DICE latch



SPLIT TRL with standard latch

- 3 TRL versions have been designed and tested at CERN.
  - TRL with standard latch.
  - 2nd version with DICE latch.
  - 3rd version: triplication of the standard latch and increasing the distance between a minimum distance between 2 bits (~50 µm).



TRL test results

- We stored enough data to extract an acceptable statistic for SEU.

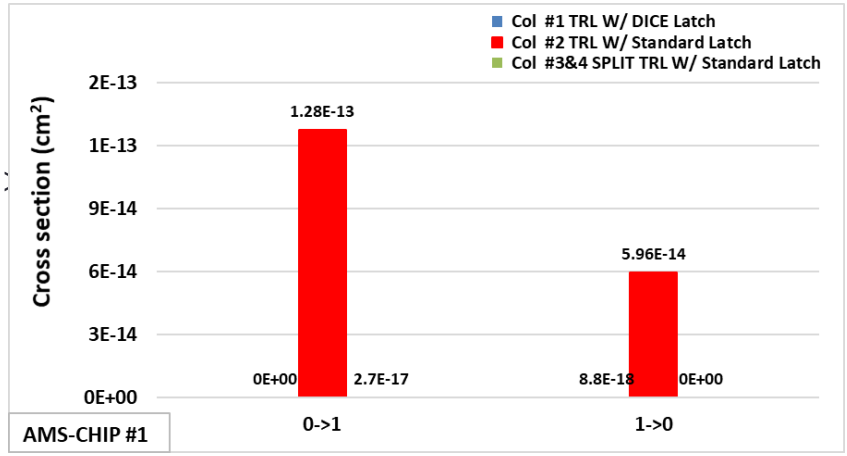
- 80 cells per type of latch and we reached a spill number > 10000.

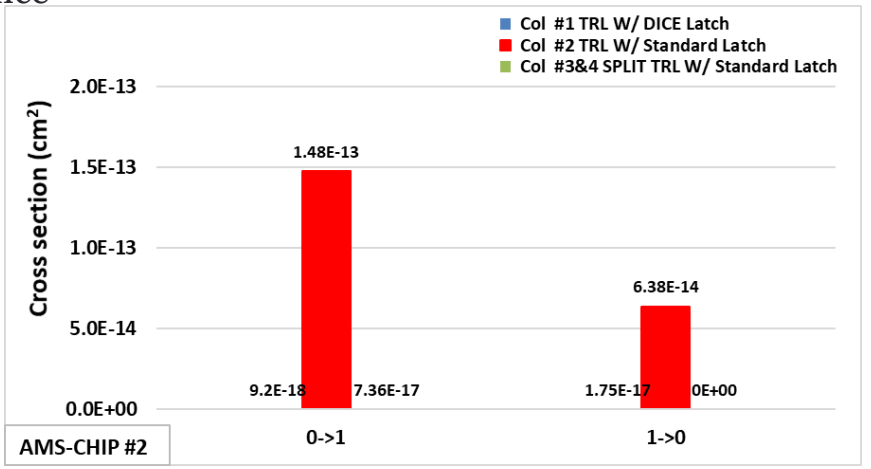
- Both the chips show similar behavior under the beam.

- Cross section of the TRL W/ standard latch: **~ 14.8 E-14 cm² (Defect in the design)**

- SPLIT TRL W/ standard latch shows very good performance with the cross section **~ 7.3 E-17 cm²**

- TRL W/ DICE latch shows very good performance as well with the cross section **~ 1.7 E-17 cm²**





TRL W/ DICE is ~x3000 robust than the Standard Latch

Conclusion

- **Serial Powering** is necessary for ATLAS ITk detector.

- **Shunt-LDO Regulator for Electronics** :
  - The block is able to generate constant voltage **of 1.8 V upto 1.5 A of input current for Serially Powering** CMOS modules in ATLAS ITk .
  - A test chip was submitted in a MPW submission in Aug 2018.

- **Charge Pump for Sensor Bias** :
  - From the simulations ➔ 2 versions of the charge pump circuit show stable response wrt sensor leakage current **upto 500 µA.**

- **SEU - Radiation Hard Cells** :
  - Designed Single Event Upset tolerant test chips in AMS/TJ/LF technologies in order to study the different architectures for various technologies.

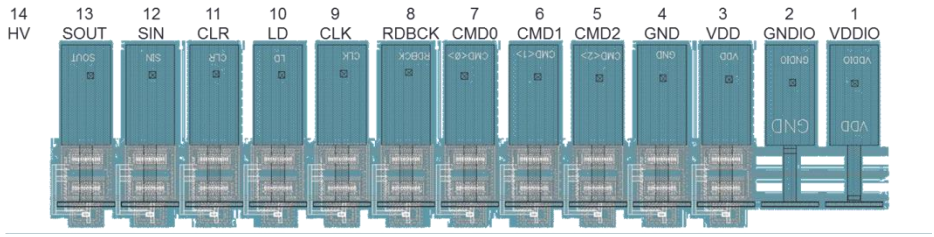
- From the measurements of AMS, the designed DICE latch showed very promising results compared to standard latch.
- Keeping the area almost same as standard latch, the **DICE is ~ 15x immune to SEU.**
- Recently, submitted the 2 SEU test chips in a MPW submission in TJ and LF technology.

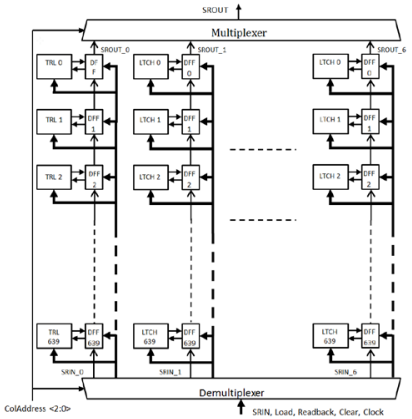
Outlook

- Testing of Shunt-regulator and charge pump test chips in a Serial Powering .
- Testing of SEU test structures in TJ and TSI technologies under the proton beam.

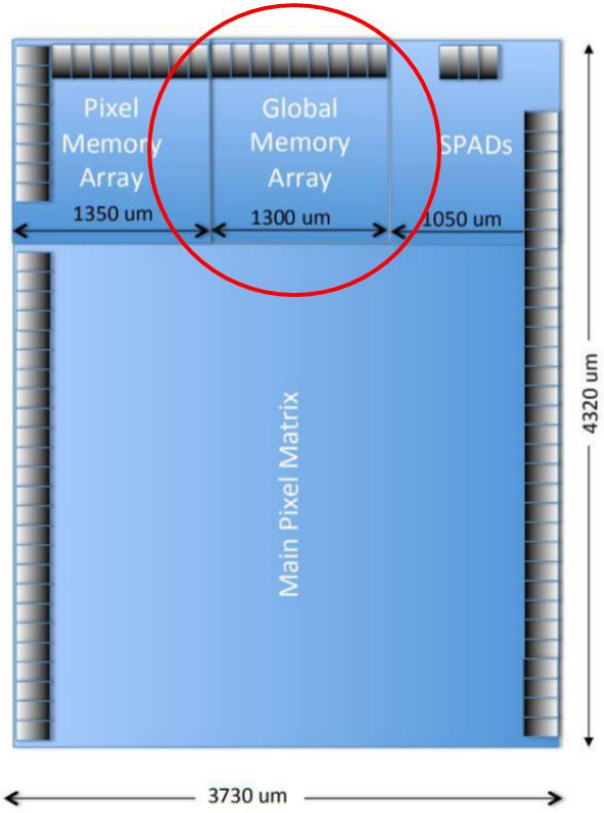
Backup

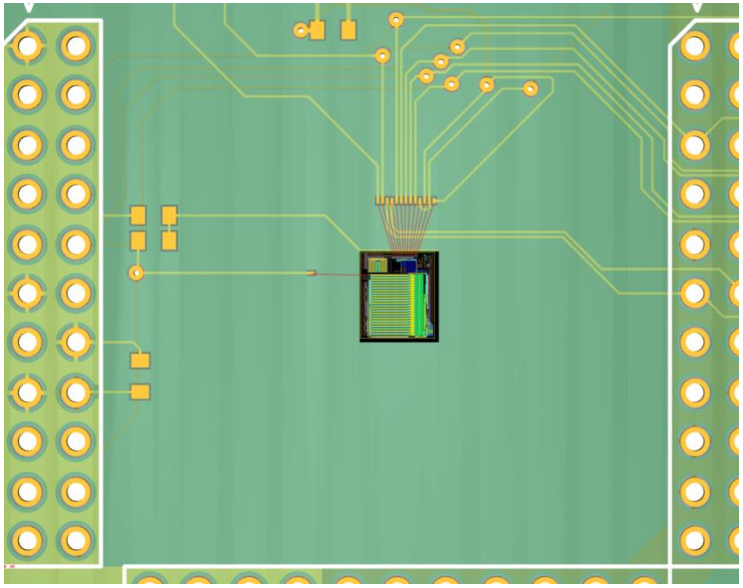
ATLASpix2 and Test Board





LD	IN	Load	Data loading
CK	IN	Clock	
RDBCK	IN	ReadBack	Latches data loading in SR
CLR	IN	Clear	Reset

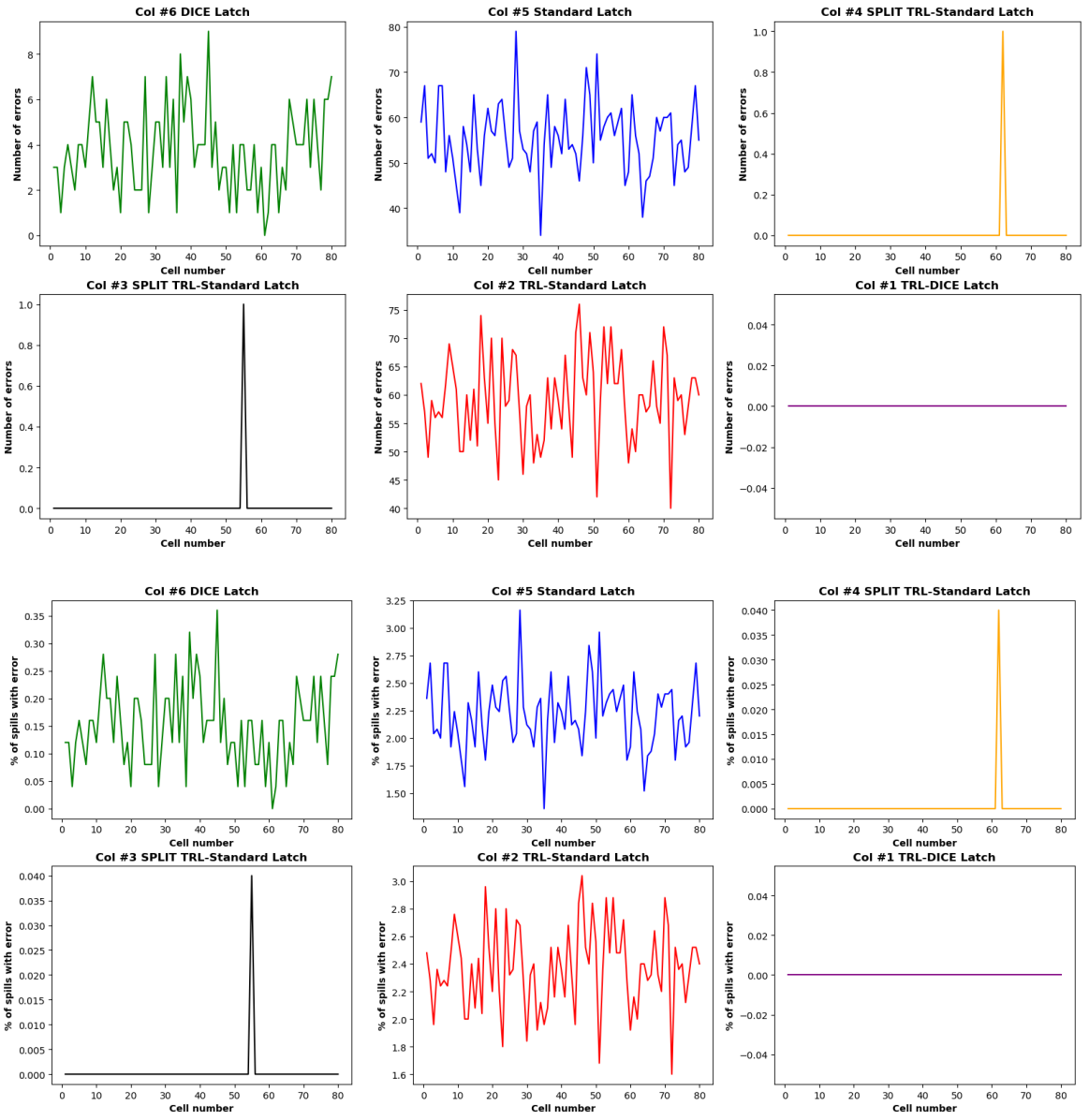




Errors with pattern all “0” for Chip #2

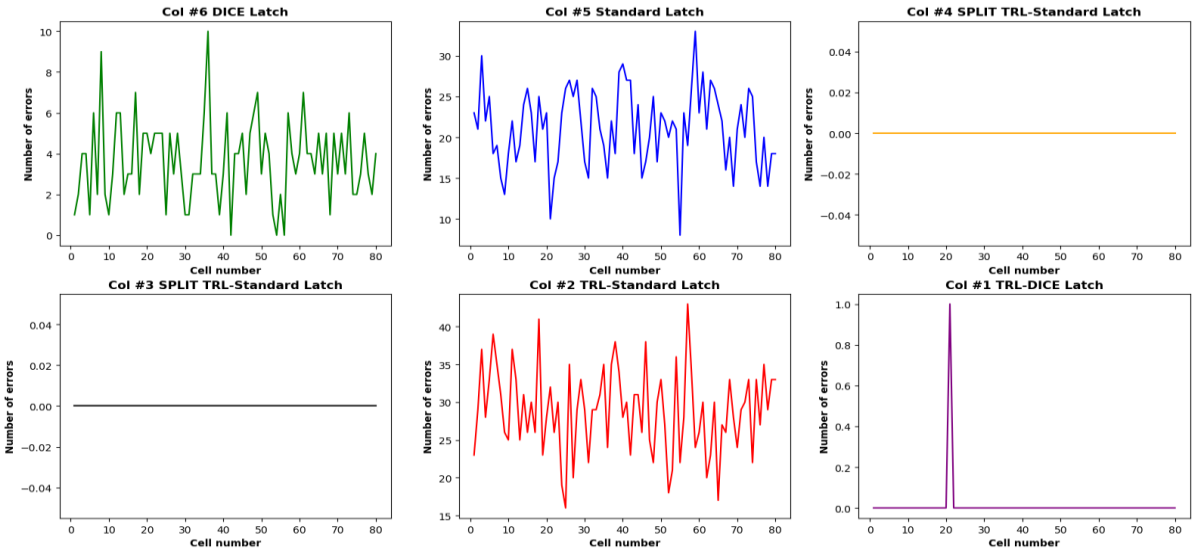
- # errors VS the cell # is shown.
- Col#5 and col# 2 shows similar behaviour.
- # acquisitions : 2500
- # spills : 2500
- Col #1,#3, #4 **are very robust.**

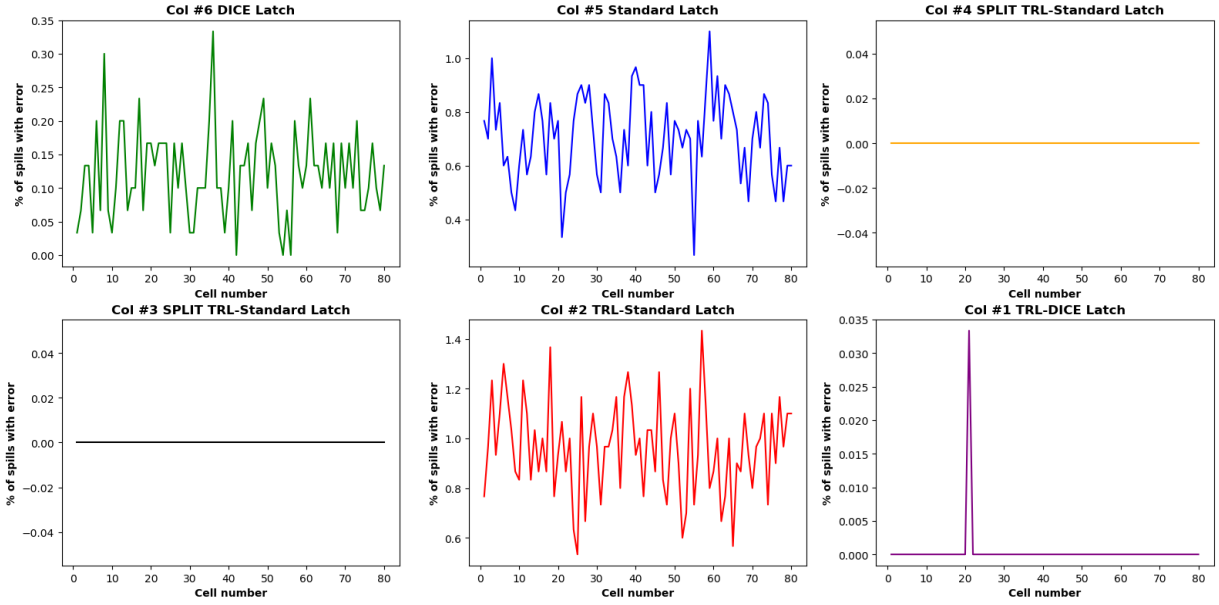
- % spills W/ errors VS cell # is shown.



Errors with pattern all “1” for Chip #2

- # errors VS the cell # is shown.
- Col#5 and col# 2 shows simil behaviour.
- # acquisitions : 3000
- # spills : 3000
- Col #1,#3, #4 **are very robust.**

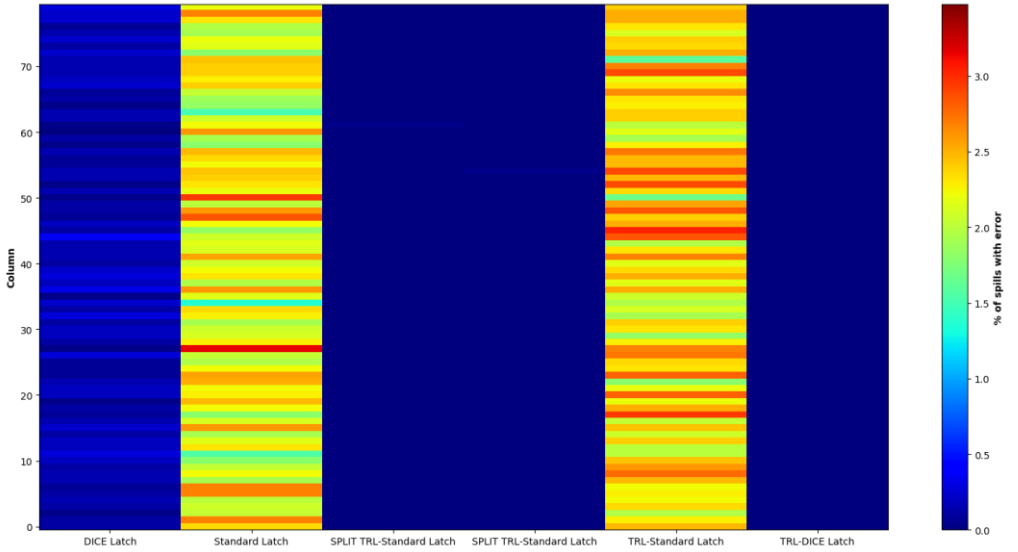




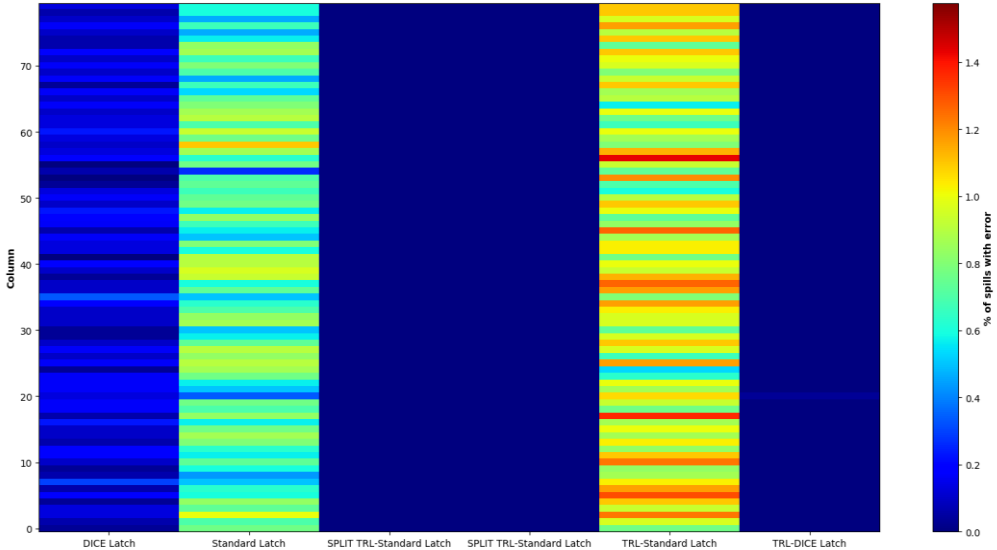
Error mapping for all “0” and all “1” for chip#2

- # errors VS the cell # is shown.
- Col #5 and col # 2 shows similar behaviour.
- # acquisitions > 3000.
- # spills ~ 3000
- Error variation between DICE and standard latch can be seen.
- Col #1, #3, #4 **are very robust.**

All “0” pattern

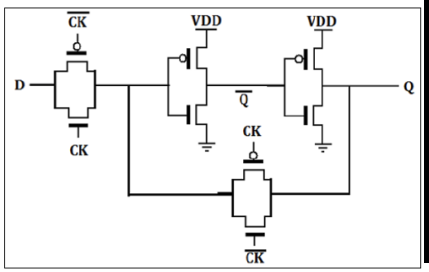


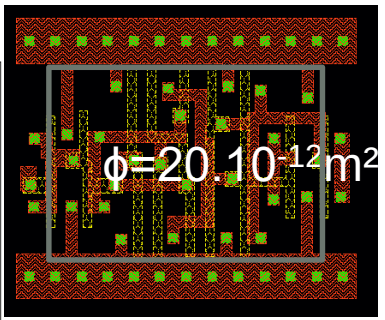
All “1” pattern



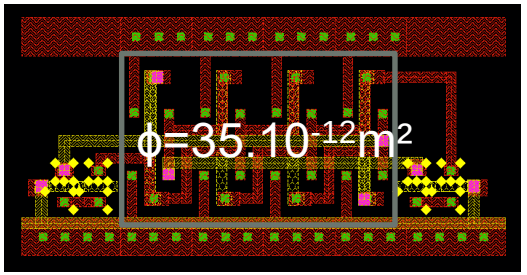
Latch(s) description

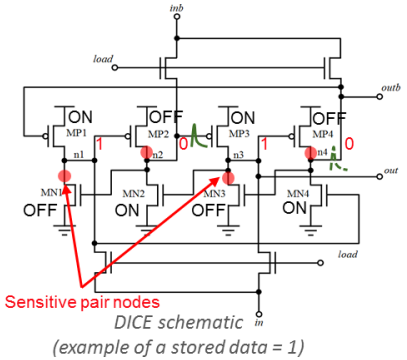
- Standard cell "LHX1_HV" from the CORELIB_HV Lib
- Active area $\phi=20.10^{-12}$ m²





- DICE "Dual Interlocked Storage Cell" cell
- DICE latch structure is based on the conventional cross coupled inverters: Active area
  - The charges deposited by a ionising particle strike one node can't be propagated due to the stability of this architecture.
  - If 2 sensitive nodes (corresponding to the OFF transistors drain area) are affected simultaneously, the immunity is lost and the DICE latch is upset

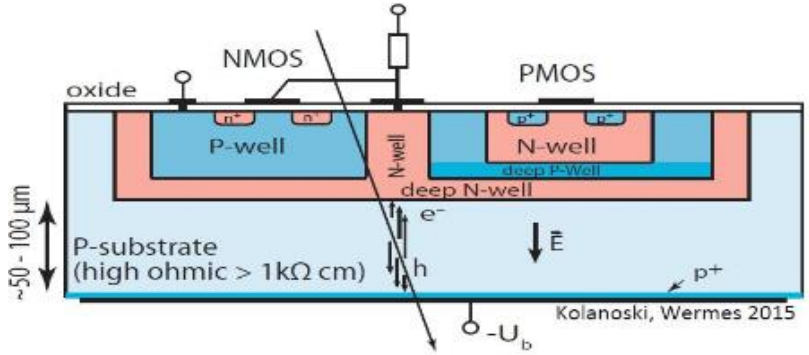




We expect to gain by 5 the BER robustness (Standard cell "LHX1_HV" is the reference)

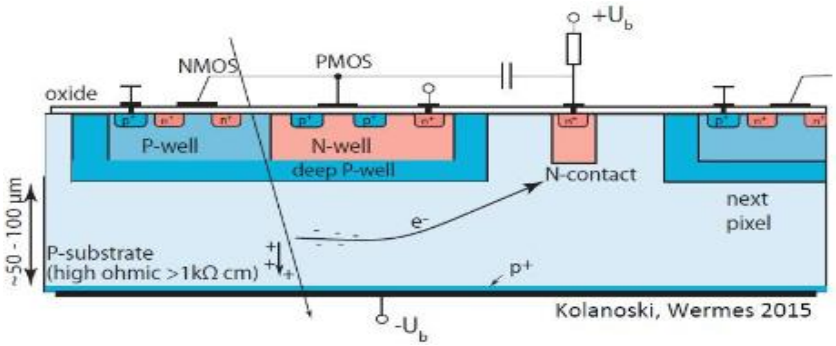
Depleted Monolithic Active Pixel Sensors (DMAPS)

2 lines of development followed : (a) large electrode design / (b) small electrode design



- matured over several years
- radiation hardness (TID & NIEL) proven
- rate capability for L4 (and even L3/L2) shown
- timing close to specs

(→ LF / AMS)



- very promising wrt. timing and power
- Vendor already established at CERN
- rate capability for L4 (and even L3/L2) shown
- fast timing due to small C
- radiation hardness -> Sept. 2018

(→ TJ)

Column # (Design)	Area (μm^2)	Distance b/w 2 sensitive nodes (D_2N- µm)
1. TRL W/ DICE latch	400	20
2. TRL W/ standard latch	360	8
3. SPLIT TRL W/ standard latch	500	50
4. SPLIT TRL W/ standard latch	500	50
5. Standard latch	20	-
6. DICE latch	30	3.5