Sidewall Spacer NVM Characterization and Modeling

Tommaso Vincenzi

24/01/2019

Confidential © ams AG

Agenda

- Introduction
- Bit Cell Testing
- Early Results
- Second Testchip
- Testing Sources
- NVM Modeling
- Conclusions

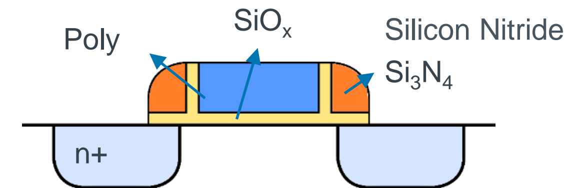
Confidential © ams AG

Introduction

Radiation Hard Non-Volatile Memory Design

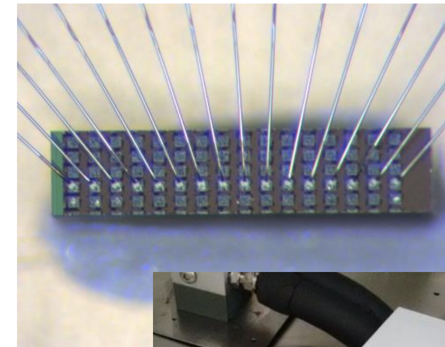
Objective:

The objective is understanding how the novel Sidewall Spacer Memory Bit Cell (SwSpc) is affected by Total Ionizing radiation Dose (TID) and design a full radiation tolerant memory IP.



Main tasks:

- Characterization of Bit Cell tolerance to TID
- Physics Based Model development of the Bit Cell

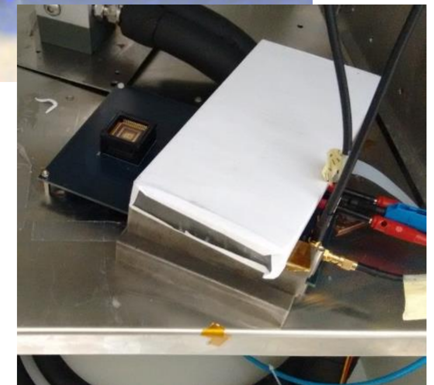


Contract duration:

July 2016 – December 2018 (30M)

Next steps:

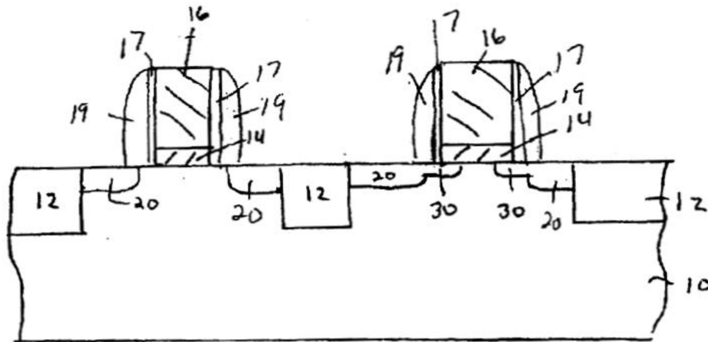
Collaboration with NSCore (Fukuoka, JP) on the development of a full Memory IP
February 2018 – April 2018



Confidential © ams AG

Introduction

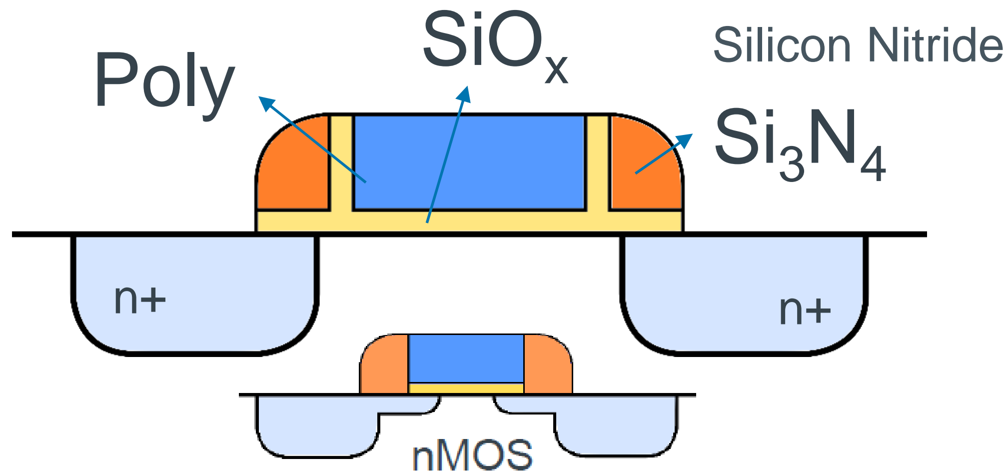
US 6,518,614 B1



EMBEDDED ONE-TIME PROGRAMMABLE NON-VOLATILE MEMORY USING PROMPT SHIFT DEVICE

Inventors: **Matthew J. Breitwisch**, Essex Junction, VT (US); **Bomy A. Chen**, Ridgefield, CT (US); **Chung H. Lam**, Williston, VT (US)

Assignee: **International Business Machines Corporation**, Armonk, NY (US)

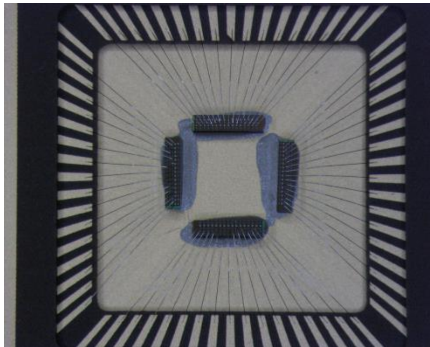


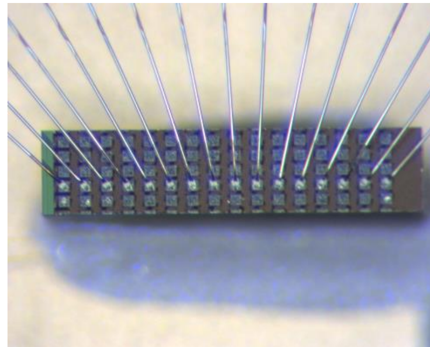
The patent can be used for bit cell development in multiple technologies due to ams/IBM patent license agreement

STREAM

ams

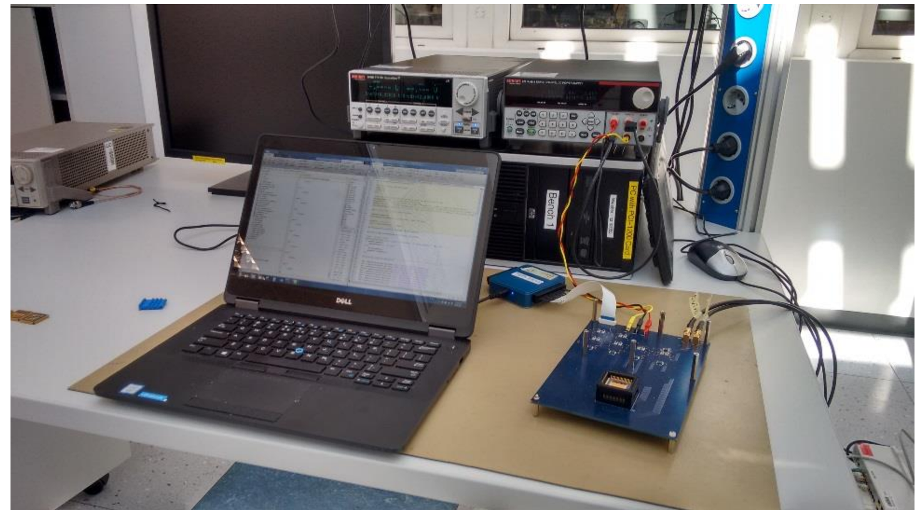
BitCell Testing





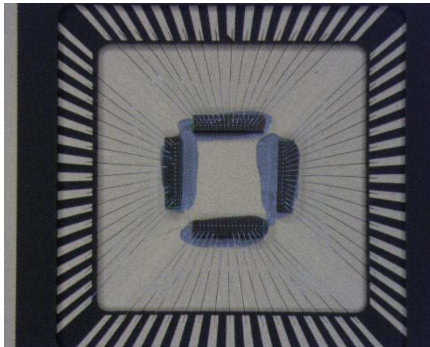
Arrays are available and have been tested electrically.

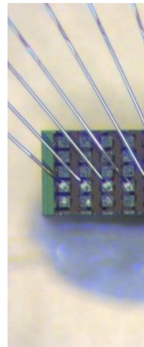
The radiation test setup measurement agrees with on-wafer measurements.

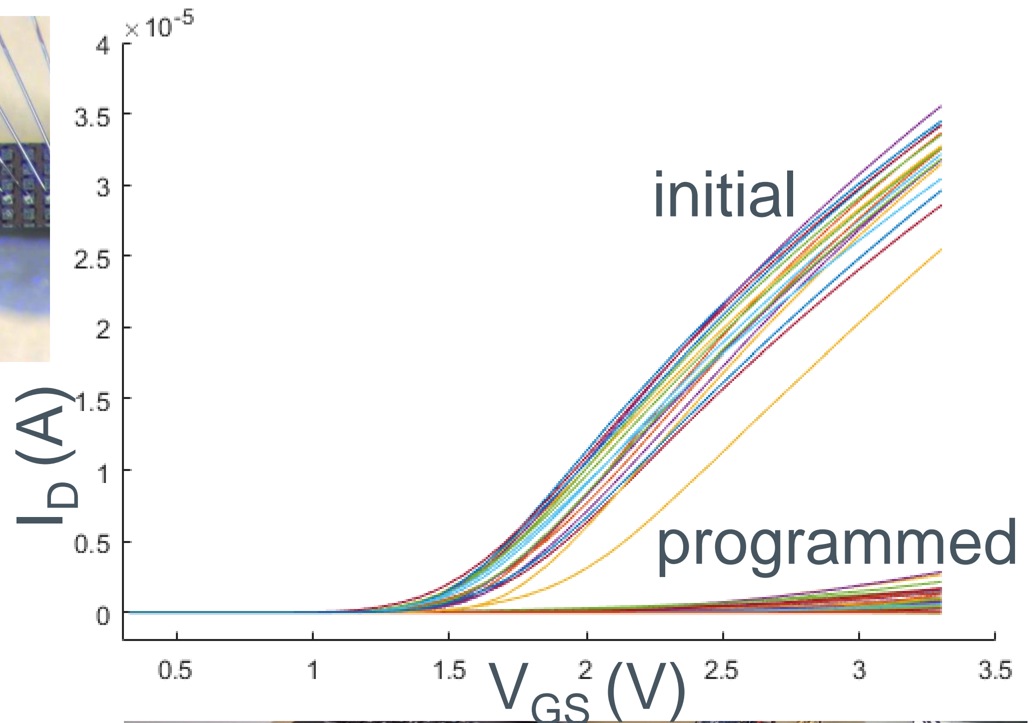


Confidential © ams AG

BitCell Testing

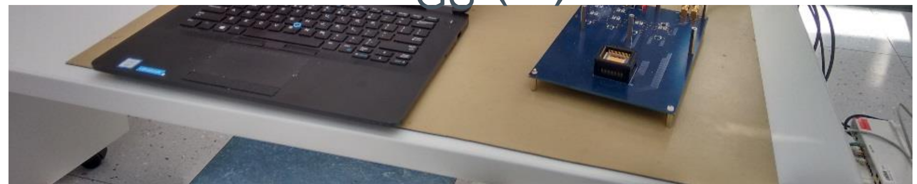






Arrays are available and have been tested electrically.

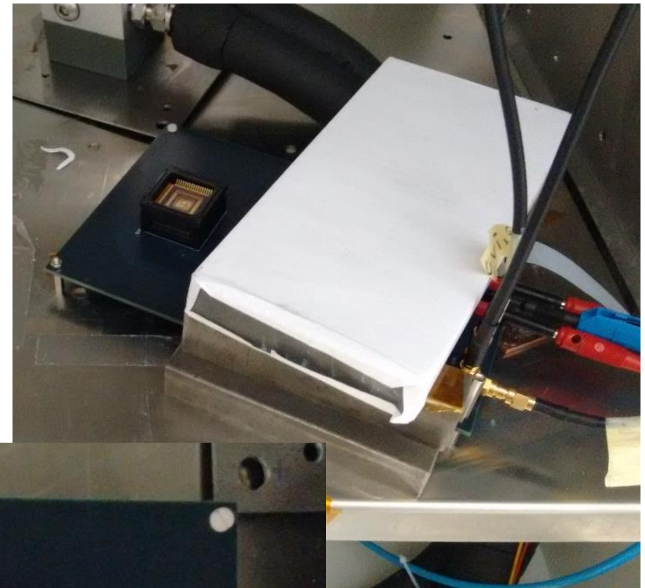
The radiation test setup measurement agrees with on-wafer measurements.

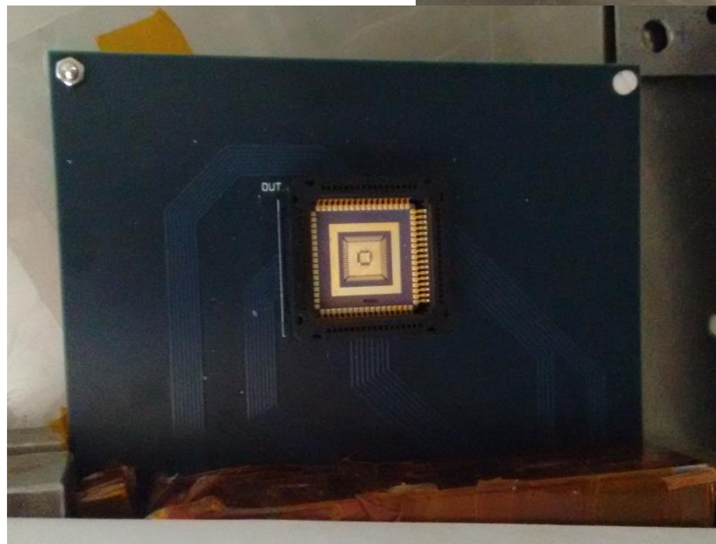


Confidential © ams AG

BitCell Testing

60 keV wide angle calibrated X-ray source



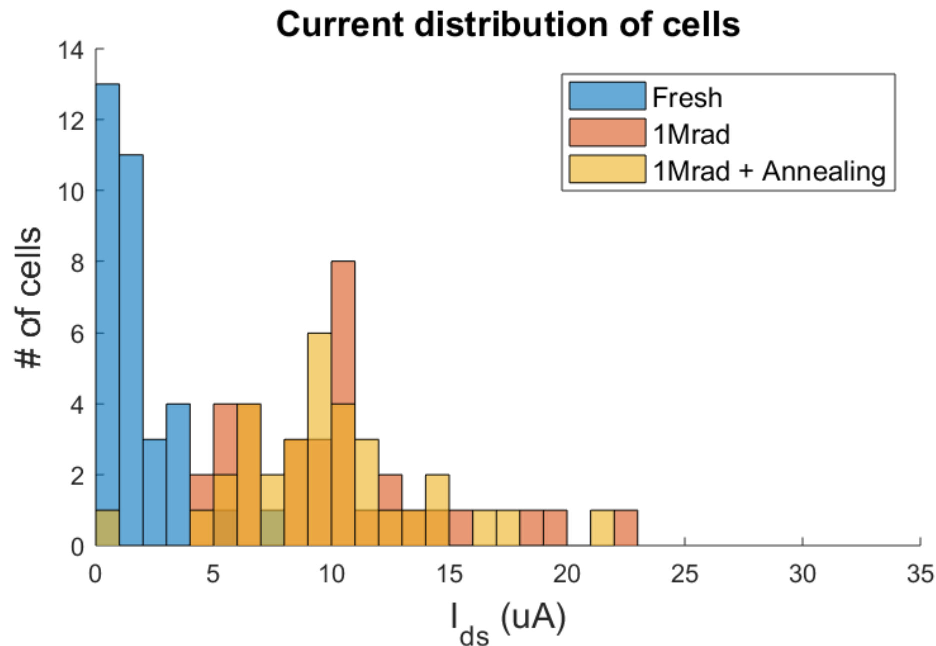


Confidential © ams AG

STREAM

ams

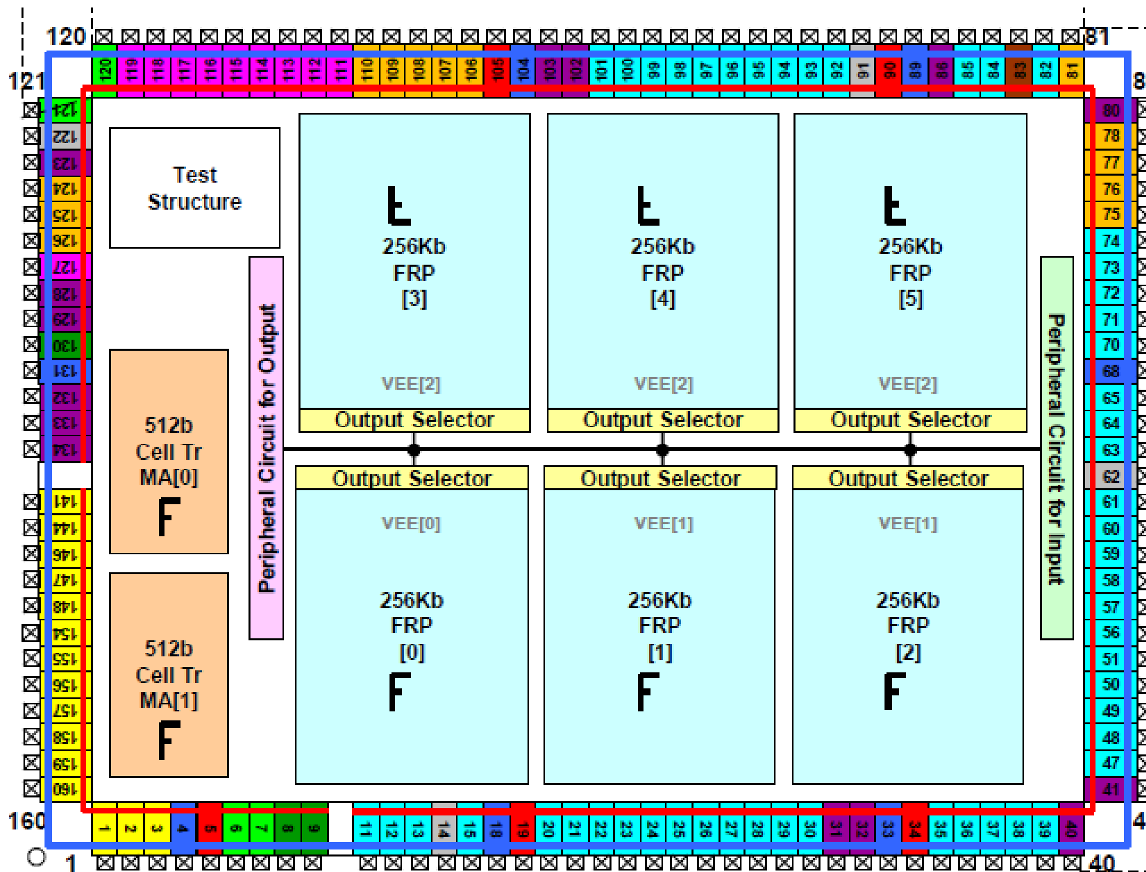
Early Results



- Variation of MUX paths within ±5%
- Array structure prevented single cell analysis
- Defects and testing mishandling caused a poor statistical sample pool.

Confidential © ams AG

Second Testchip



Result of the Secondment in Japan

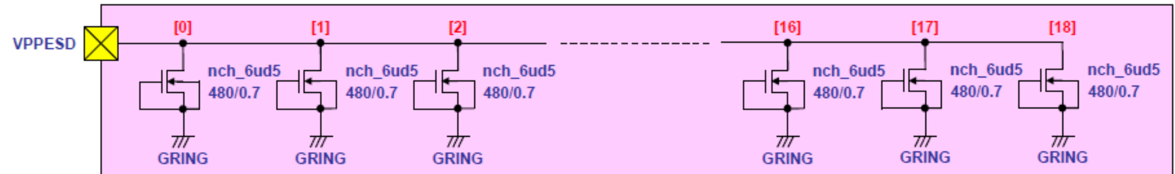
Collection of Macro with different types of device.

Bit Cell Matrices for distribution analyses

Single Structures for device charactrization

Second Testchip

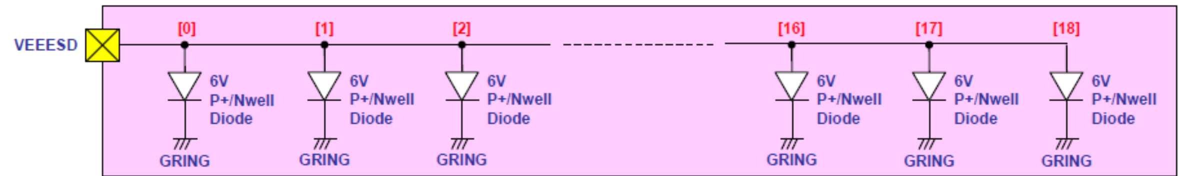
✓ For VPP



✓ DNW=VRING

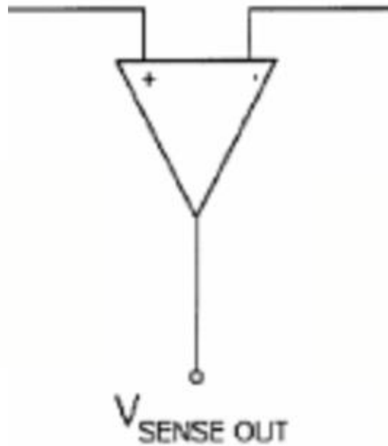
ESD Protection

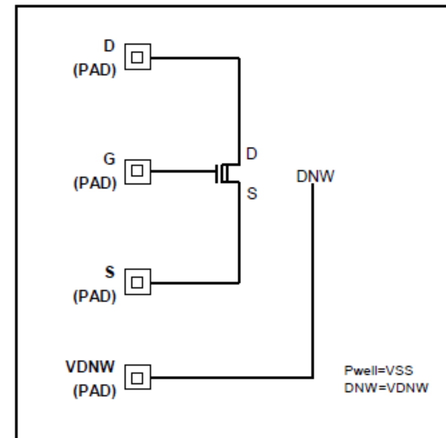
✓ For VEE



✓ DNW=GRING

Sense Amplifier





Bit Cell

STREAM

ams

Testing Sources

Test sources:

- **X-ray sources**
- **ɣ-ray sources**

TID based on trapped energy in matter:

=> Geometry related (secondary effects in X-ray surface absorption)

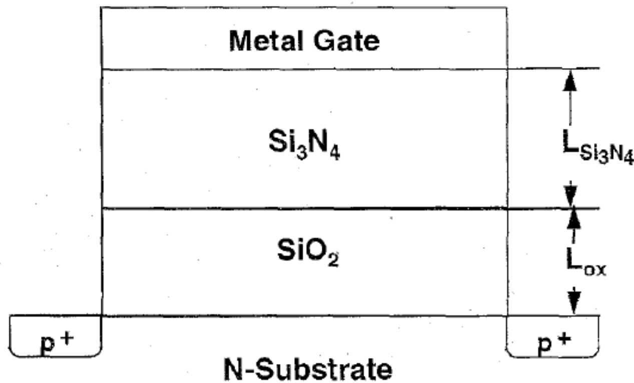
Testing Sources

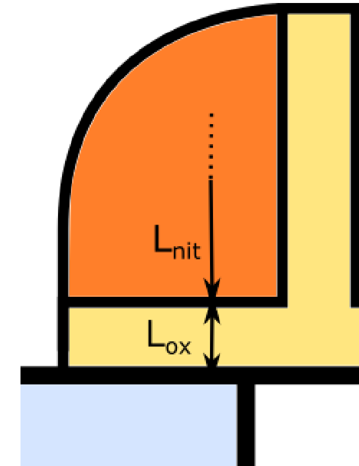
Collaboration between Federico Faccio at CERN and TUGraz:

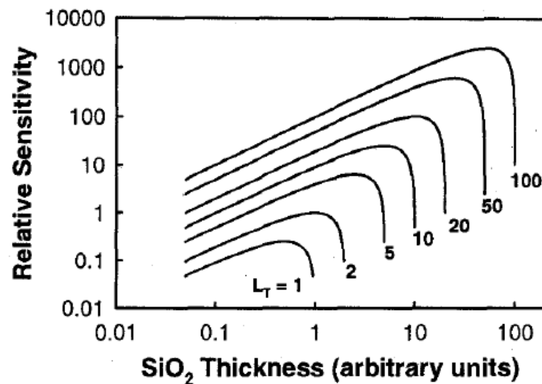
- Comparison of the method used at CERN (AXUVHS5 Opto Diode Corp) with the standard method using vacuum chamber.
- Investigation of the difference between X-ray and ɣ-ray use in testing circuits.

Confidential © ams AG

NVM Modeling







- Determination of the sensitivity of the device depending on material thickness
- Possible correction factors due to geometry improvements to the device compared to state of the art devices

J. R. Schwank, S. B. Roeske, D. E. Beutler, D. J. Moreno and M. R. Shaneyfelt, "A dose rate independent pMOS dosimeter for space applications," in *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, pp. 2671-2678, Dec. 1996.

Conclusions & Future Work

- SwSpc Memory Bit Cell remains a good candidate in terms of radiation tolerance
- More investigations are needed for poor results
- The new testchip provides all the necessary structures for a consistent measurement
- More investigation is necessary on testing techniques because of possible lack of consistency in TID definition
- A phisical model is needed to understand fully the potential of the BitCell

Confidential © ams AG

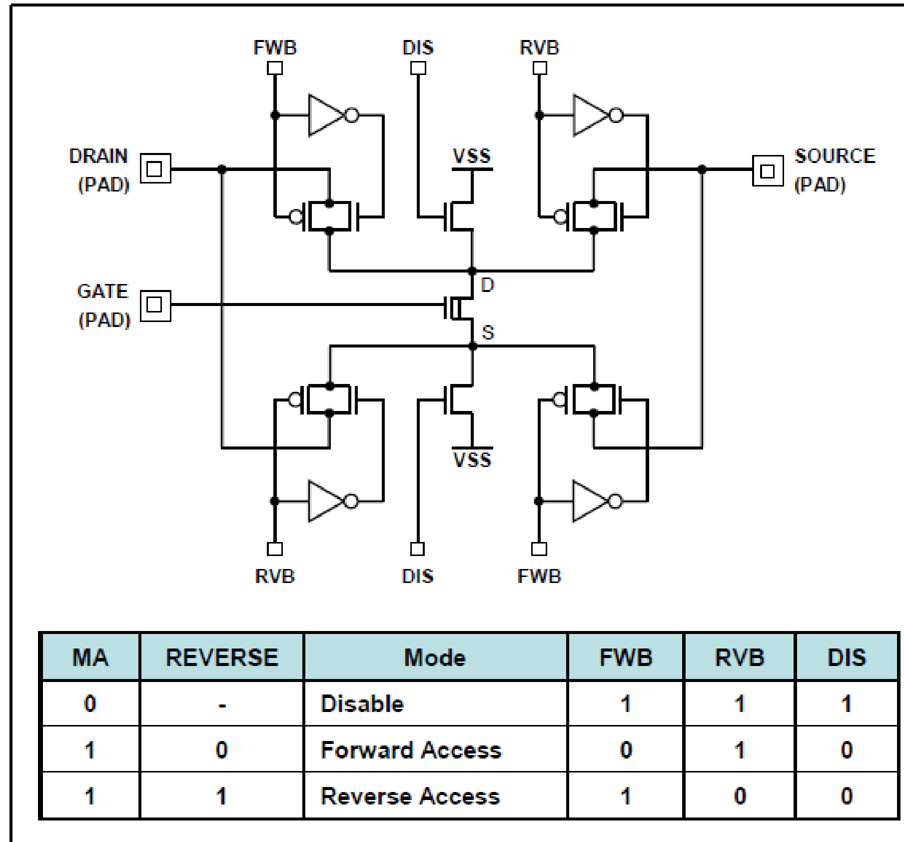
Thank you

Please visit our website www.ams.com

Confidential © ams AG

Structure of the Cell Transistor Matrix

✓ **Bit Cell**



MA	REVERSE	Mode	FWB	RVB	DIS
0	-	Disable	1	1	1
1	0	Forward Access	0	1	0
1	1	Reverse Access	1	0	0