Pixel Sensor Design Implementation and Test Results for the ATLAS ITK upgrade

TJ-Monopix (DMAPS) & CDR53B (clock/data recovery)

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Smart Sensor Technologies and Training for Radiation Enhanced Applications and Measurements (STREAM) is a project funded by the European Commission under the Horizon2020 Framework Program under the Grant Agreement no 675587. STREAM began in January 2016 and will run for 4 years.

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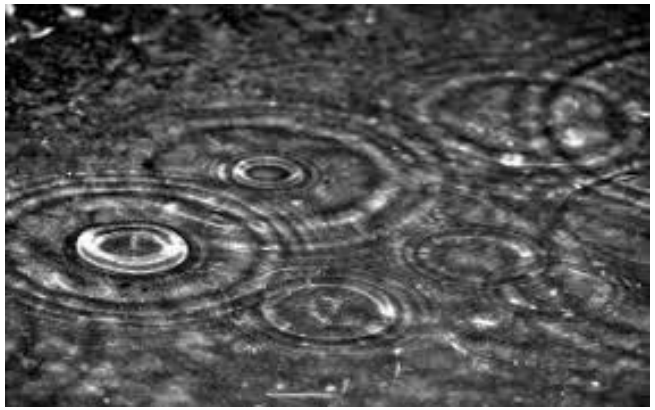
Pixel Sensors in the HL-LHC Era



LHC

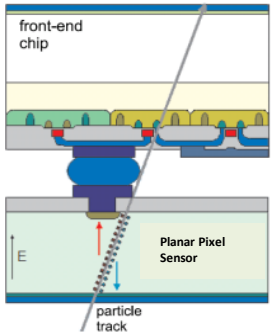
Vs

HL-LHC

	ATLAS-LHC	ATLAS-HL-LHC	
		Inner	Outer
Time resolution [ns]	25	25	
Particle Rate [kHz/mm^2]	1000	10 000	1000
Fluence [n_{eq}/cm^2]	2x10^{15}	2x10^{16}	1,5x10^{15}
Ion. Dose [Mrad]	80	> 1000	80
Pixel Sensor Type	*Hybrid*	*Hybrid*	*DMAPS or Hybrid*

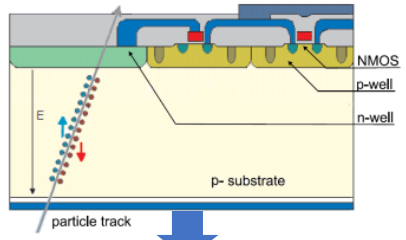
- High radiation level:
  - NIEL up to 10^{16} n_{eq}/cm^{2}s ➞ sensor
  - TID up to 1Grad ➞ electronics
  - SEU/SET ➞ memory, time critical blocks (CDR/PLL)
- High particle rate:
  - occupancy, bandwidth ➞ high density, high speed data link

I.



Baseline hybrid approach: Separate sensor and electronics optimization

II.



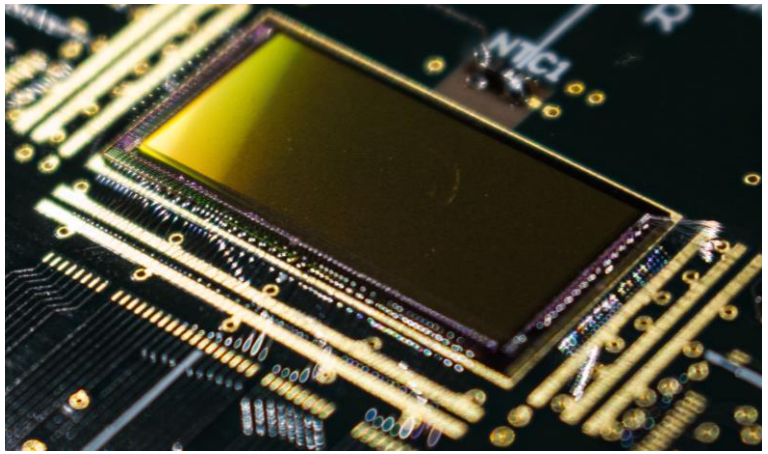
New advancements in imaging CMOS processes: HV/HR

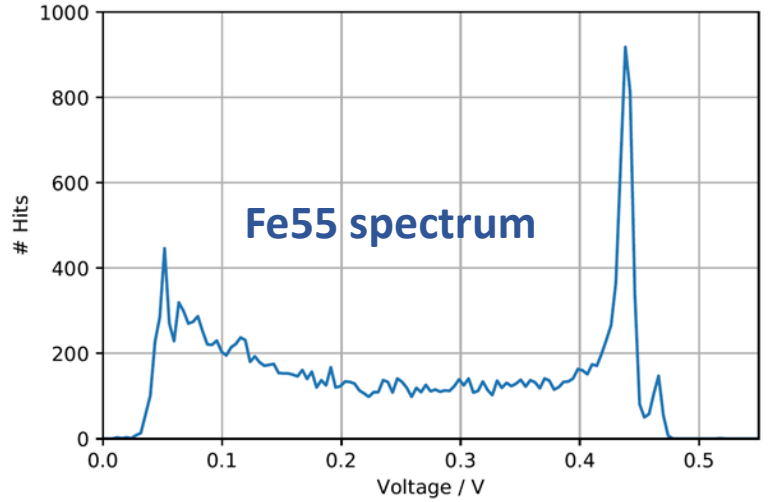
Enhanced charge collection & radiation tolerance

Outline - Achievements

I. TJ - Monopix

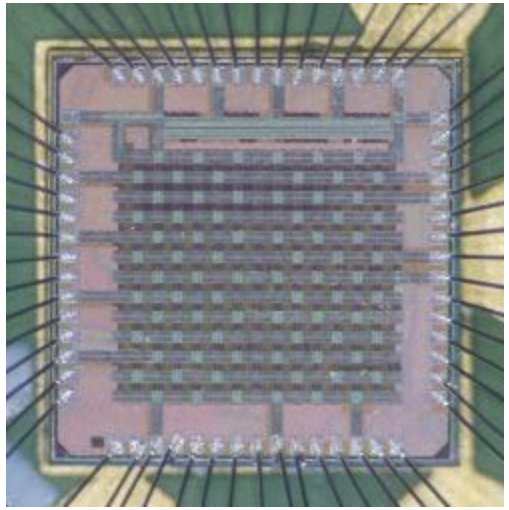
- **Large scale DMAPS** based on a novel 180nm process for the ATLAS ITk
- Standalone **column-drain** readout architecture

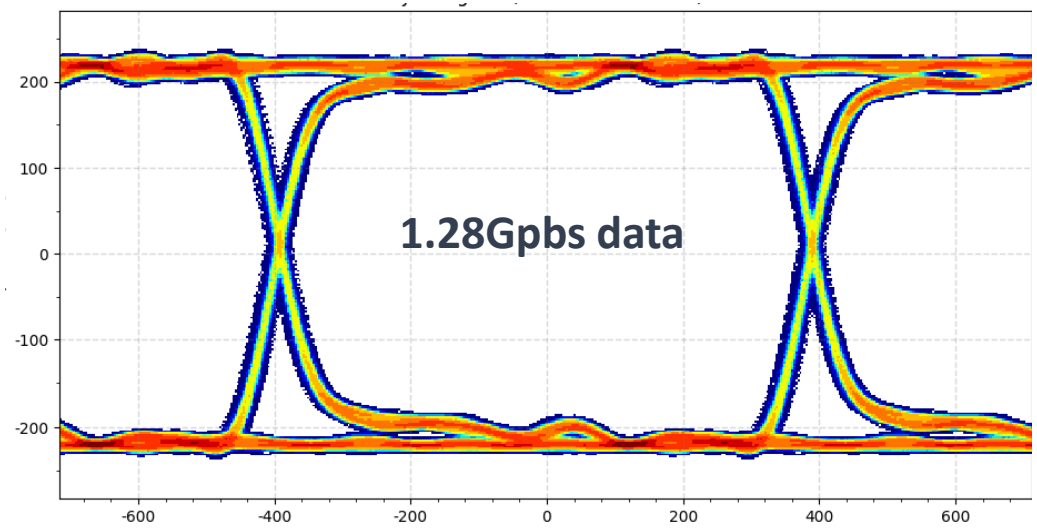




II. CDR53B

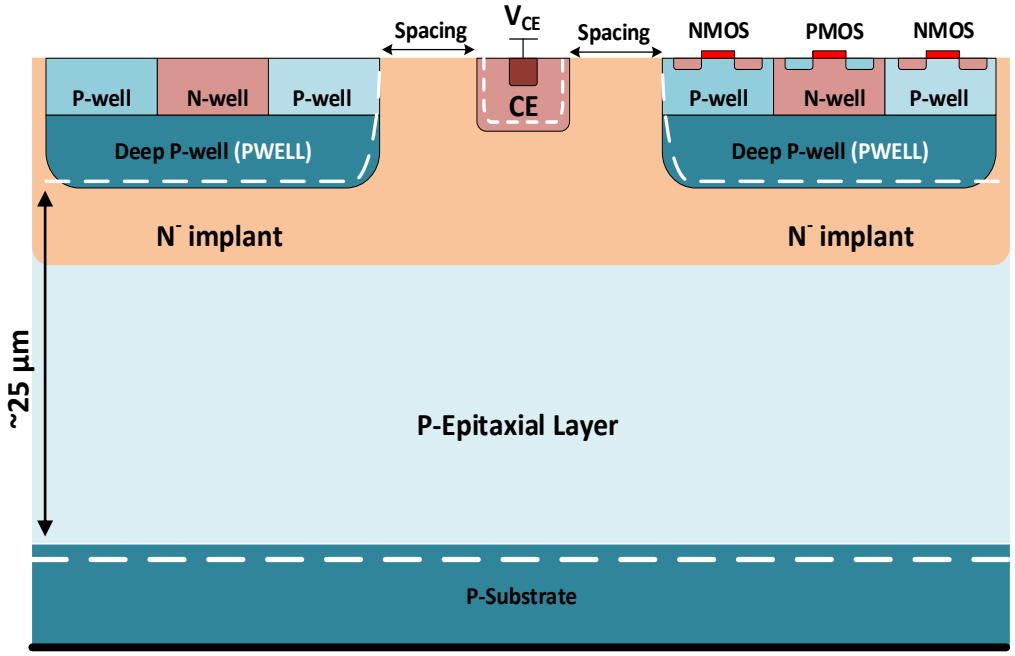
- **Clock & data recovery** for the RD53B FE (ITk baseline)
- Implemented test chip includes the **full data link chain** with serializer and GTX CML driver





TJ – Submission: Concept

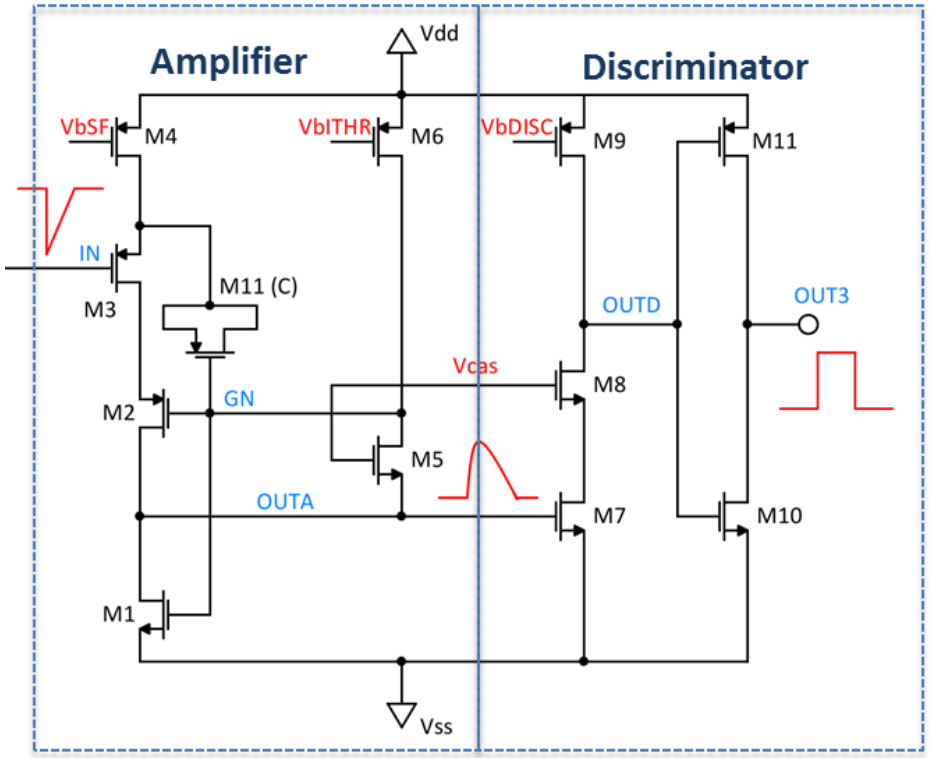
Small collection electrode, enhanced radiation tolerance



- Novel **modified** TJ-180 nm process ⟹ **full depletion**
- **Small** n-well collection electrode, $C \leq 3fF$
- Small pixel size (≈ 36x36 µm)

$$V_{in}\,(MPV) = \frac{e^{-}q_e}{C} \cong \frac{0{,}2fC}{3fF} \cong 65mV(ideal)$$

Low power, compact front end

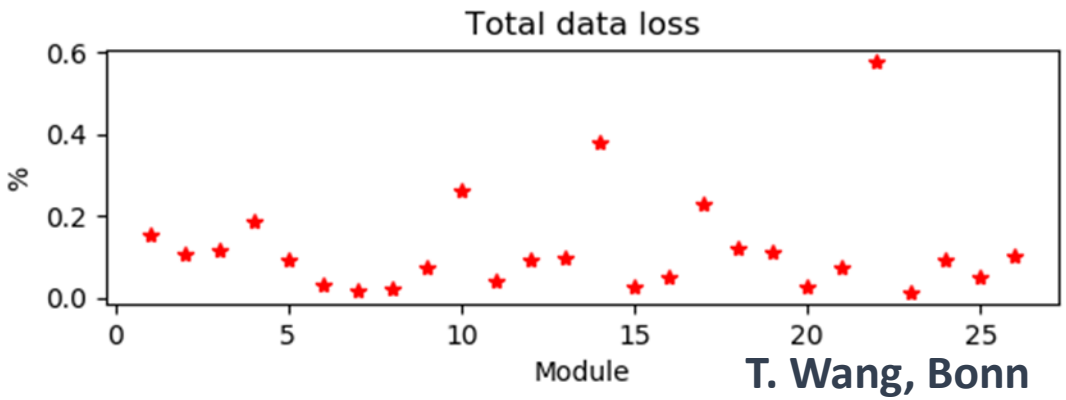


$$Gain = \frac{V_{OUTA}}{Q_{IN}} \cong 0.4\,{}^{mV}/_{e^-}$$

$$Power = 0.9\mu W$$

TJ – Monopix: Readout Architecture

- Why Column Drain Readout Architecture for CMOS DMAPS?
  - ✓ Fast readout with ToT capability
  - ✓ Has been used in the ATLAS b-layer (FE-I3)
  - ✓ Simple implementation
    - ✓ Less area – preferable for technologies with larger feature size
    - ✓ Reduced crosstalk
  - ✓ Not significant routing complexity
  - ✓ Simulated to be capable of handling the L4 expected hit rate



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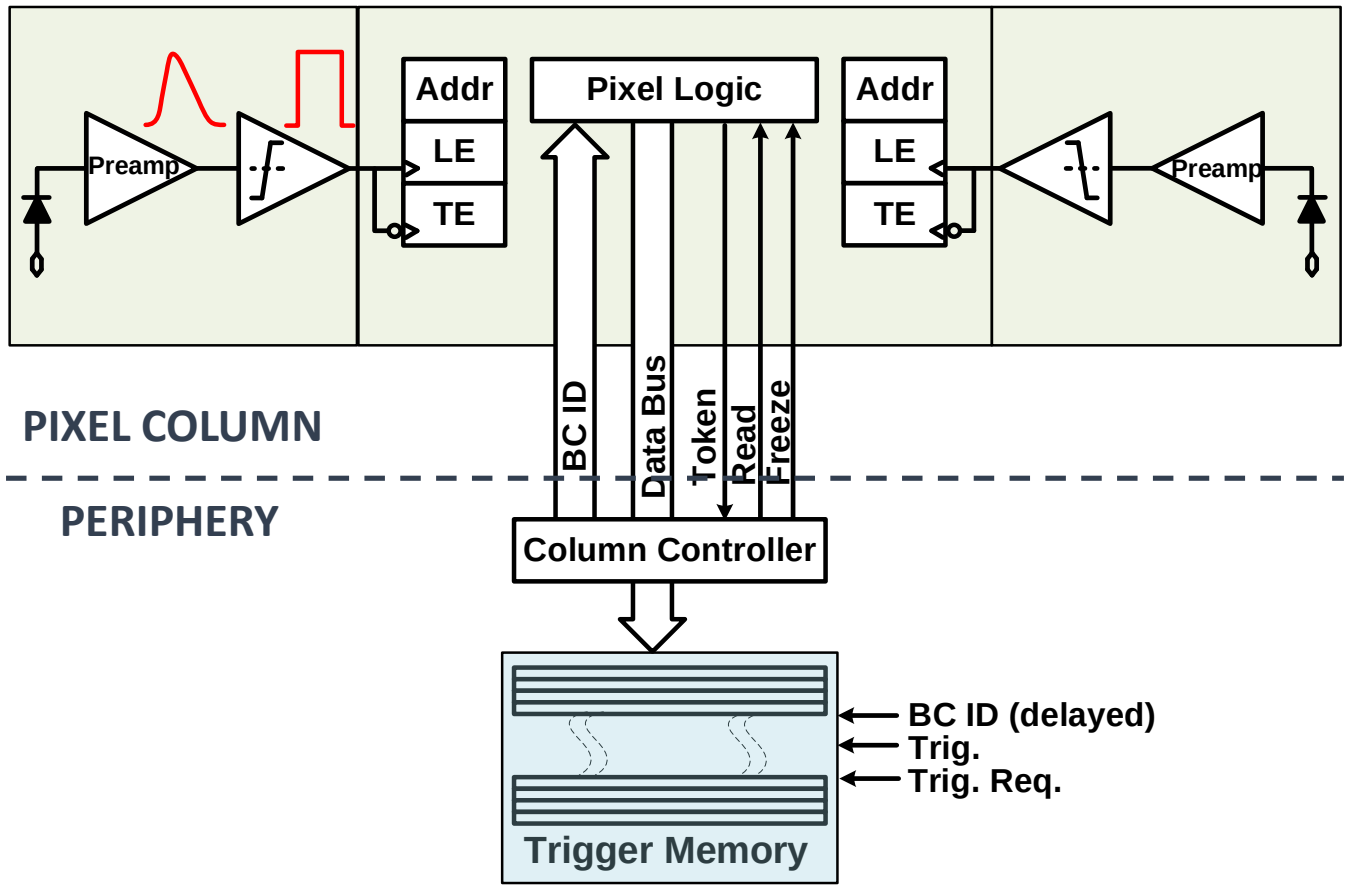
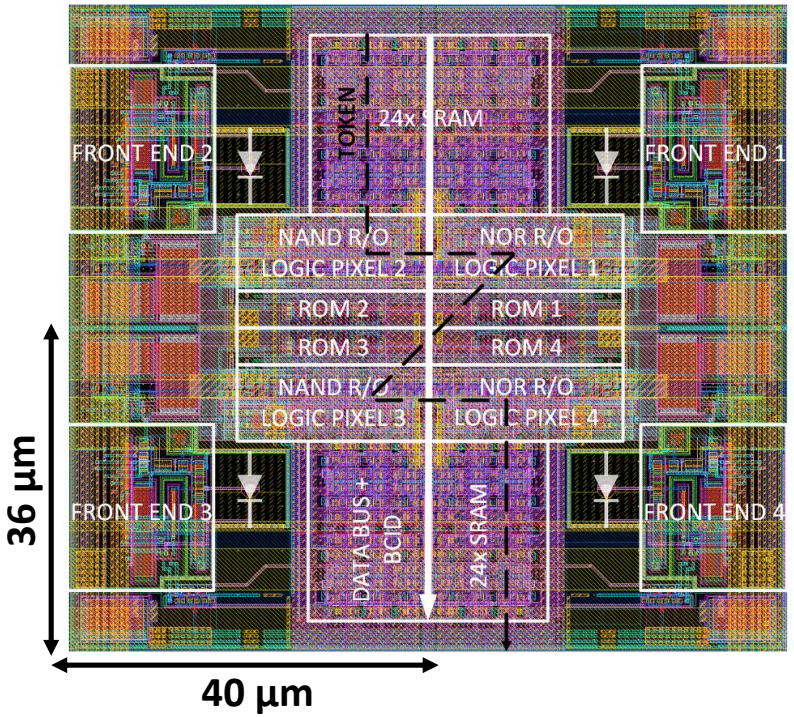
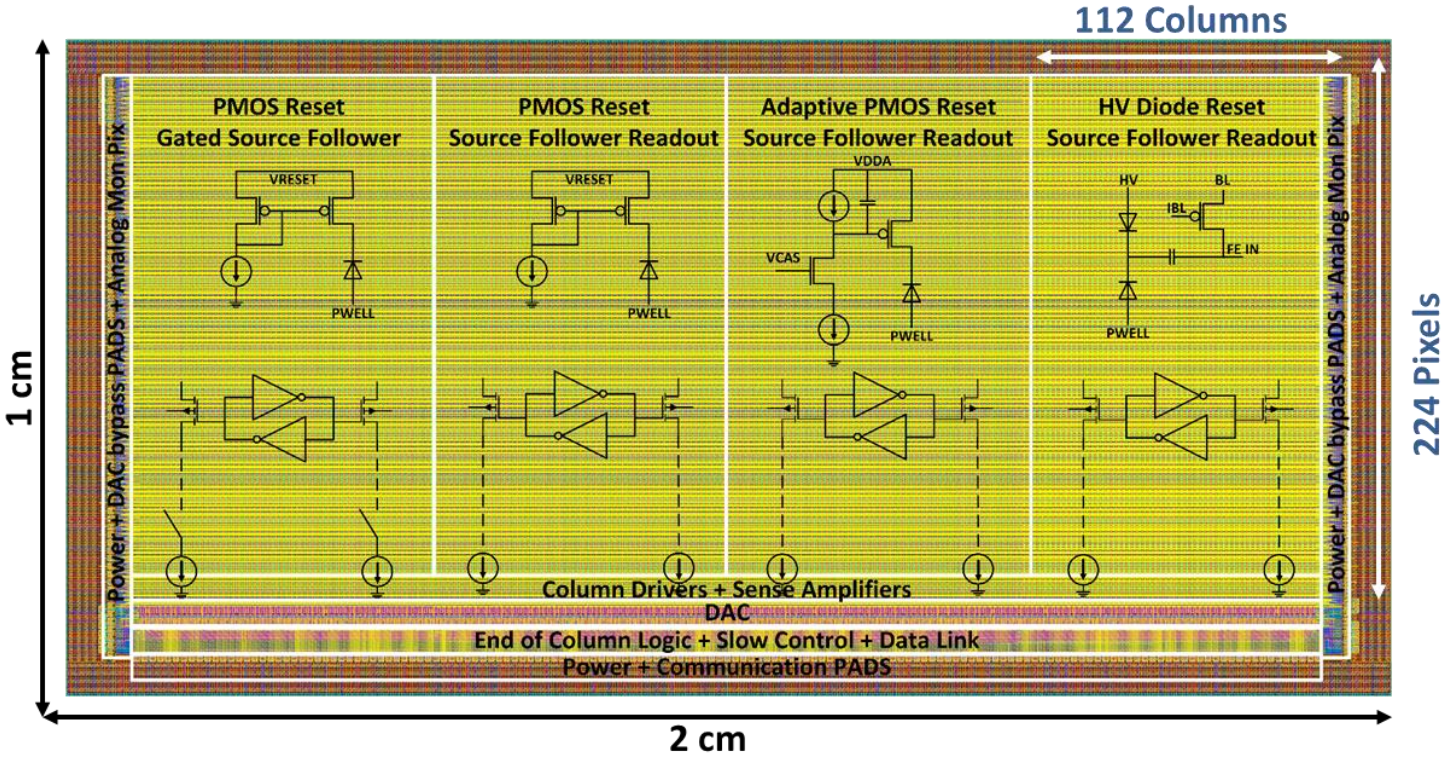


TJ – Monopix: Chip Design

2x2 Pixel Layout





- **Small pixel size:** 36x40 µm²
- **Low power:** $< 65\ mW/cm^2$
- No in-pixel tuning
- Design and layout strategies to minimize crosstalk

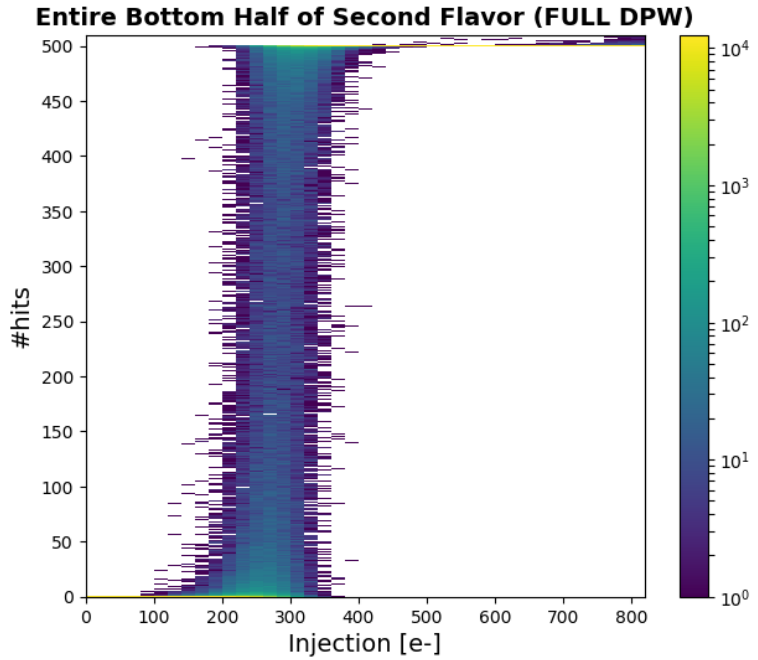
- **1x2cm² size, 224x448 pixel matrix**
- **4 Flavors, that include:**
  - Low-power column data-bus
  - Leakage compensation
  - AC-coupled pixels (front-side biasing)
- No trigger memory, 4x40Mhz data transmission

TJ – Monopix: Characterization

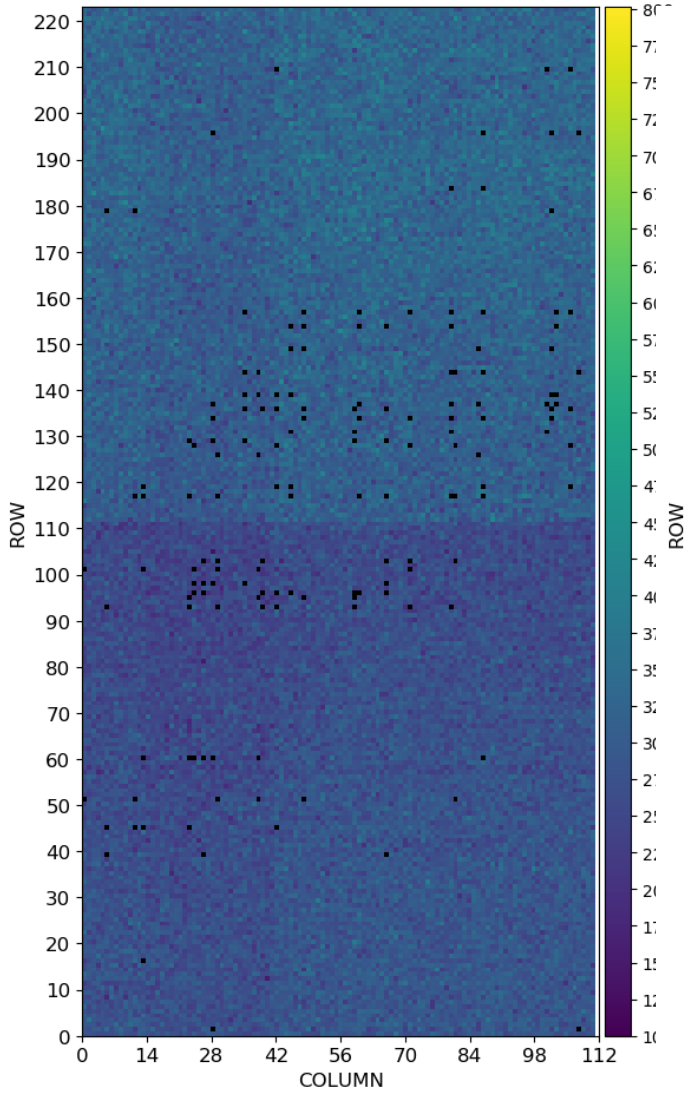
I) INJECTION SCAN

TJ-Monopix is fully operational

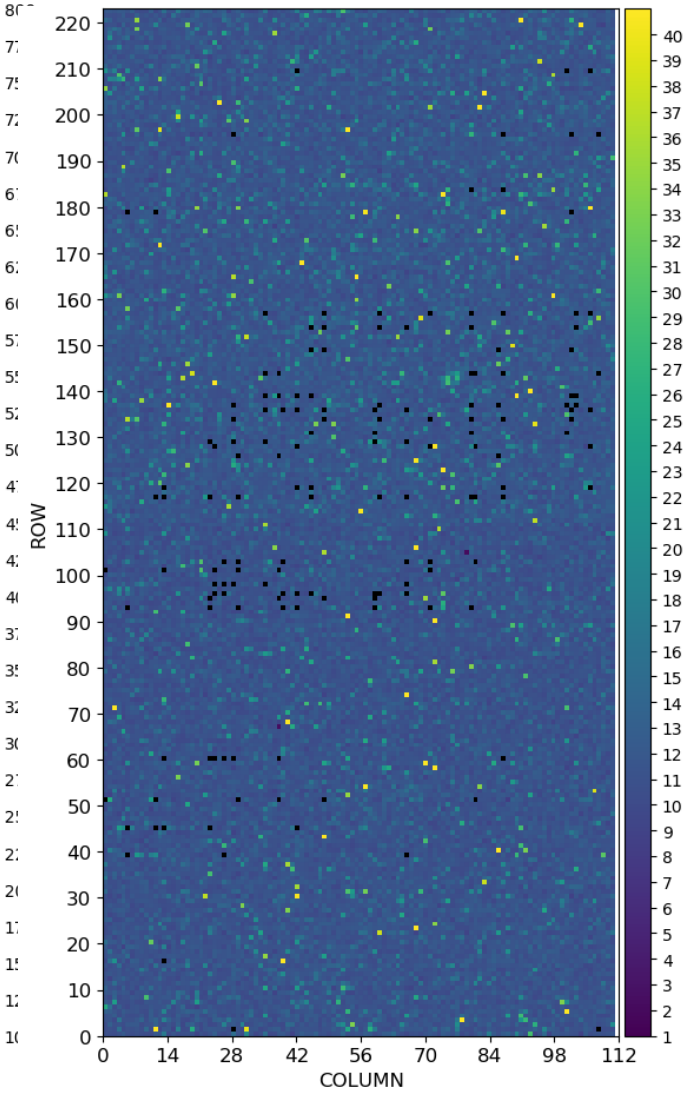
- Threshold $\leq 300e^-$, < 0.5% masked pixels, noise occupancy << 10^{-6} hits/BX
- Calibration performed with ^{55}FE



Threshold 2D map



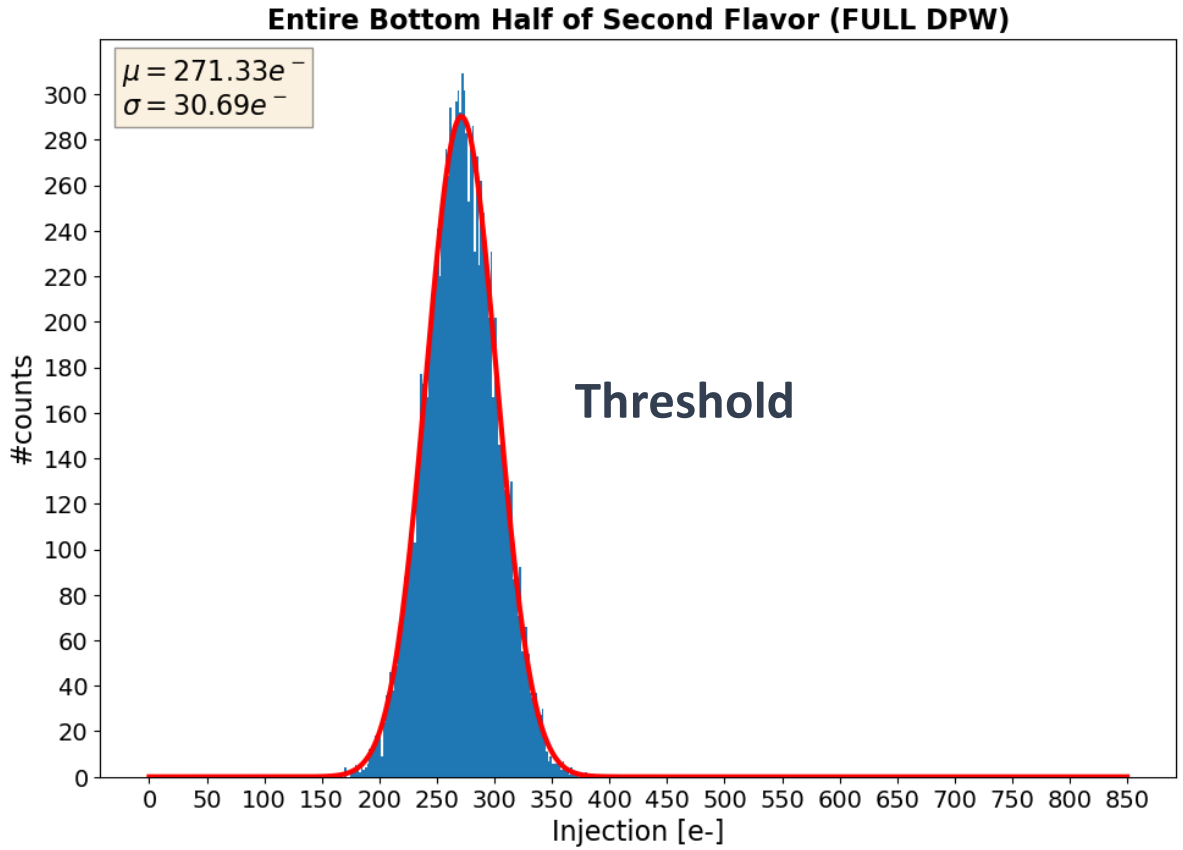
ENC 2D map

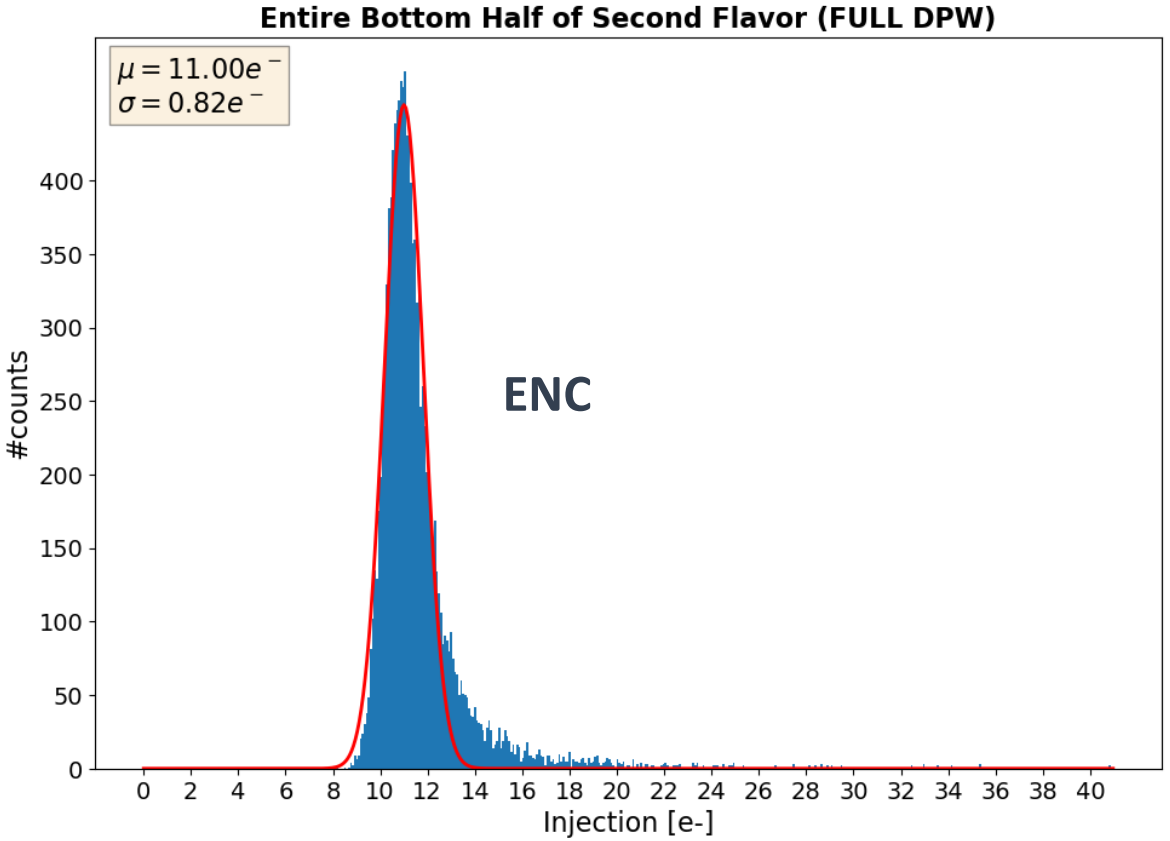


TJ – Monopix: Characterization

I) INJECTION SCAN

- Threshold mean ≅ 270e^-, total dispersion ≅ 31e^-
- Higher threshold and dispersion for the removed DPW region (lower input signal)
- ENC mean ≅ 11e^-, dispersion ≅ 0.8 e^-. (In agreement with simulation)



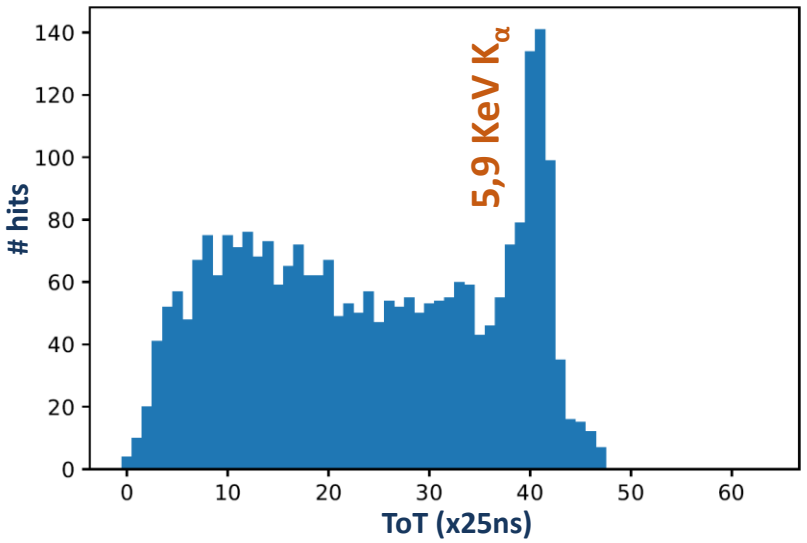


TJ – Monopix: Characterization

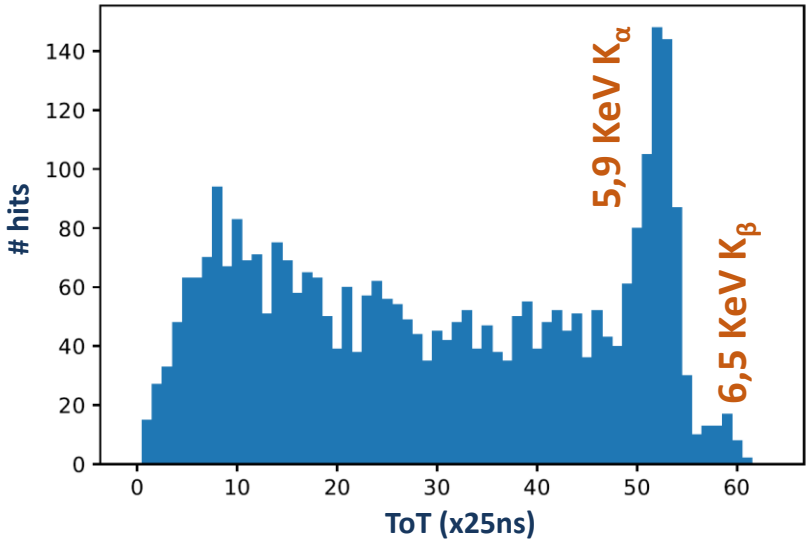
II) RADIOACTIVE SOURCE

- FE^{55} spectrum was measured using two different ways in different biasing conditions:
  1. Digital readout: 6-bit ToT, 64 bins, 25ns/bin
  2. Analog output of the front end using the oscilloscope ADC to capture the signal
- Only 10 mins of runtime for the digital capture. Even though the number of samples is not high the Mn K_α and K_β X-ray peaks are visible
- More samples during the analog capture. FWHM≅55e^- ⟹ σ≅23.5e^- ⟹ **ENC≅19e^-** (after subtraction of the Fano noise)

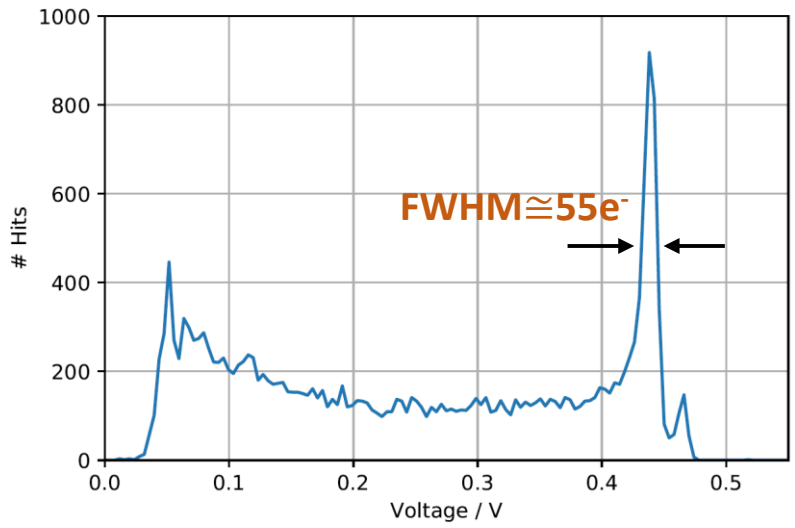
PWELL=-3V, PSUB=-3V, Digital readout



PWELL=-6V, PSUB=-6V, digital readout



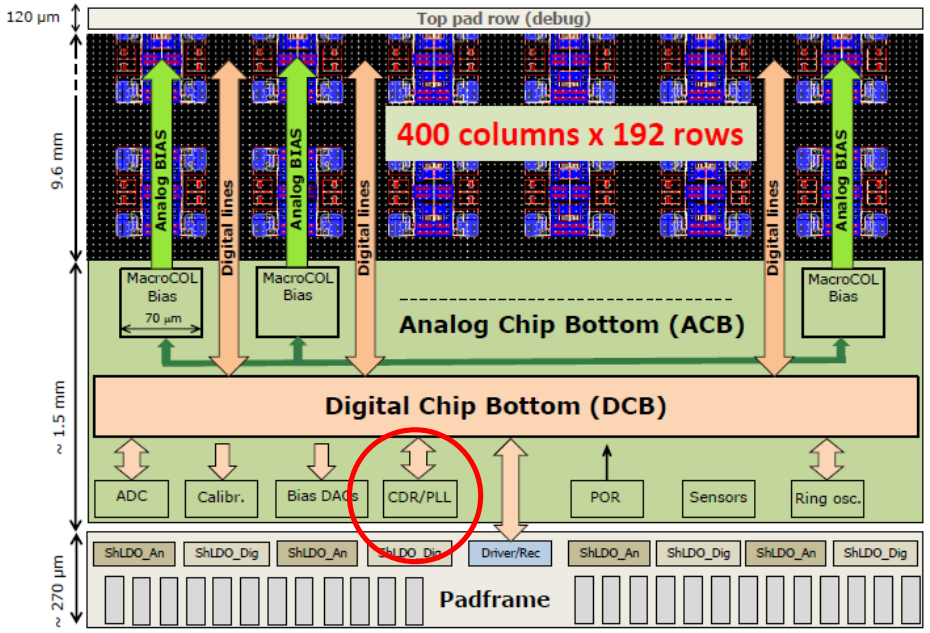
PWELL=-3V, PSUB=-3V, analog monitoring

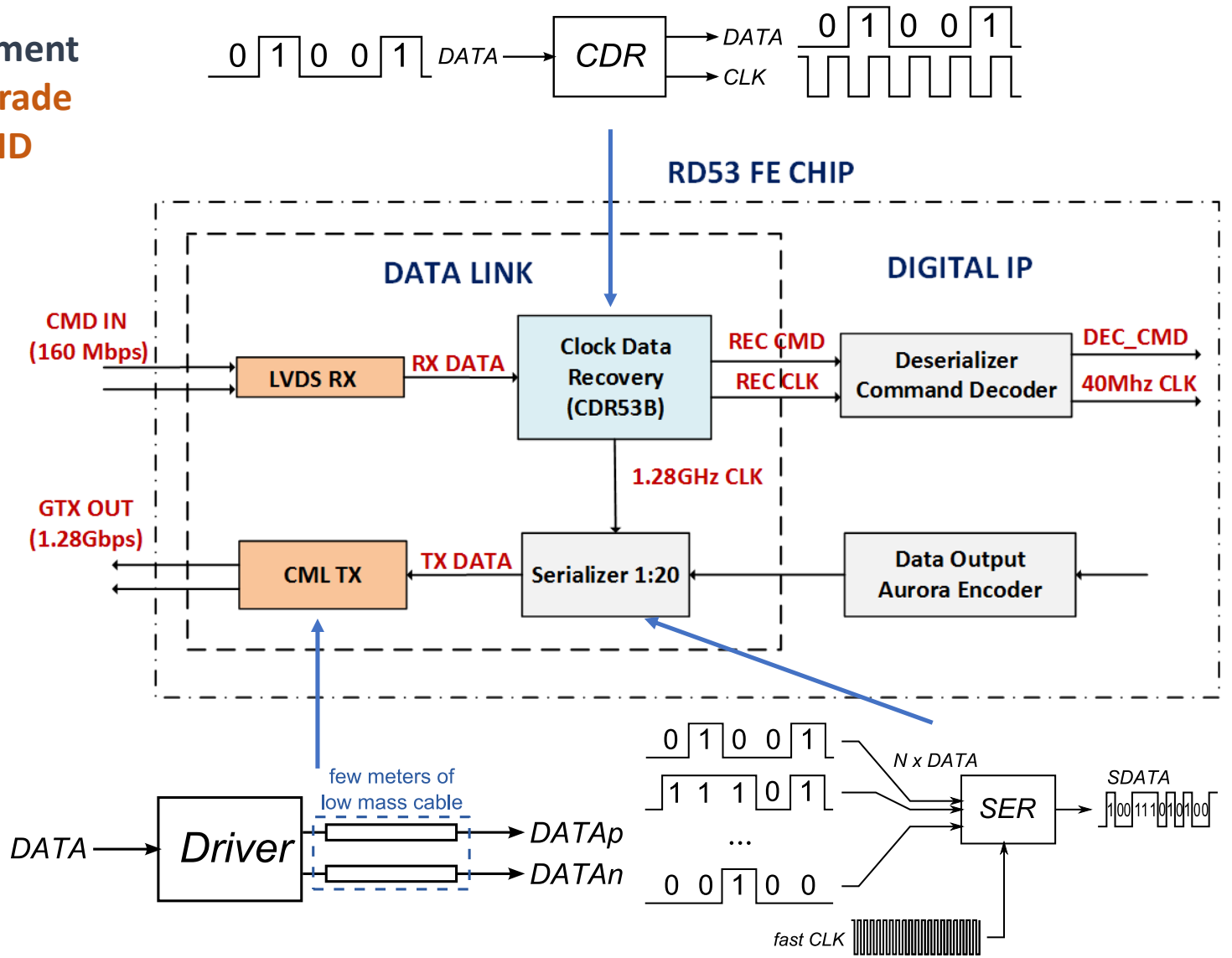


CDR53B: Introduction

- **RD53: ATLAS/CMS collaboration for the development of the large scale FE chips for the LHC phase 2 upgrade**
- **Must be able to operate at least up to 500 Mrad TID**
- **Technology of choice: TSMC 65nm**
  - **Logic density**
  - **High TID tolerance**

RD53A chip design





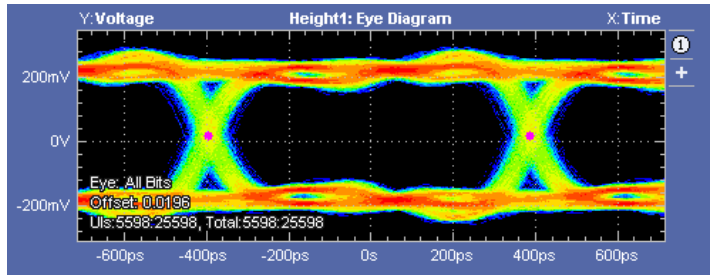
CDR53B: Introduction

- The CDR/PLL is a critical block that directly affects the whole chip operation and signal integrity
  I. Robustness: Locking and stability of the recovered clock must be guaranteed (drives every digital gate)
  II. Jitter: Major contributor of jitter in the data stream. High speed and low BER require a low jitter design
  III. SEU/SET: Errors due to SEU/SET must be minimized by design (triplication, large devices, high filter capacitance). The CDR should always be in the locking range and always recover
  IV. Furthermore, it must remain operational and within specification for every corner, wide range of temperatures (-40°C to 40°C) and for radiation damage up to at least 500 Mrad TID

- Jitter Specification
  1. Command input to RD53
     - Expected jitter at the output of LPGBT: $J_{RMS} = 5ps$
     - Will be increased by distortion and ISI from the low mass cable
  2. RD53 high speed data link (1.28 Gbps)
     - LPGBT automatic mode: $J_{RMS} < 10ps, J_{P-P} < 60ps$
     - LPGBT manual mode: $J_{RMS} < 40ps, J_{P-P} < 200ps$

RD53A CDR

CMD = PRBS5, J_{RMS} = 18ps, J_{P-P} = 134ps

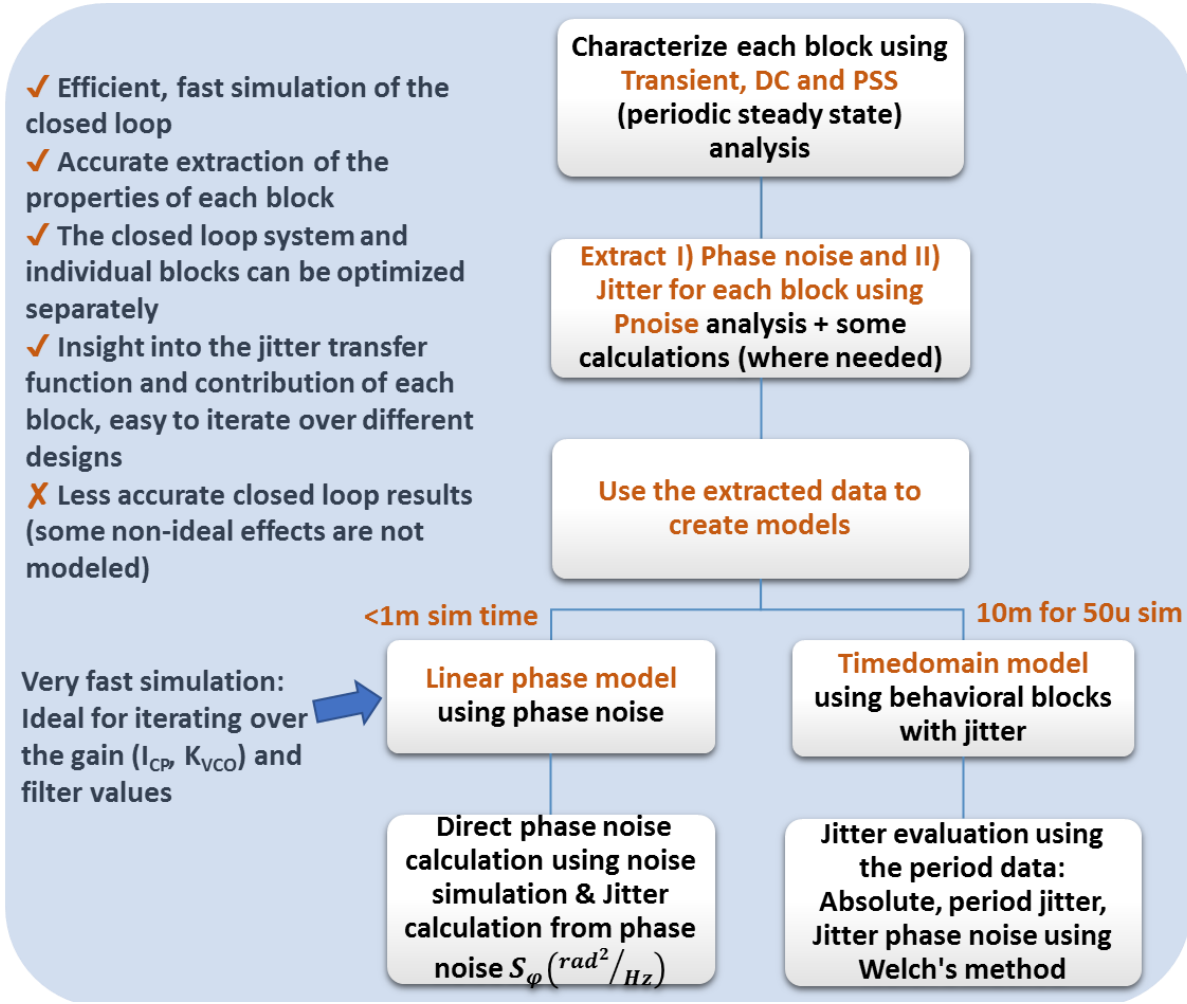


- The motivation behind CDR53B is the improvement of performance and reliability of the CDR and data link sub-system of RD53A: 1) Locking behavior and 2) Jitter of the output data stream

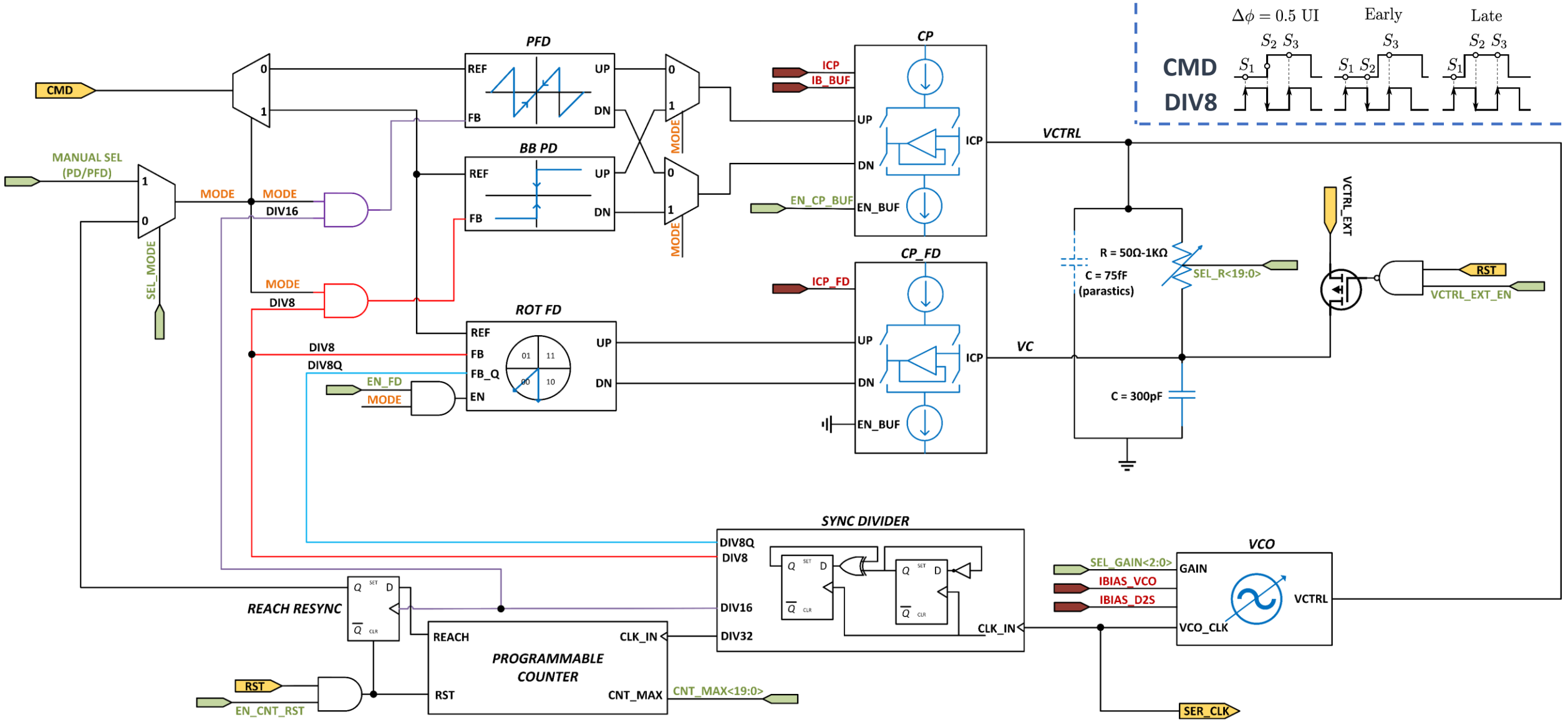
CDR53B: Design Strategy

1. Robustness, tolerance to radiation effects (TID, SEU)
   - All analog transistor dimensions larger than the recommended (2x minimum)
   - Radiation models for normal and RF transistors used in design and verification phase
   - TMR divider and configuration
   - Bang-bang, low BW loop ⟹ Detector SEU impact on the output frequency is reduced
   - Startup by PFD, Locking is guaranteed by a rotational frequency detector

2. Jitter
   - Optimization of the loop dynamics and jitter transfer function using behavioral models for fast simulation
   - Optimization of each block separately, model parameter extraction
   - Substitution of real blocks in the loop simulation for verification

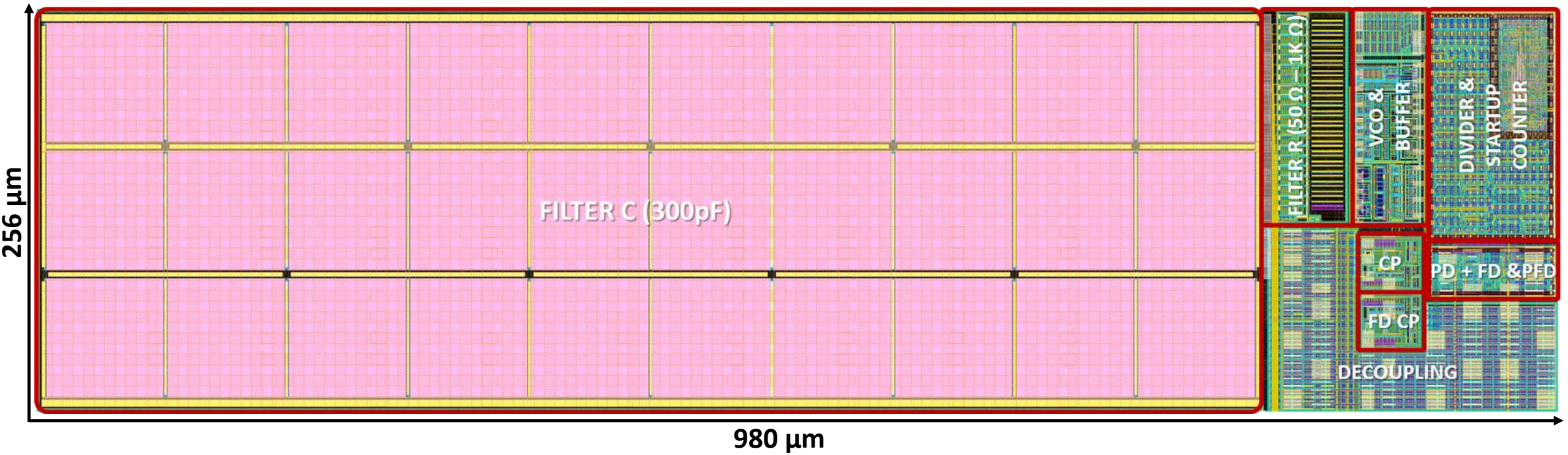


CDR53B: Block Diagram



CDR53B: Layout

- Area: 1mm X 0.25mm, designed with RD53B floorplan (2mm X 0.3mm) in mind
- Crtmom filter capacitor (300pF) improves jitter performance, but occupies large area (tradeoff)
- Careful layout to minimize resistance of the capacitor block interconnections (<0.5Ω), capacitance loading of high speed lines and coupling to sensitive nodes
- Filling the CDR block with decoupling, local decoupling in the vco buffer, divider and PD



CDR53B: Test chip

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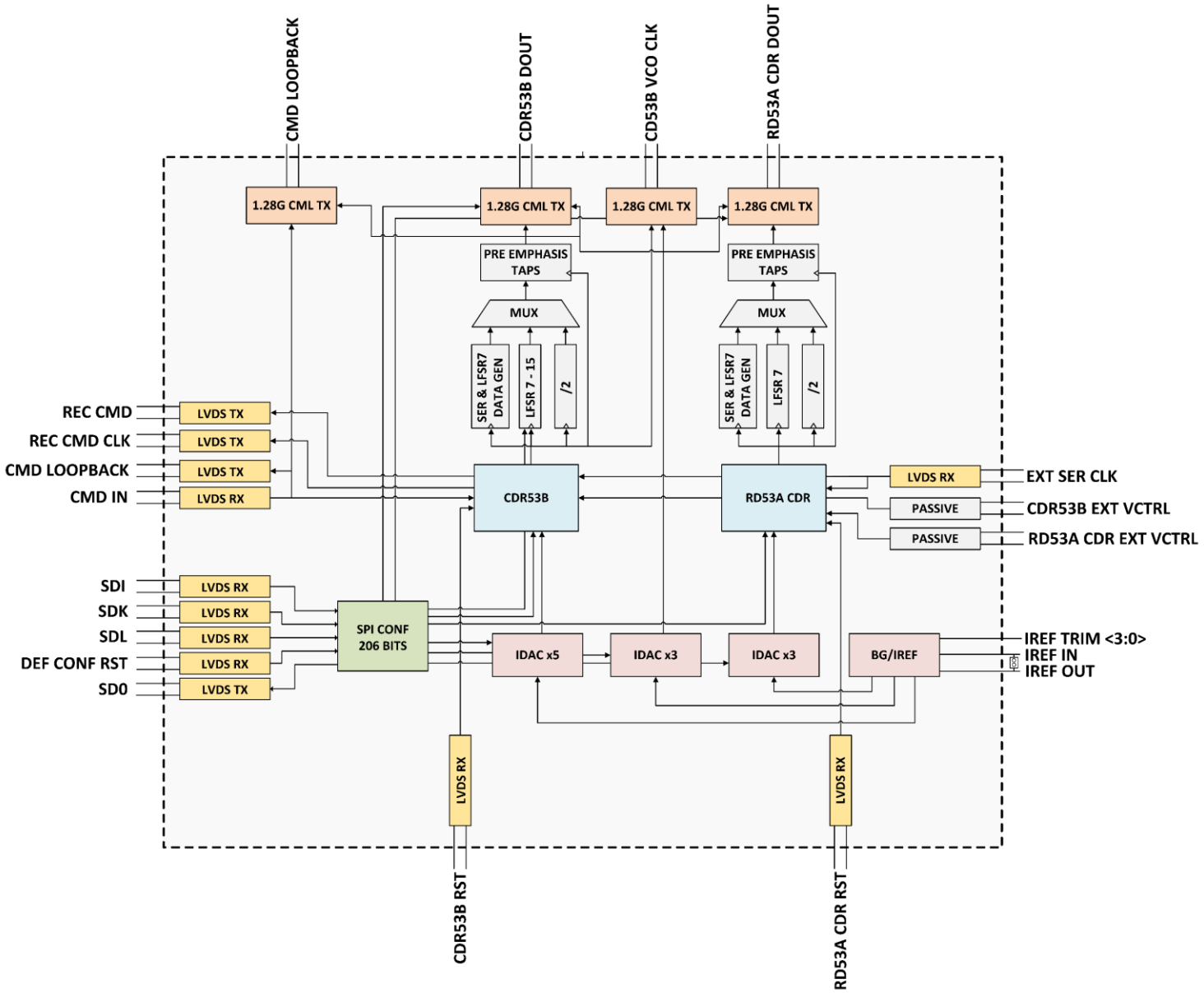
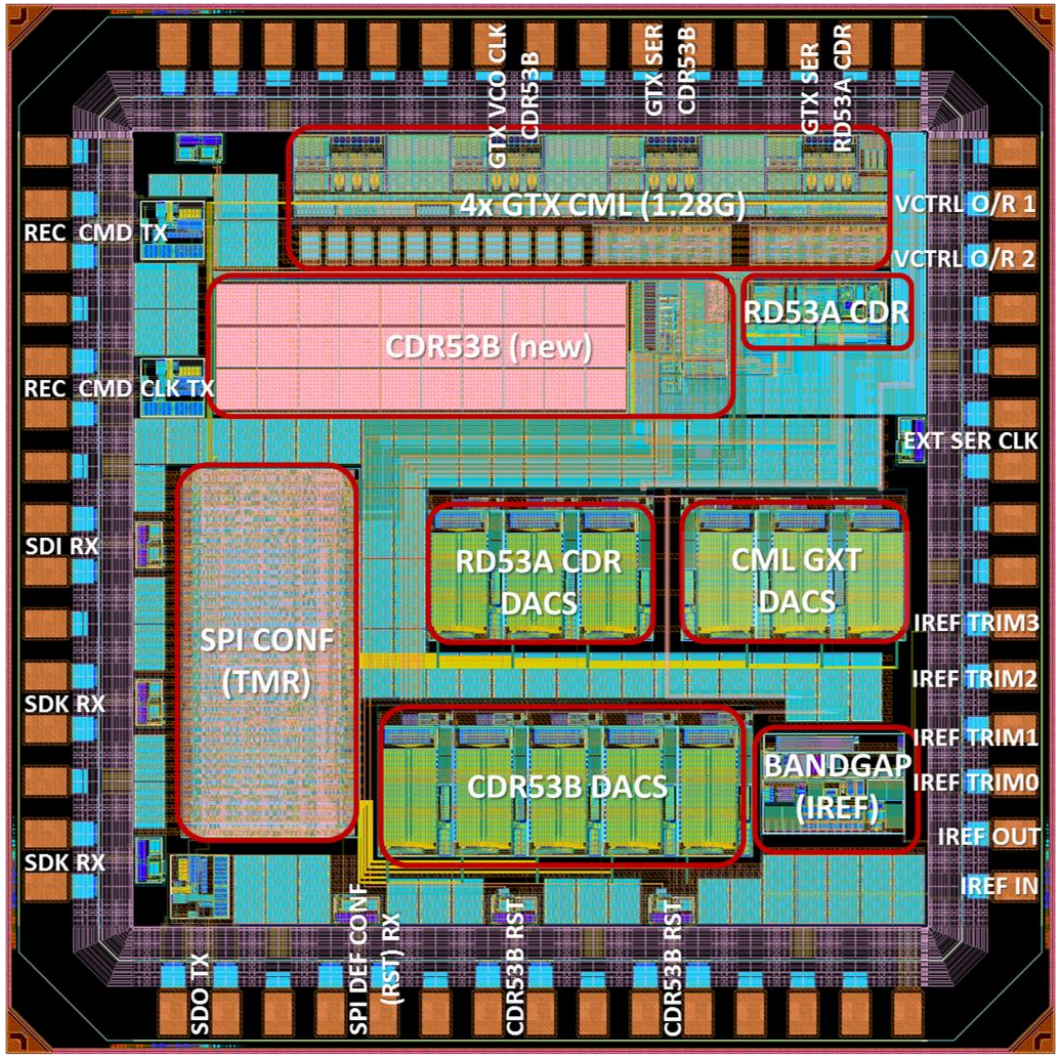
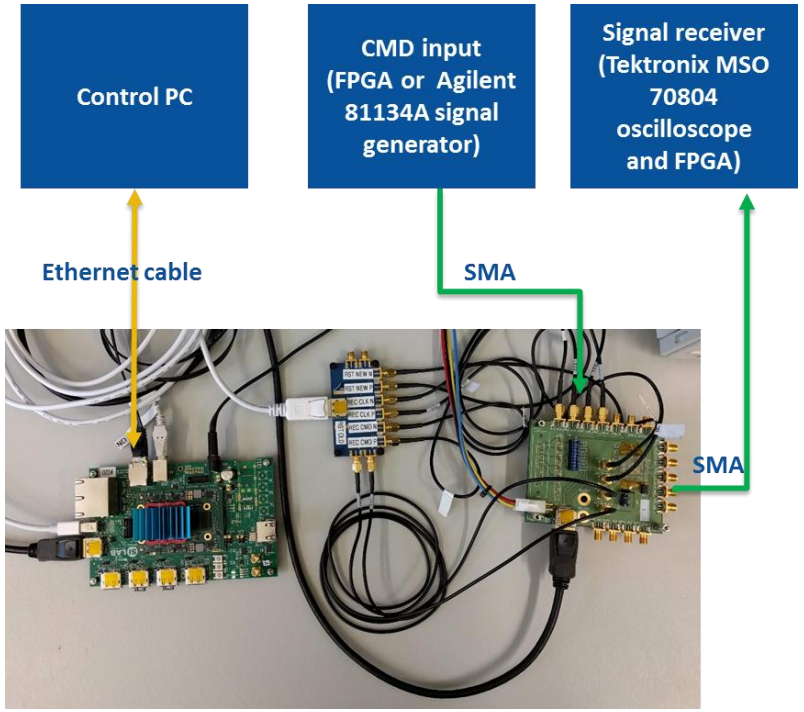
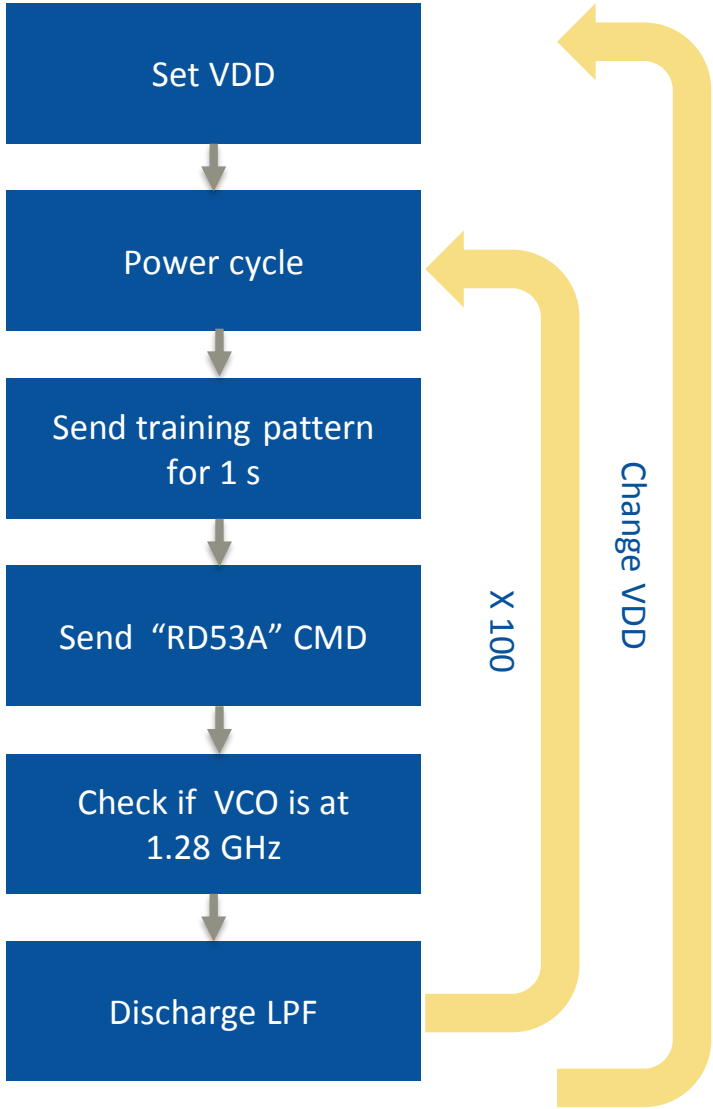




CDR53B: Characterization



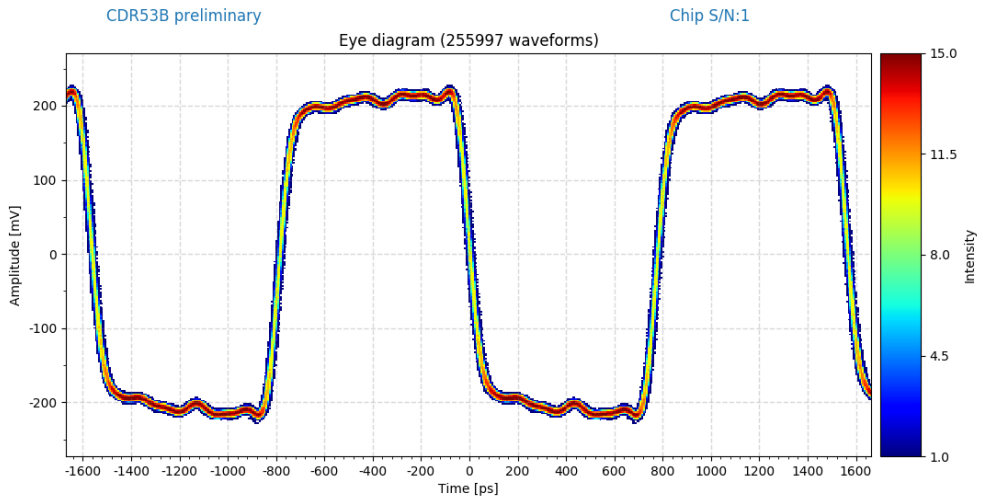


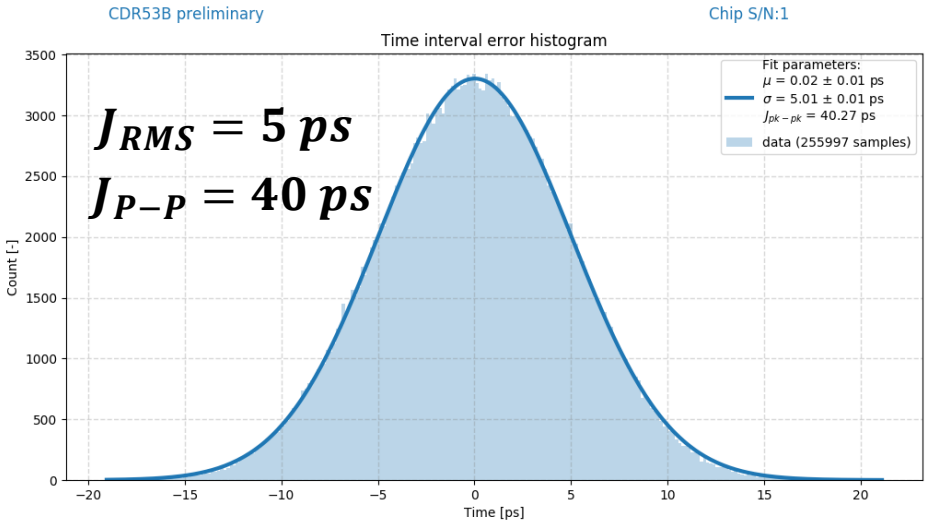
Lock success rate [%]										
Sample number	VDD [V]									
	0.8	0.85	0.9	0.95	1.0	1.05	1.1	1.15	1.2	1.25
1	0	0	100	100	100	100	100	100	100	100
2	0	0	98	100	100	100	100	100	100	100

CDR53B: Characterization

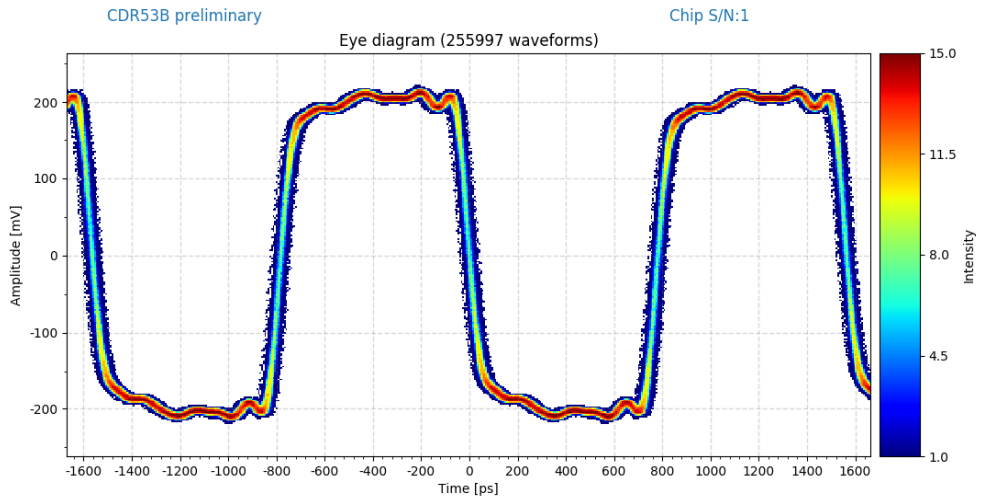
- **80 MHz clock input with 5 ps RMS jitter, 640 MHz clock output through the full chain (1.28GHz/2 in the serializer)**

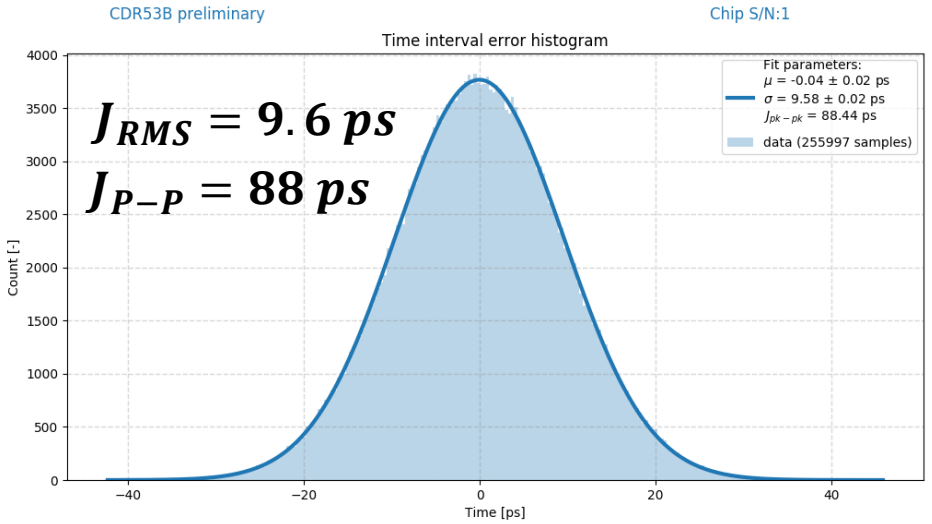
CDR53B





RD53A CDR (on CDR53B)

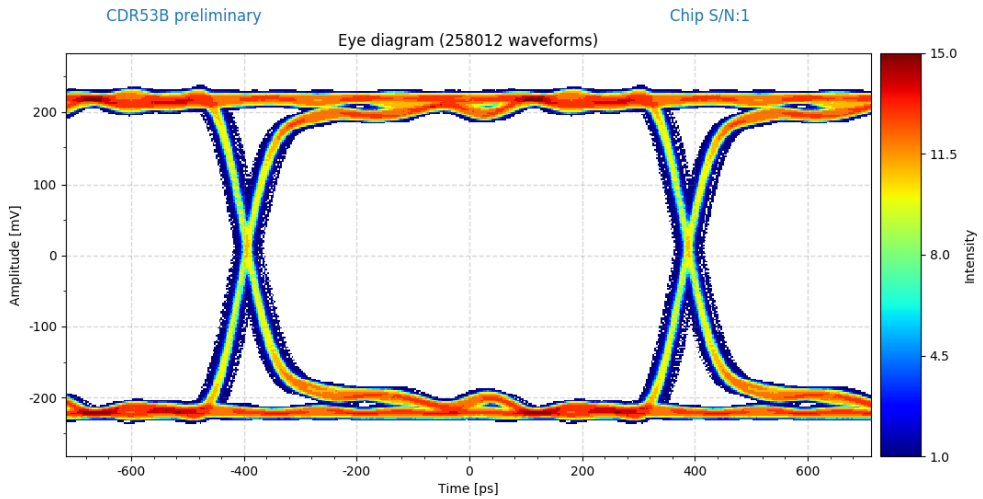


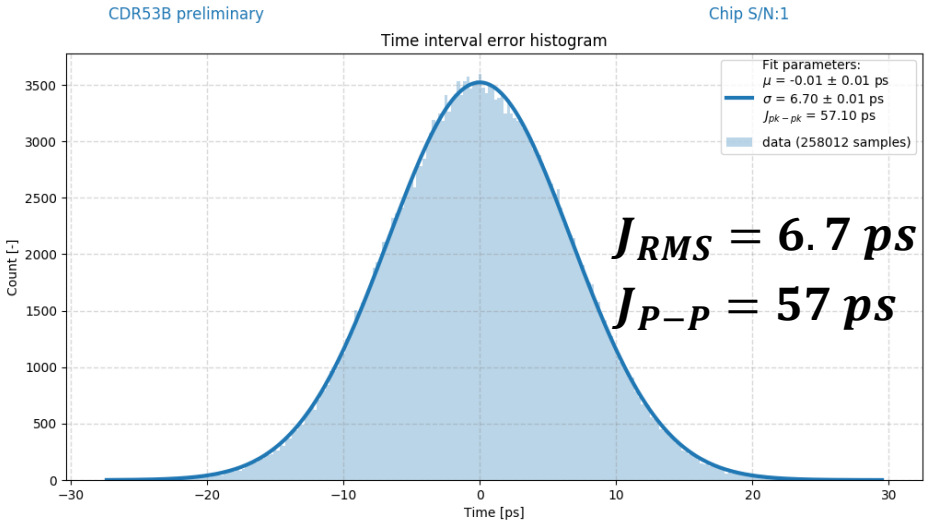


CDR53B: Characterization

- **PRBS 5 input with 5 ps RMS jitter, PRBS 15 data output (generated by an LFSR inside the serializer)**

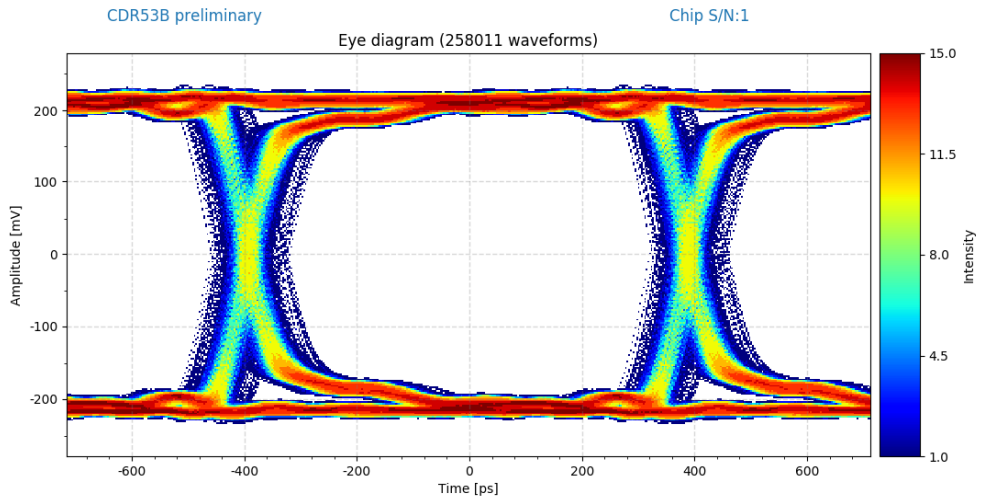
CDR53B

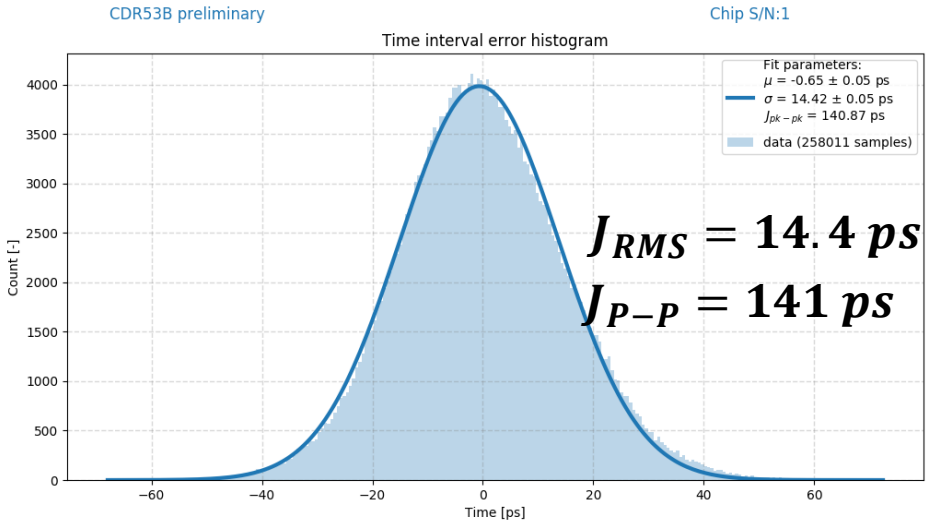




$$J_{RMS} = 6.7\ ps$$
$$J_{P-P} = 57\ ps$$

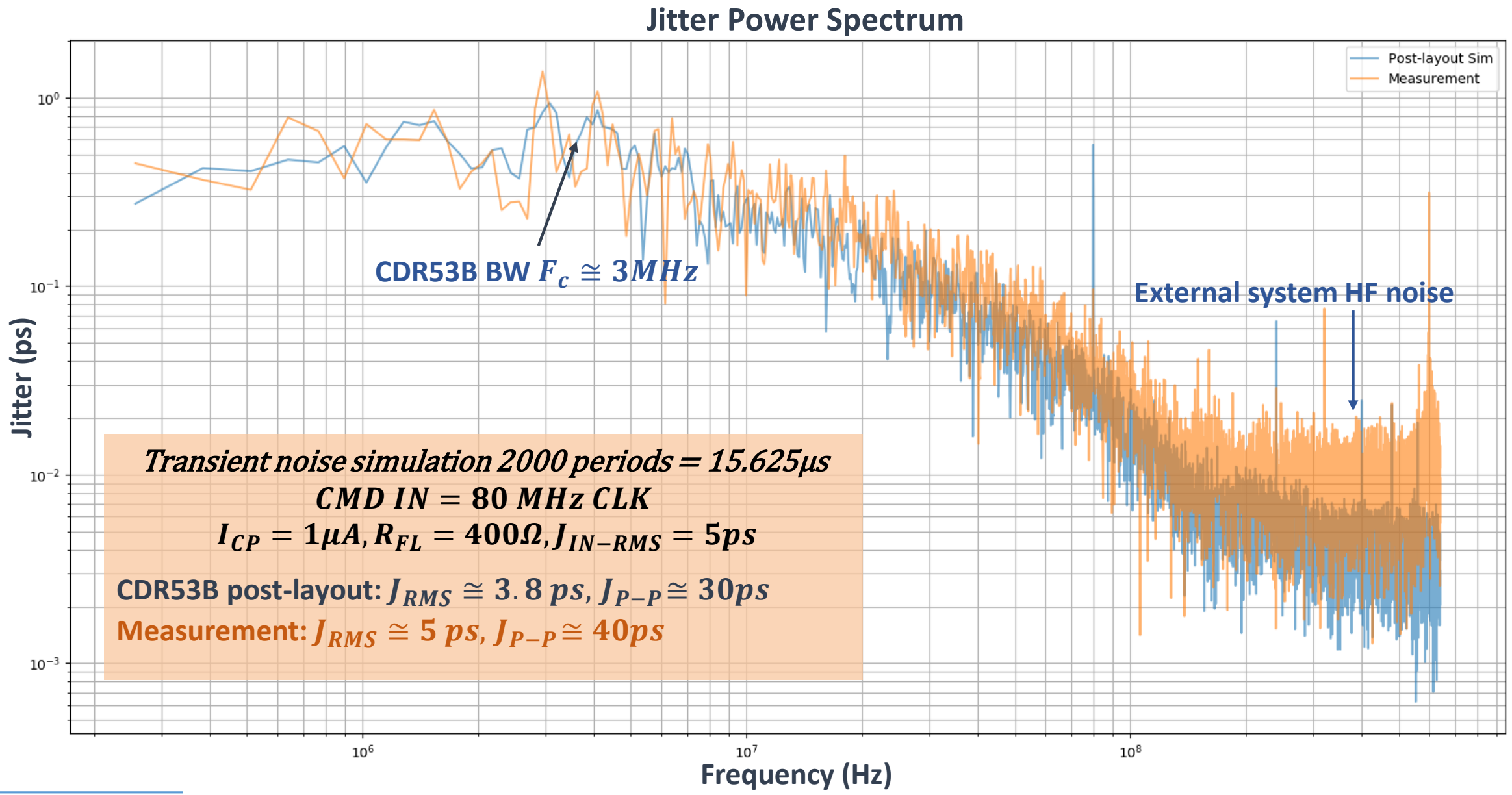
RD53A CDR (on CDR53B)





$$J_{RMS} = 14.4\ ps$$
$$J_{P-P} = 141\ ps$$

CDR53B: Characterization



Conclusion - Outlook

Summary

- A large scale DMAPS demonstrator chip and a CDR/PLL test chip for the HL-LHC phase2 upgrade have been successfully designed and characterized
- Both prototypes are fully operational and within the designed electrical specifications
- The implementations were done with radiation tolerance as a critical constraint, employing special design techniques

Current Research

- A successor to TJ-Monopix called TJ-Monopix2 is currently being designed to improve performance and to fully comply with the ATLAS specifications
  - Full scale matrix: 2x2cm^2
  - Process modification improvements to increase charge collection efficiency
  - Improved front end (increased gain, less threshold dispersion)
  - Threshold tuning

- CDR53B characterization is ongoing:
  - Performance measurement under low temperature conditions,
  - X-ray irradiation to investigate TID effects
  - SEU rate measurement
- Integration to RD53B

Dissemination/Outreach

January 2018 – December 2018

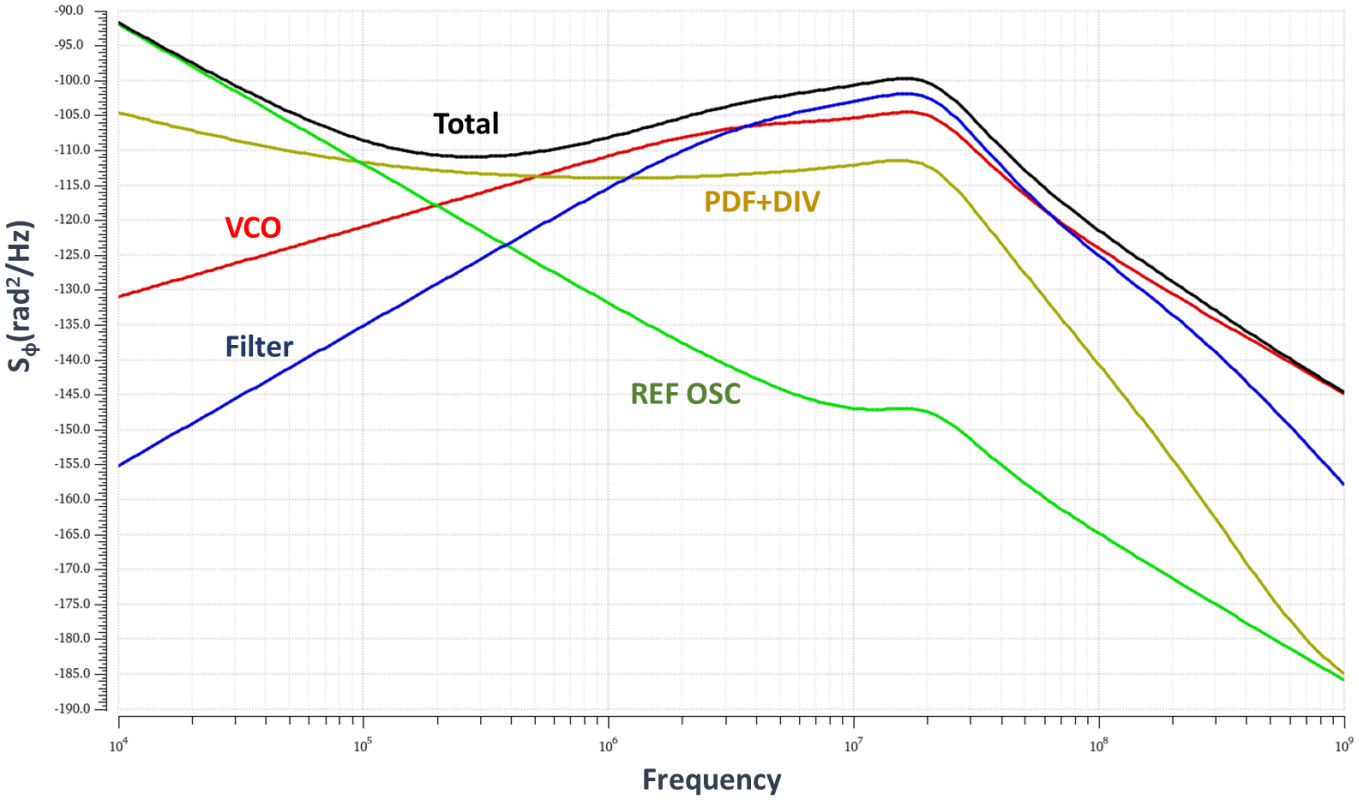
- **Oral presentation at the 81st Annual Meeting of the German Physical Society (DPG), 28.03.2017, Münster, (DE) with title: *"Monolithic pixel sensor development in a novel 180nm CMOS process for the ATLAS inner tracker upgrade"***
- **Oral presentation at the ATLAS Upgrade Week (AUW), 17.04.2018, CERN, Gevena, Switzerland with title: *"TJ Monopix, a Low-Power High-Granularity Monolithic Pixel Sensor for the ATLAS ITK upgrade: First Measurement Results"***
- **Oral presentation at the 14th Pisa Meeting on Advanced Detectors, 27.05.2018 - 02.06.2018, La Biodola, Isola d'Elba, Italy with title: *"CMOS Monolithic Pixel Sensors based on the Column-Drain Architecture for the HL-LHC Upgrade"***

- **Authored and published article at the Nuclear Instruments and Methods in Physics Research (NIM) journal with title: *"CMOS monolithic pixel sensors based on the column-drain architecture for the HL-LHC upgrade"*** https://doi.org/10.1016/j.nima.2018.09.100
- ***Co-author in several additional scientific articles***

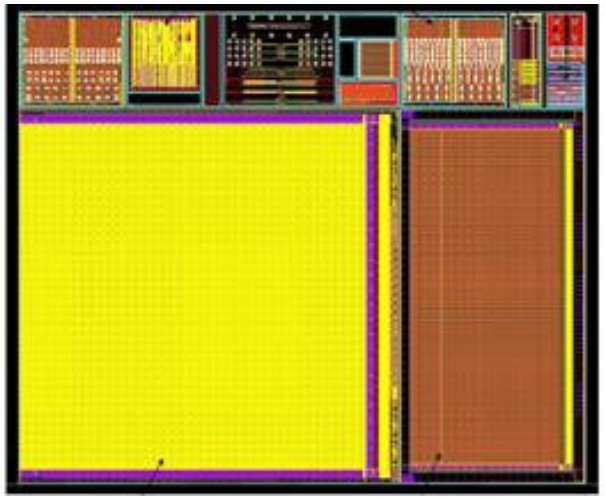
BACKUP

CDR53B: Design Strategy

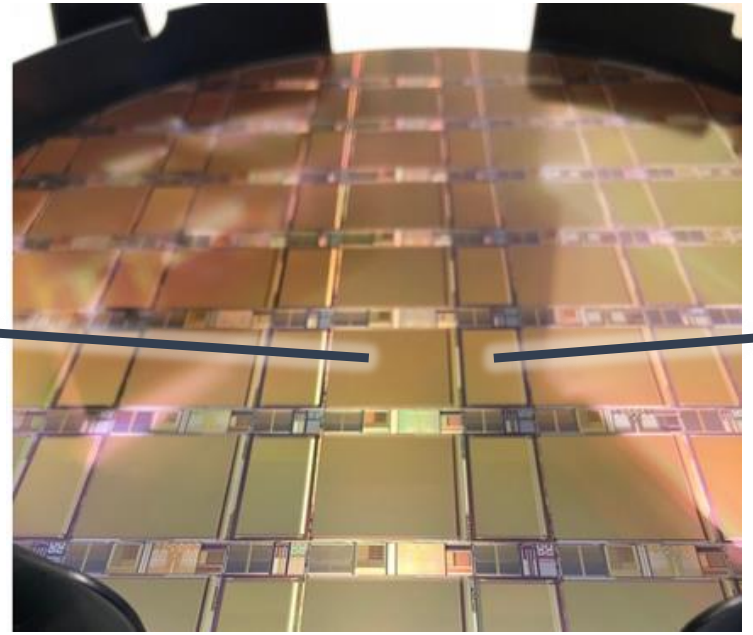
- Jitter considerations in the design of a PLL (CDR):
  1. A Charge Pump (CP) CDR is a second order (usually) closed loop system characterized by its bandwidth (BW) and damping ratio (β)
  2. Time interval error (TIE) or absolute jitter of a the VCO will accumulate for frequencies higher than the -3dB cutoff (as if it was a "free-running VCO")
  3. Input (CMD) TIE jitter will pass through the CDR (no jitter cleaning) for frequencies lower than the -3dB cutoff
  4. Jitter peaking must be avoided by designing for maximum phase margin (optimal β)
  4. Noise at the input of the VCO (charge pump current noise, PD,DIV synchronous jitter) will be converted to jitter by the gain of the VCO. Lowering the VCO gain reduces jitter
  5. The filter resistance must not contribute significant thermal noise. The resistor can be reduced while the CP current can be increased to compensate



TJ – Submission: Sensor chips



- Measurement results from the TJ-Investigator indicated the **enhanced radiation tolerance** of the **modified process** sensor
- ***Design of two large-scale demonstrator DMAPS, with integrated in-pixel readout logic for the ATLAS ITk***



MALTA: 2x2cm²

- Novel **asynchronous readout** architecture
- Time-walk based charge information

TJ-Monopix: 1x2cm²

- **Synchronous column – drain readout** architecture
- 6-bit ToT information