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PROGRESS IN ASYNCHRONOUS PIXEL DESIGNS IN TOWERJAZZ 180 NM

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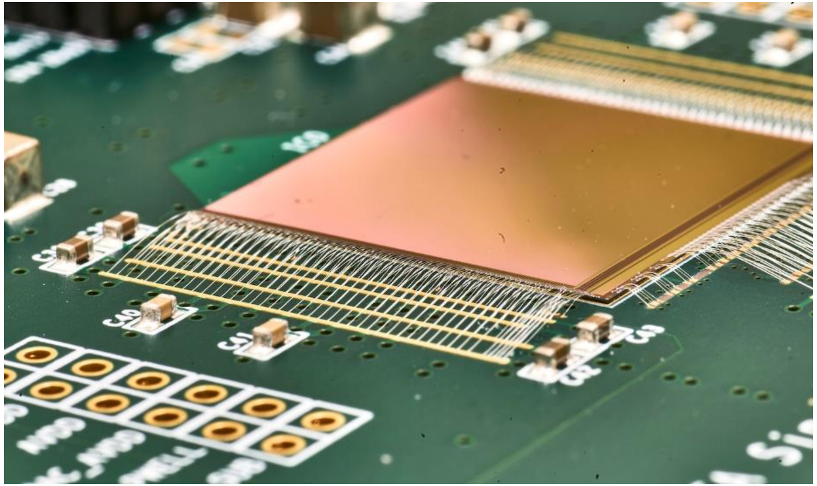
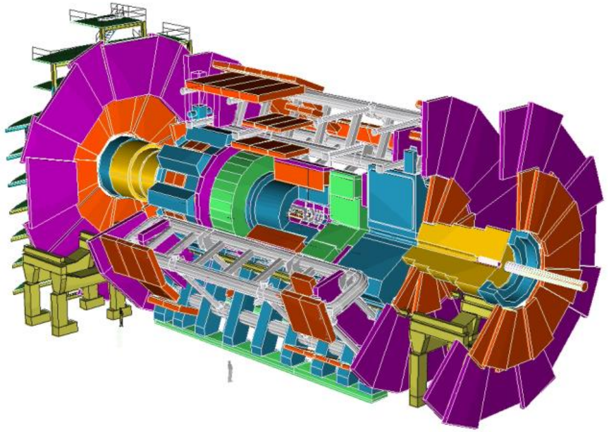
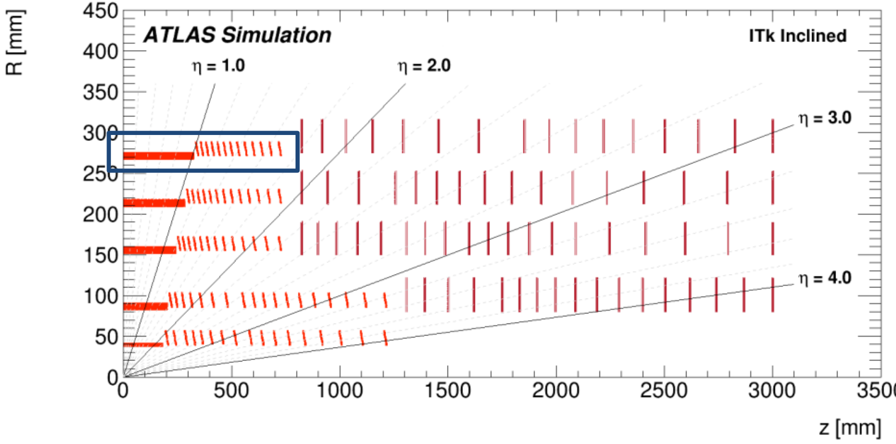


Introduction

- The ATLAS experiment will undergo a major upgrade for the High-Luminosity LHC phase
- CMOS pixel sensors are considered for the outermost layer of the ITk pixel detector

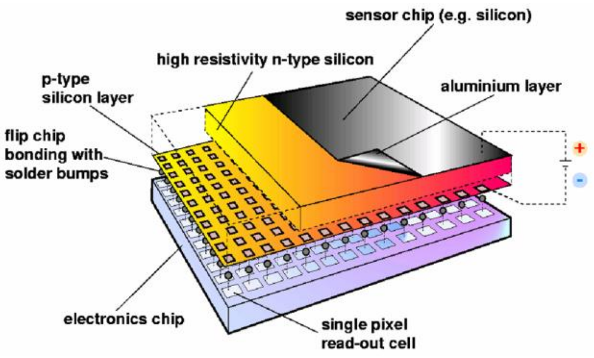


- Requirements for layer 4:
  - High efficiency (**>97 %**)
  - Fast timing (**<25 ns** bunch crossing time)
  - High hit rate capability (hit rate **~2 MHz/mm²**)
  - Low power consumption (**<0.5 W/cm²**)
  - Radiation tolerance (**1.5×10^{15} n_{eq}/cm^2** NIEL and **80 Mrad** TID)
  - SEU robustness



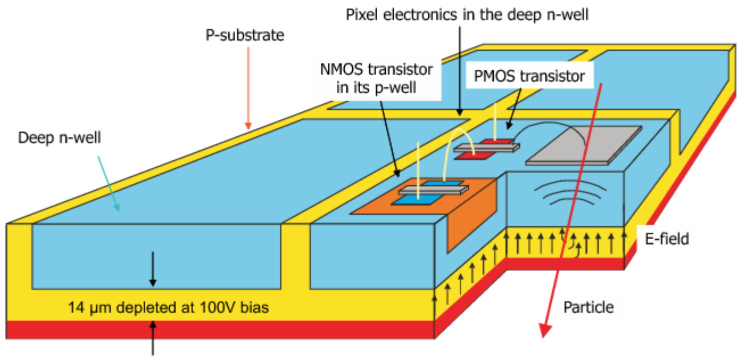
Hybrid vs. CMOS pixel detectors

- **Hybrid** pixel detectors



- Used in the majority of present systems
- Sensor and readout on separate chips – can be optimised separately (different materials, high sensor bias voltages)
- Fast charge collection, good radiation tolerance
- Complex and costly assembly due to fine-pitch bump bonding

- **CMOS** monolithic pixel sensors

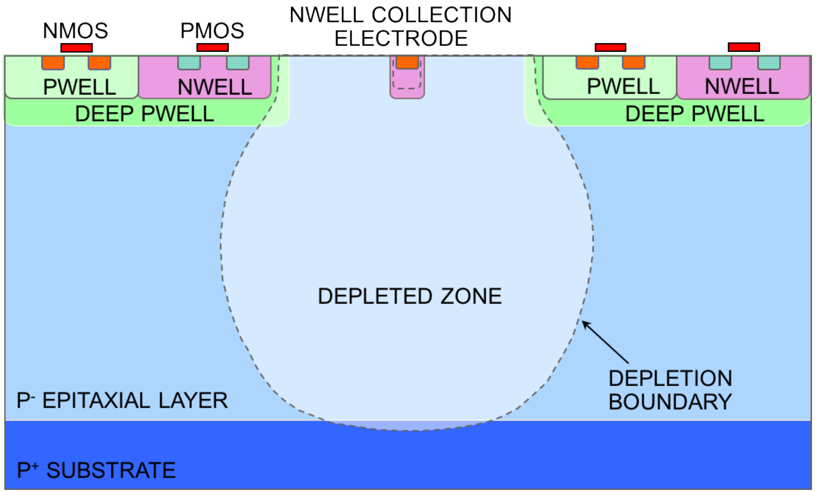


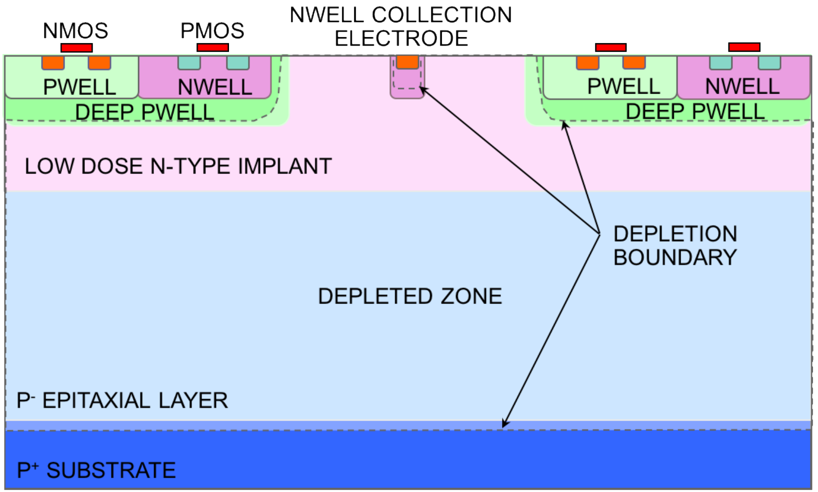
- Sensor and readout integrated into the same silicon die (large or small collection electrode)
- High granularity, low power consumption, significant reduction in material budget
- No bump-bonding: easy integration, lower cost
- Recent progress in radiation hardness

Sensors in the TowerJazz 180 nm technology

- **Small collection electrode** design with high resistivity (> 1 kΩ cm) p-type epitaxial layer (25 µm thick → MIP charge ~1500 e$^-$)
- Deep p-well shielding n-well to allow **full CMOS**
- **Reverse bias** (~6 V) to further reduce input capacitance and increase depletion volume

- Modified process – adding a **planar n-type layer** to improve depletion under the deep p-well near the pixel edges
- A fully depleted epitaxial layer results in faster charge collection and **better radiation tolerance**
- No circuit or layout changes required

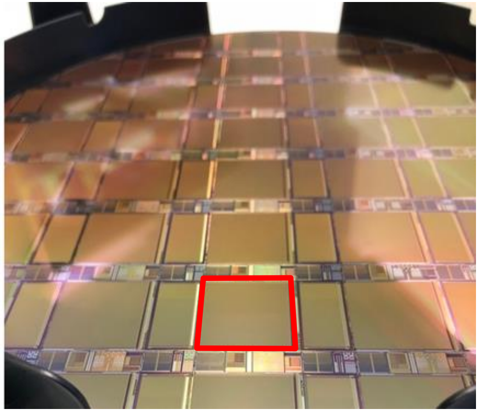


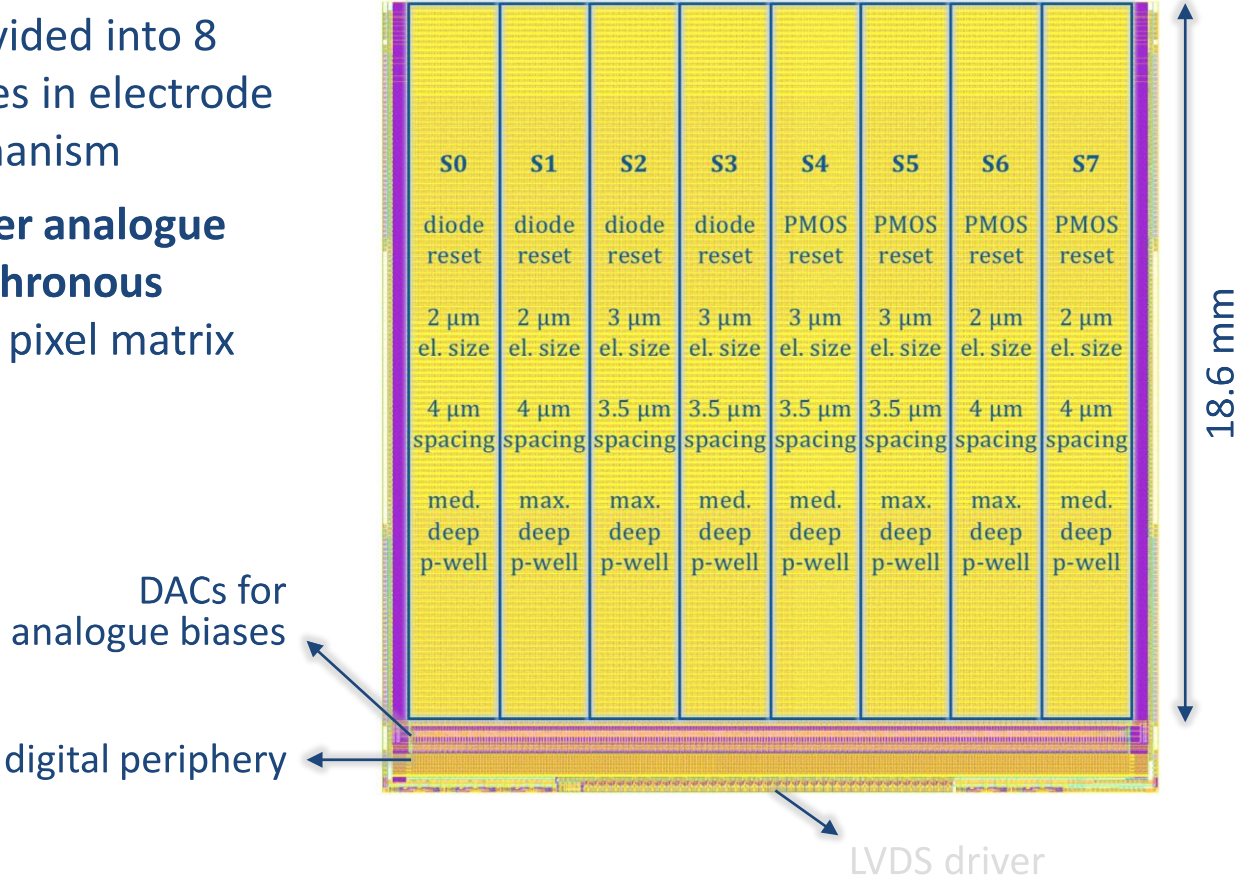


W. Snoeys et al. https://doi.org/10.1016/j.nima.2017.07.046

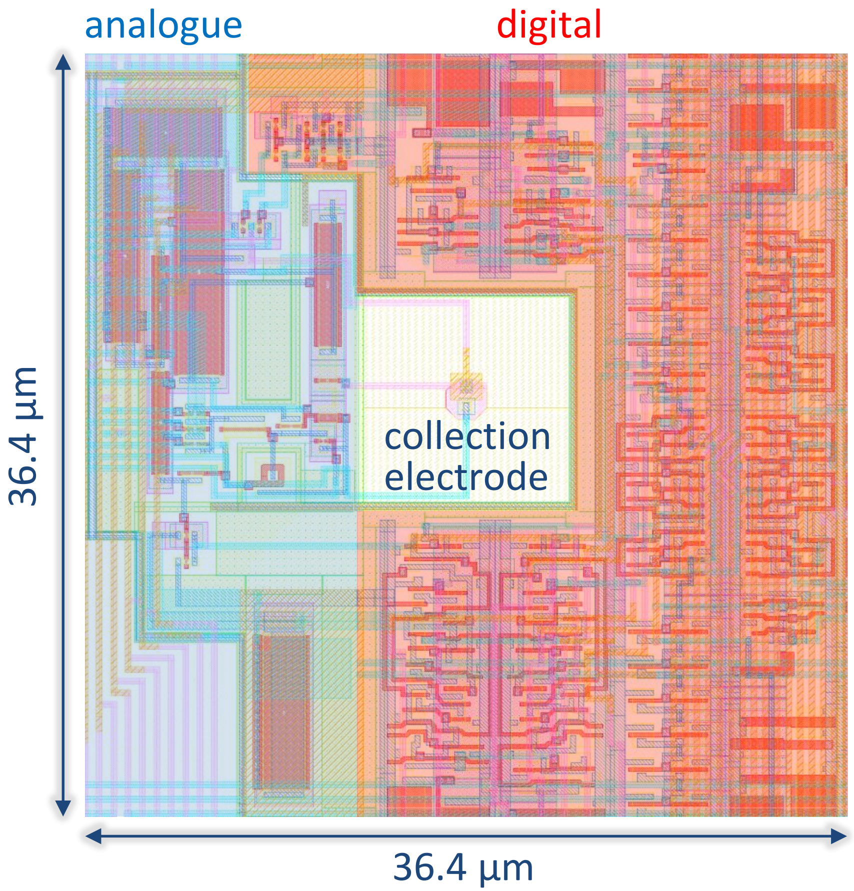
MALTA pixel sensor

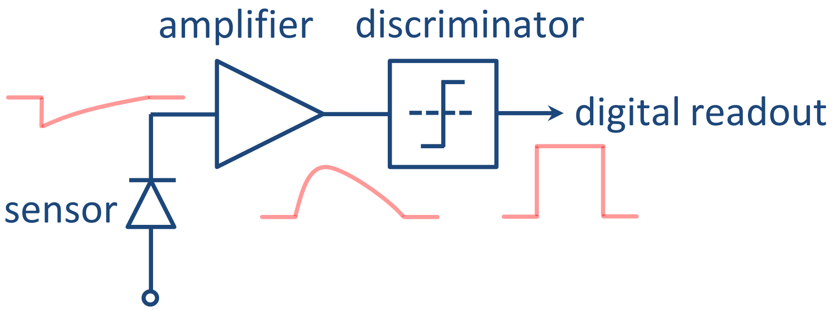
- The 512x512 pixel matrix divided into 8 sectors with slight differences in electrode size, spacing and reset mechanism
- Design based on a **low-power analogue front-end** and a novel **asynchronous architecture** to read out the pixel matrix





The MALTA pixel

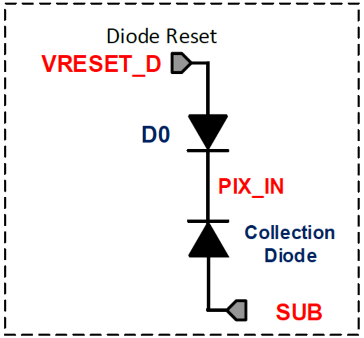


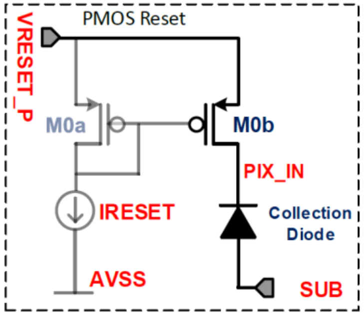


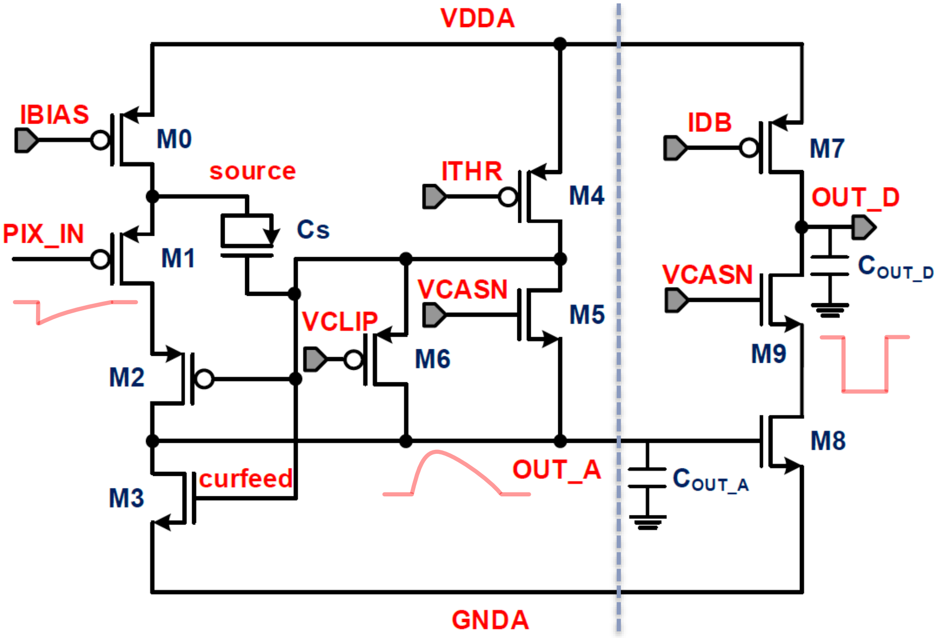
- Sensor and analogue front-end (shaper-amplifier and discriminator) shielded from digital part to **minimise crosstalk**

Analogue front-end design

- Fast, low power, low noise amplifier based on a previous design for the ALICE upgrade (shaping time **~25 ns**, power **<1 μW/pixel**)
- Designed for a threshold of **~200 e$^-$** with a simulated ENC noise of **<10 e$^-$** and RMS channel-to-channel threshold variation of **~10 e$^-$**



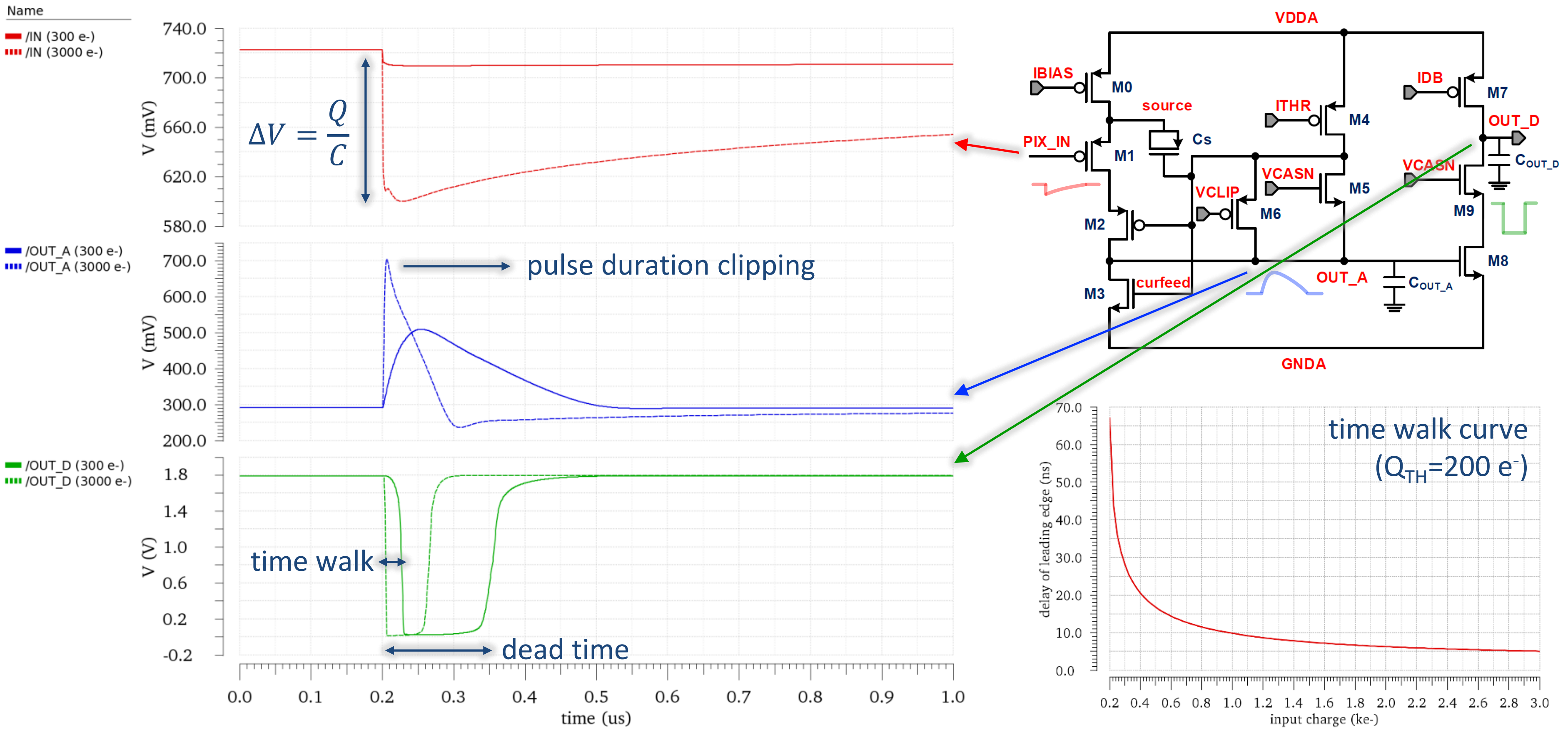




D. Kim et al. https://doi.org/10.1088/1748-0221/11/02/C02042

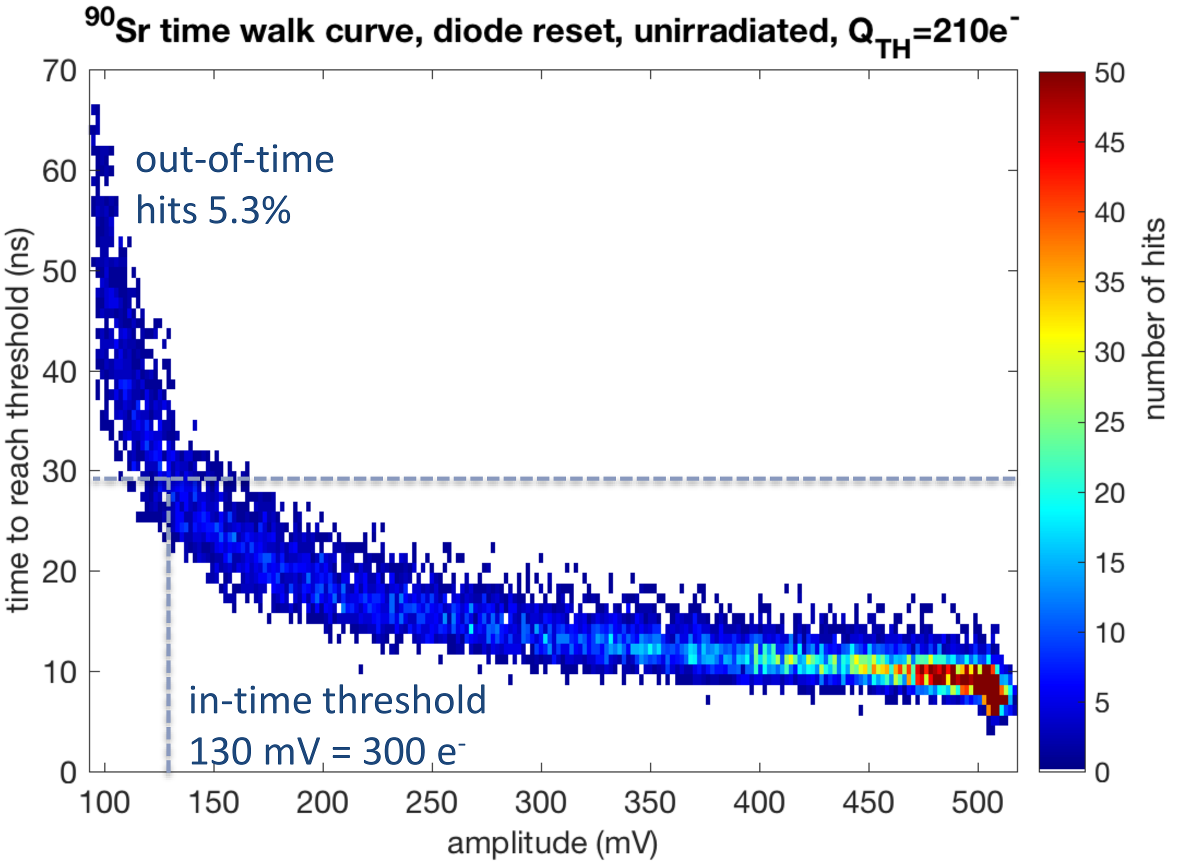
- Input node reset using either a diode or a PMOS
- M1 acts as a source follower, amplification caused by transfer of charge from C_S to C_{OUT_A} ($C_S >> C_{OUT\_A}$)
- M3-M5 form a low-frequency feedback to stabilise OUT_A
- M6 clips the analogue pulse for high input charges
- M7-M9 form a simple discriminator

Analogue front-end timing optimisation



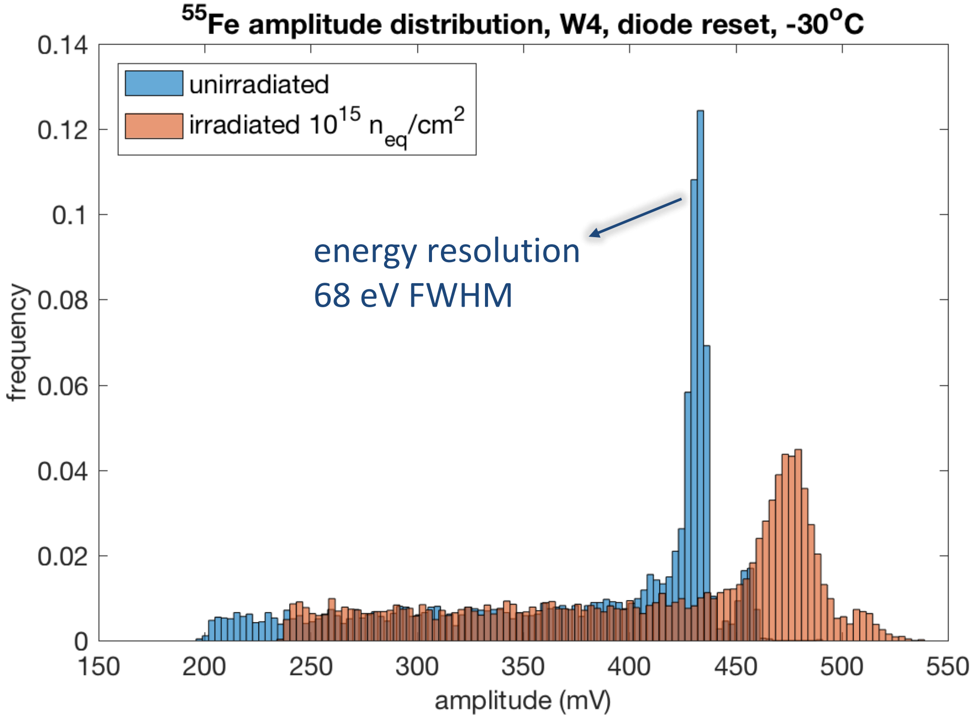
Analogue front-end timing measurements

- Time walk measurement performed with a ^{90}Sr source using special pixels to monitor the analogue output
- With a threshold of 210 e$^-$ the **in-time threshold** is **300 e$^-$** (20% of MIP charge)
- Out-of-time hits mostly due to charge sharing (measurement done on a single pixel)



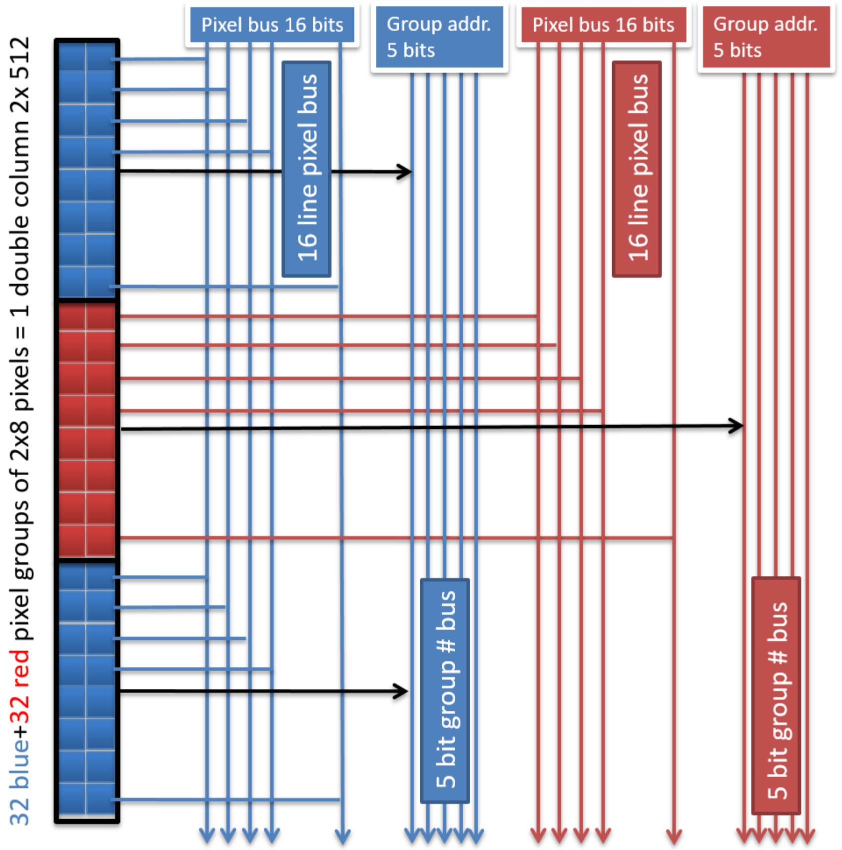
Front-end response before and after irradiation

- MALTA chips irradiated with neutrons up to **10^{15} n_{eq}/cm^2** (with a background TID of **1 Mrad**)
- Monitoring pixels also used to study sensor and front-end response to ^{55}Fe source before and after irradiation
- Characteristic K_α and K_β peaks of the source clearly visible even after irradiation
- Irradiated front-end shows a slightly higher gain due to TID and a somewhat increased noise



MALTA asynchronous readout architecture

- Front-end discriminator outputs are injected into double-column digital logic generating a **short pulse** (0.5-2 ns)
- Data is transmitted **asynchronously** over high speed buses without clock distribution over the active matrix to **save power**
- 2 independent buses serve alternating 2x8 pixel groups (one bus for the red groups and another for the blue groups)
- 22 bits per bus: reference (1b) + pixel pattern (16b) + group address (5b)
- In-pixel logic includes hit arbitration in case of simultaneous hits within one 2x8 group



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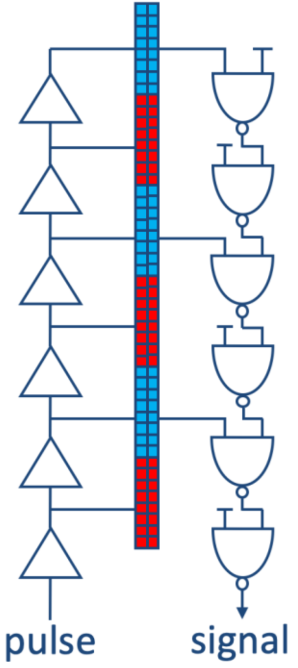
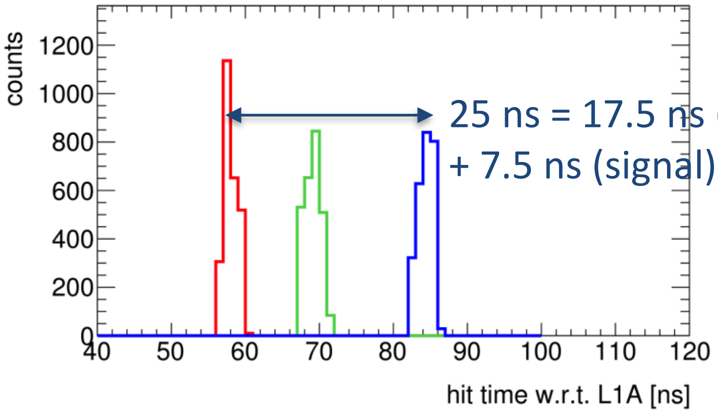
Asynchronous readout architecture – measurements

- Hit signals from the pixels are buffered and arrive at the end-of-column with a maximum propagation delay of **~7.5 ns**



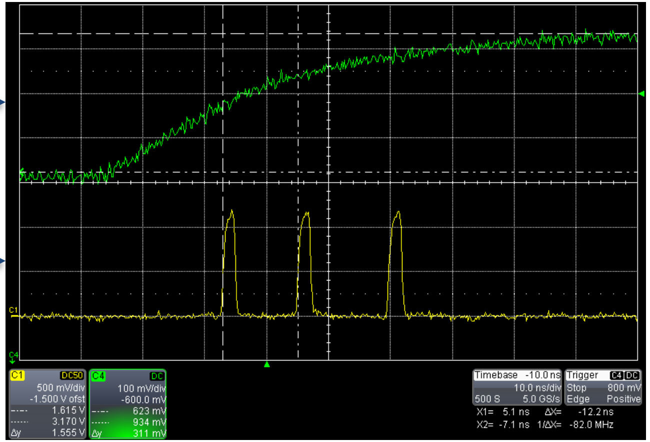
(measured by pulsing pixels on top, middle and bottom of the column)



25 ns = 17.5 ns (pulse) + 7.5 ns (signal)

analogue output of one pulsed pixel

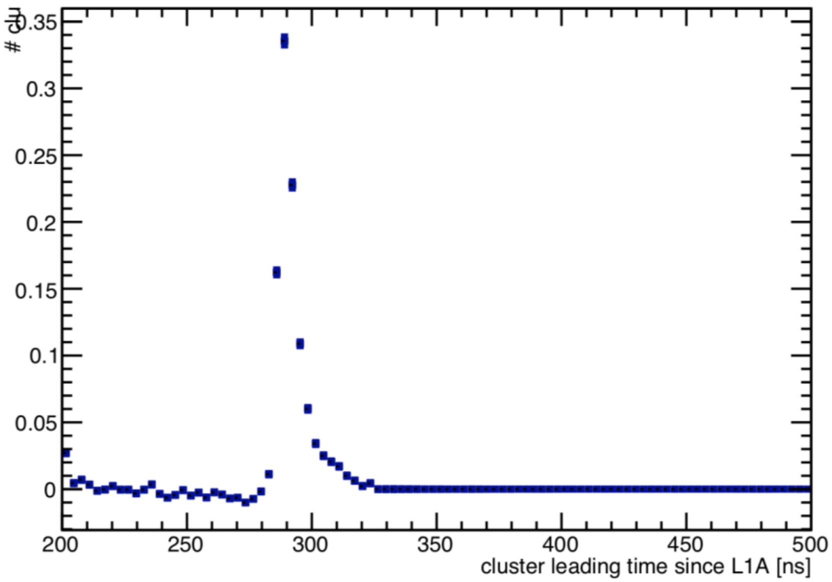
reference signal

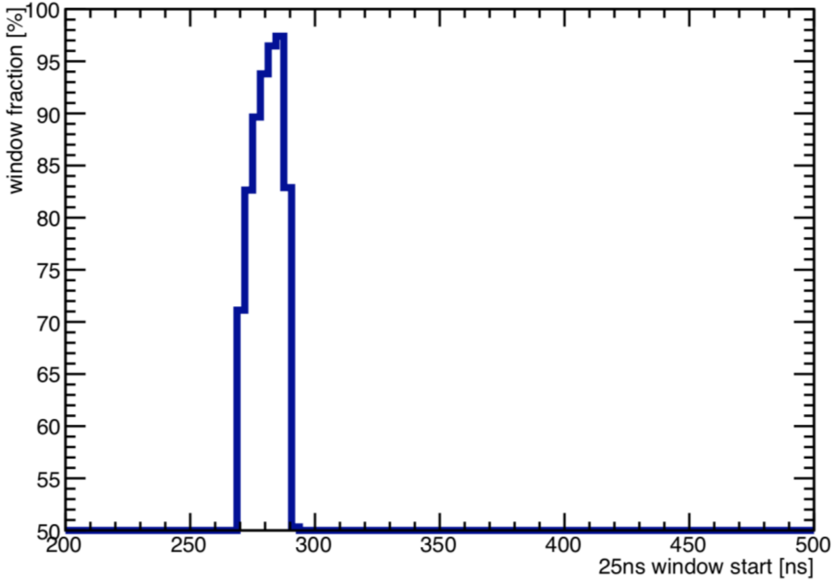


Front-end and readout timing measurements

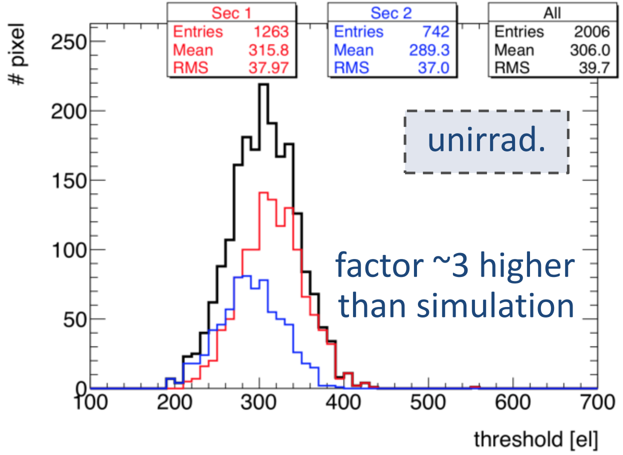
- Time walk can also be obtained by measuring the delay of digital output signals with respect to a fast trigger (scintillator)

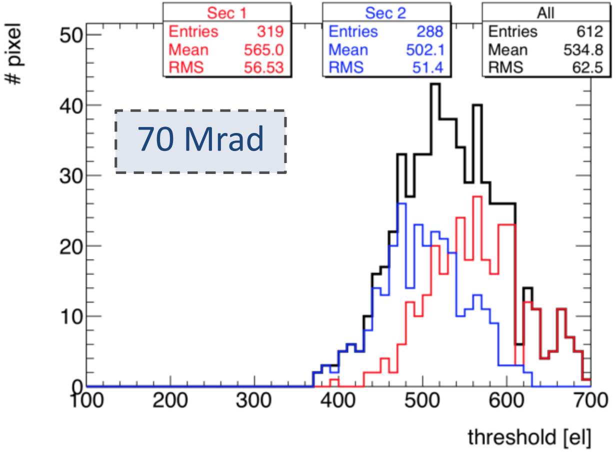
- In-time efficiency for leading signals in clusters reaches **98%** with a 300 e^- threshold (no correction for the **7.5 ns** propagation delay down the column)

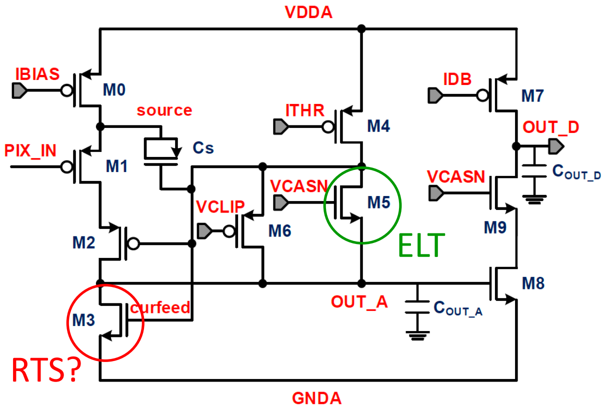


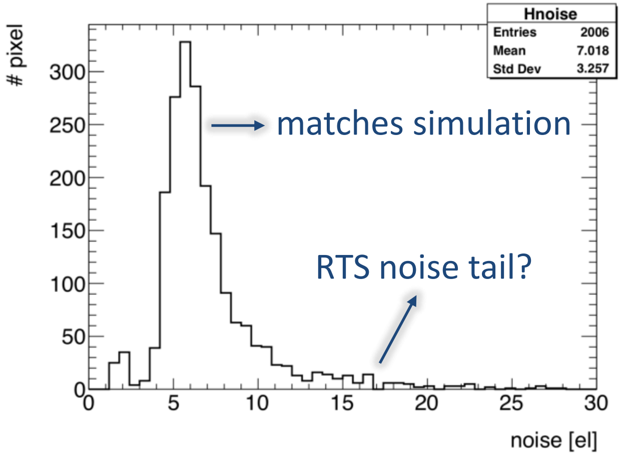


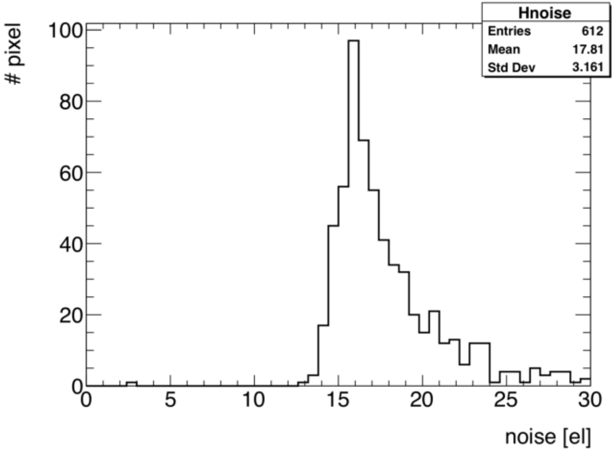
Threshold dispersion and noise before and after TID



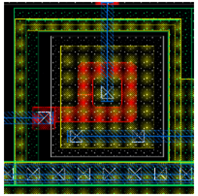








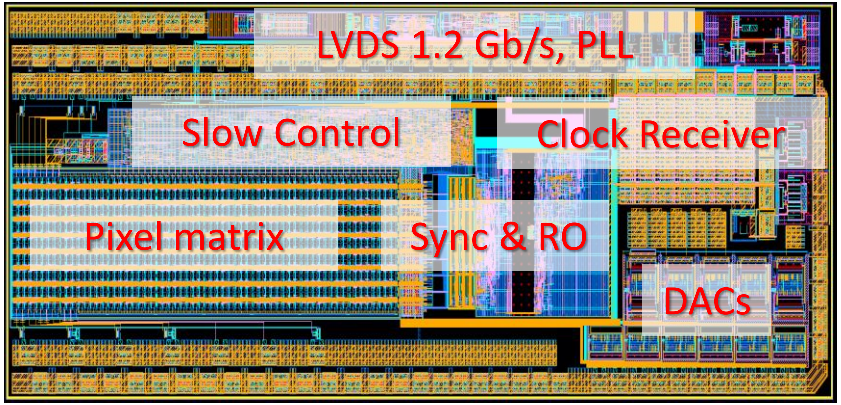
- Front-end still operational after 70 Mrad due to ELT in sensitive branch



- Increase in threshold spread and noise under investigation

The miniMALTA prototype

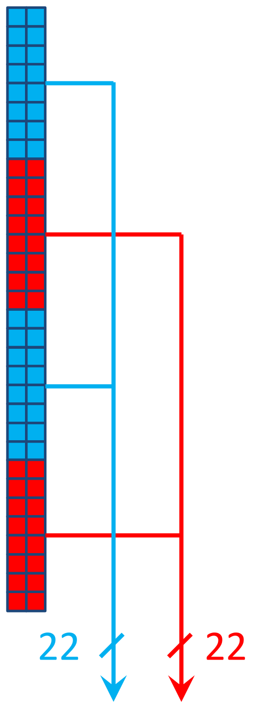
- The next small prototype after MALTA, contains:
  - A 64x16 pixel matrix with the same designs as MALTA, but enlarged transistor to fix RTS noise
  - A block to synchronise signals at the periphery
  - A priority encoder readout and serialiser to send the data out at 1.2 GB/s
  - A new modular DAC design (Francesco)
  - Process modifications for improved efficiency after irradiation (Roberto)

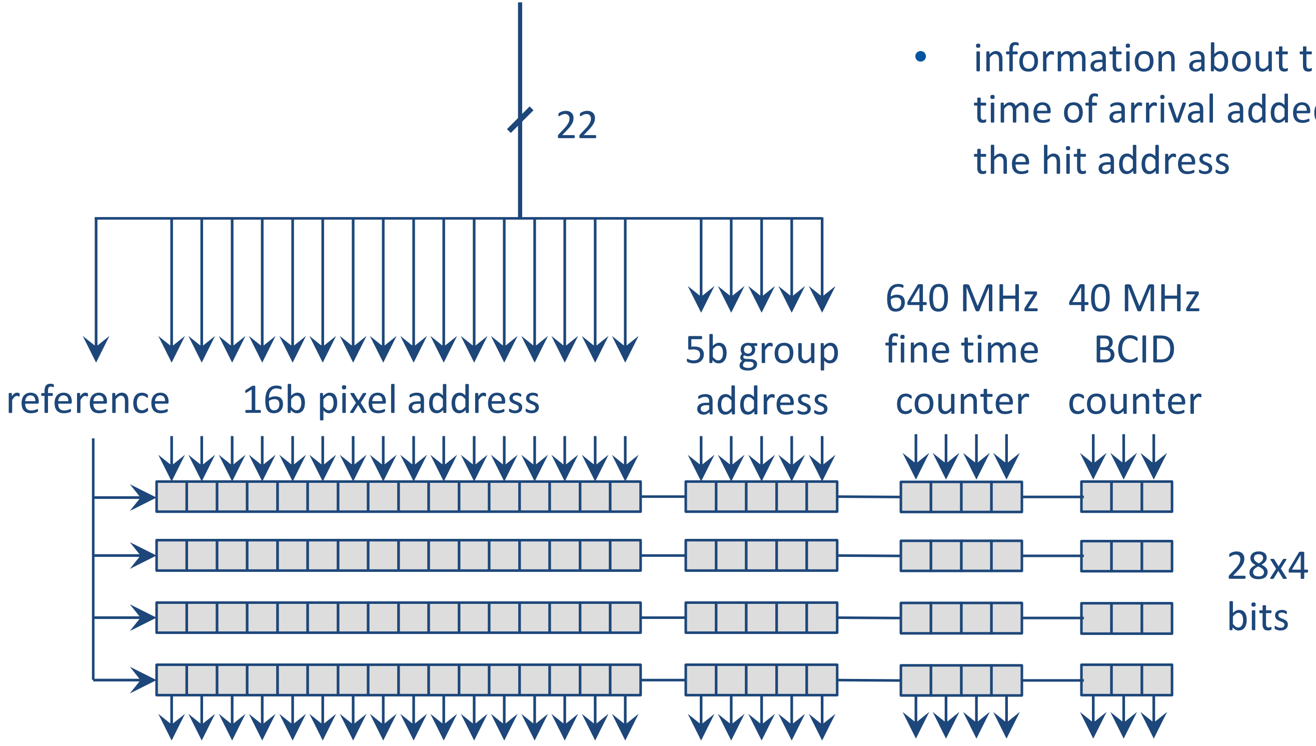


- Chip recently back from fabrication, first tests show that the chip is functional (configuration, analogue pulses, source response)

Synchronisation in miniMALTA

- hits at the output of the MALTA double column stored asynchronously into FIFO RAM memory and read out synchronously

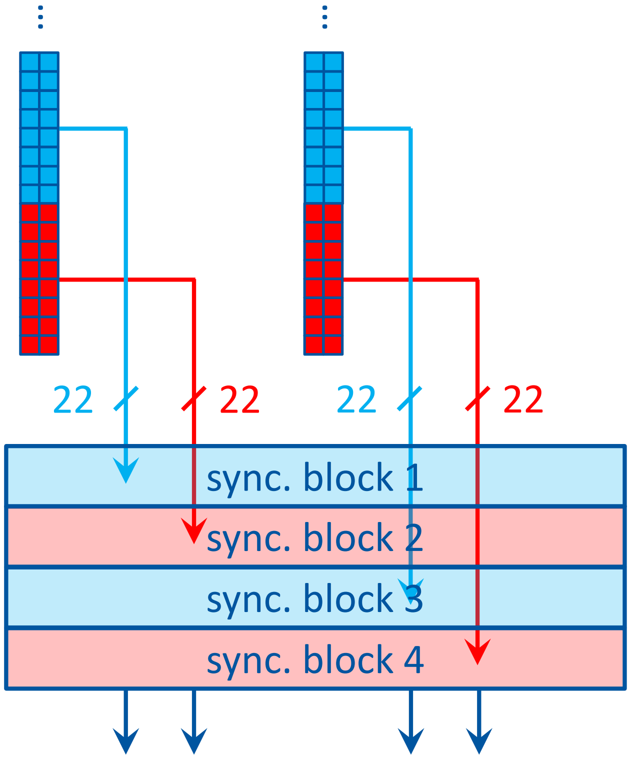


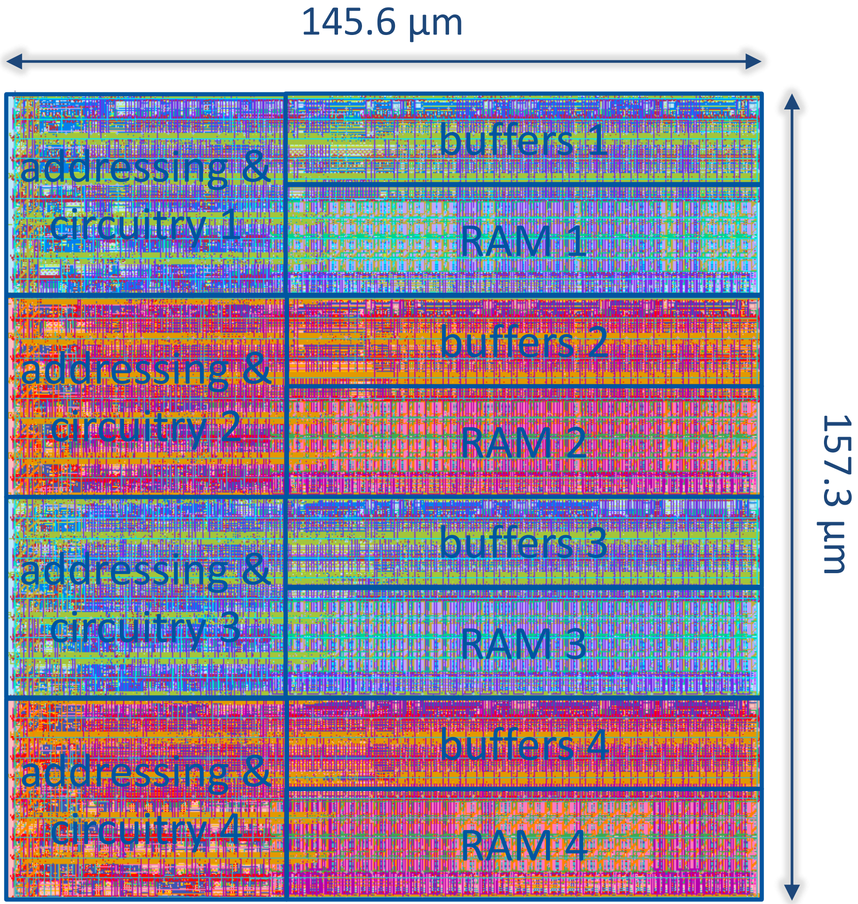


- information about the time of arrival added to the hit address

Synchronisation in miniMALTA

- 4 columns grouped together to optimize layout space





Conclusion and outlook

- The MALTA CMOS pixel sensor was developed in view of the ATLAS High-Luminosity upgrade
- The large pixel matrix implements a fast, low-power analogue front-end and a novel asynchronous readout architecture
- The chip has been extensively characterised in lab measurements and testbeam, and shows good results in terms of front-end performance and readout capability

- The miniMALTA prototype includes a synchronization block at the chip periphery and other improvements

- Designs in TowerJazz 180 nm continue towards a full-scale ATLAS-ready pixel detector chip with a synchronous architecture (TJ Monopix V2)

Thank you for your attention!

QUESTIONS?