MALTA & LAPA

Measurement results and more..

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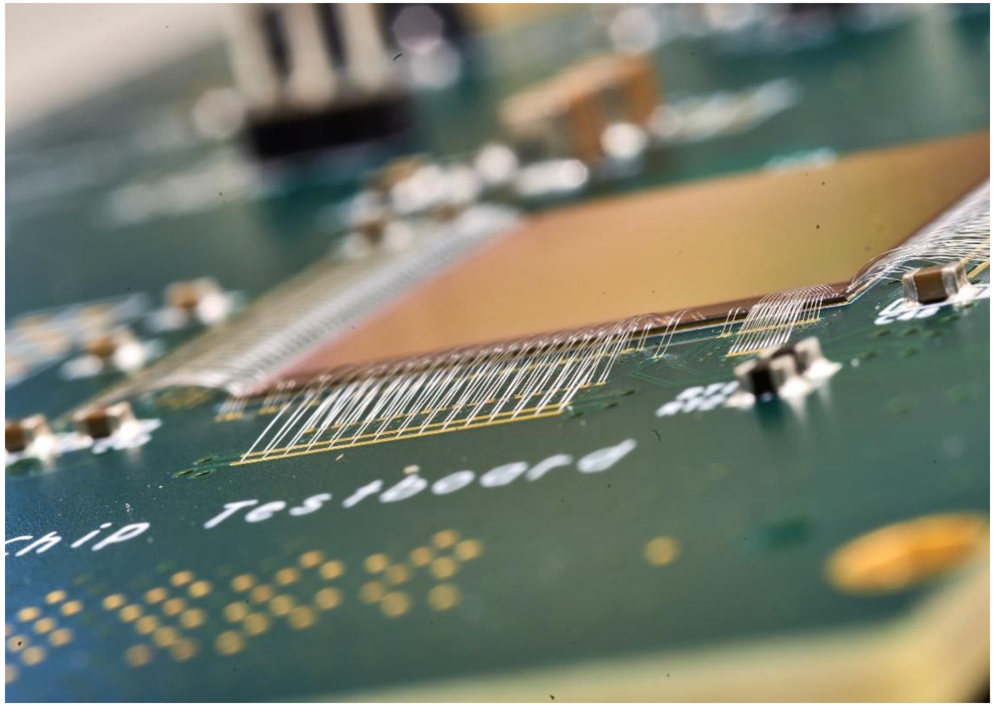
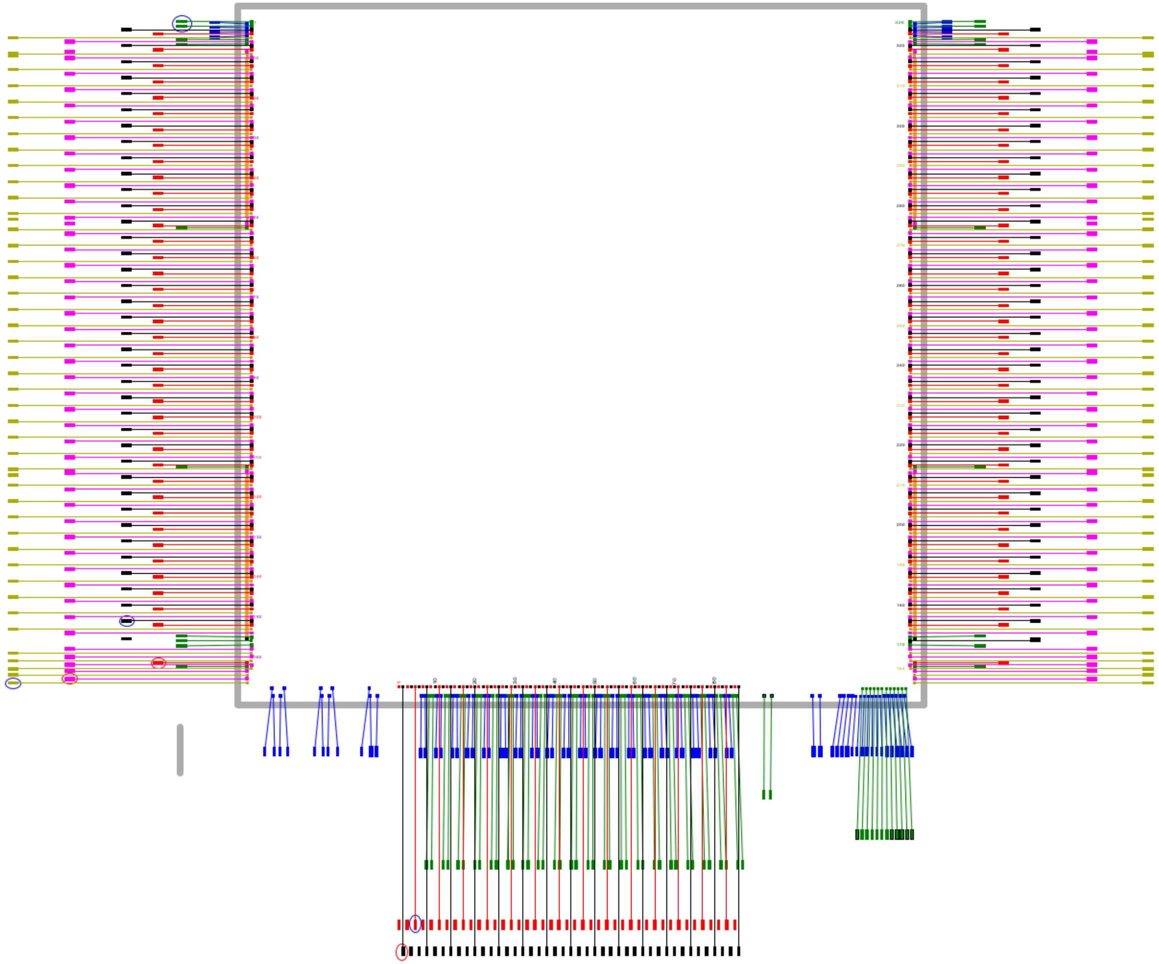
Outline

1. MALTA chip
   - From Assembly to Efficiency
   - Rad Hardness studies
   - Improvements and MiniMalta
2. Other R&D on MALTA
3. LAPA
   - Collection of results
4. Conclusions



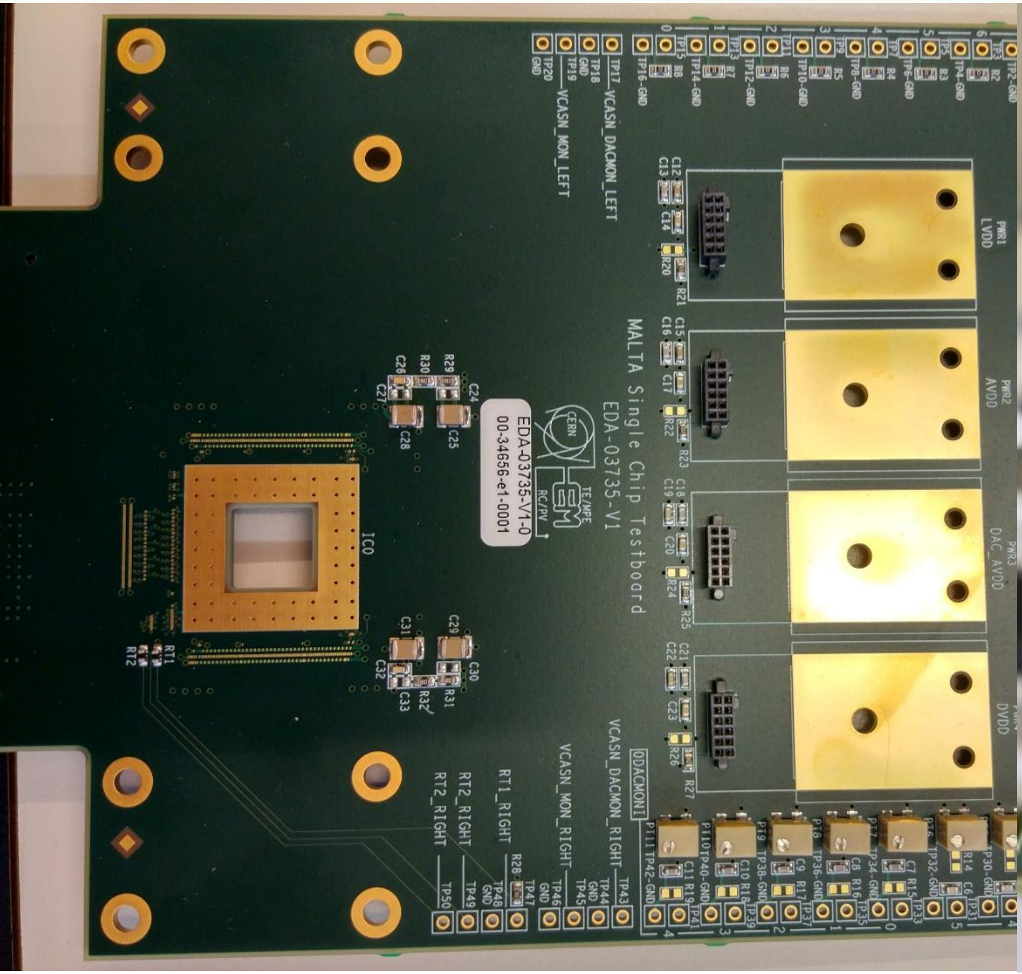
MALTA carrier board

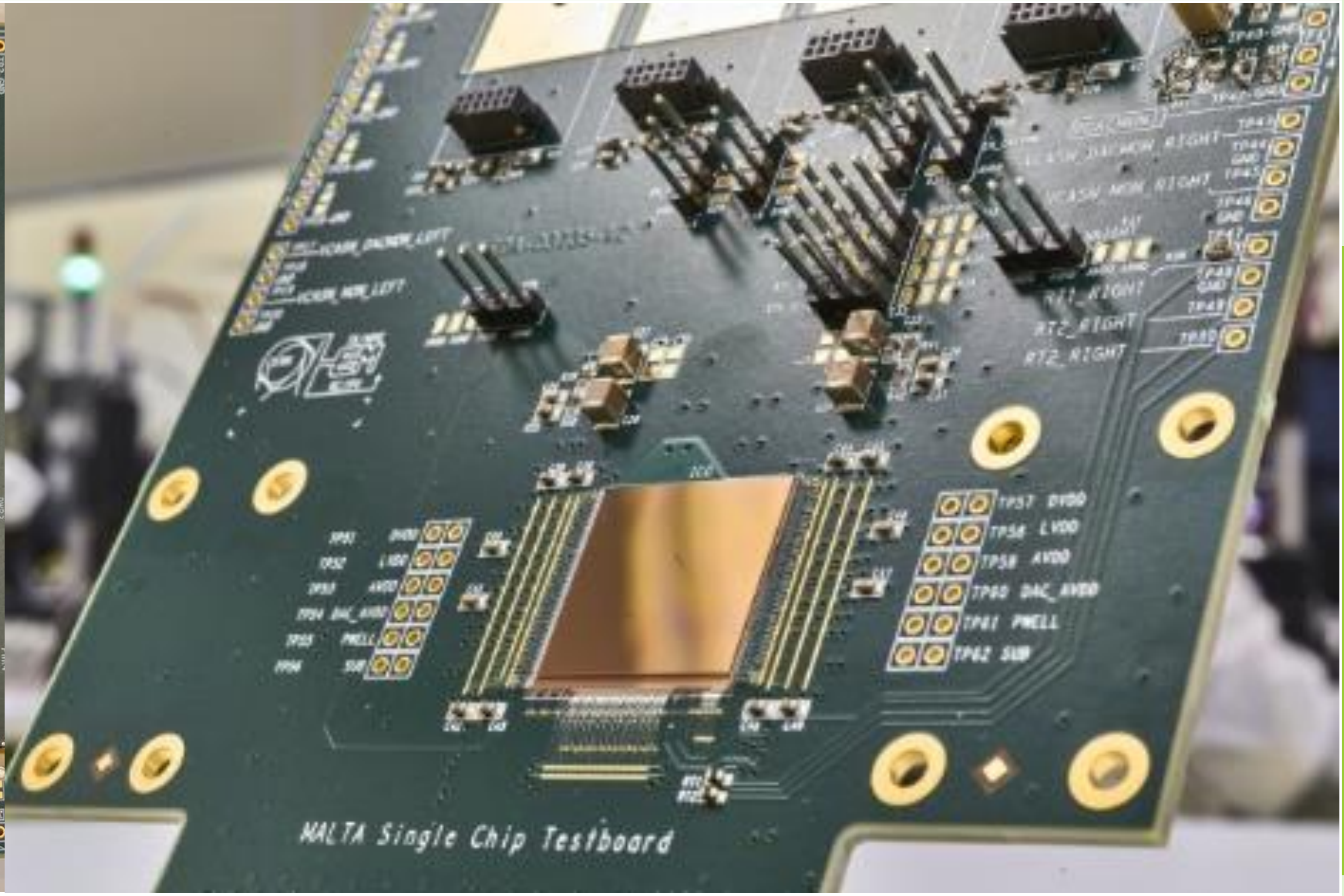
From last year meeting: MALTA board to be tested



Challenging PCB design: 700 to 1000 wirebonds

MALTA carrier board



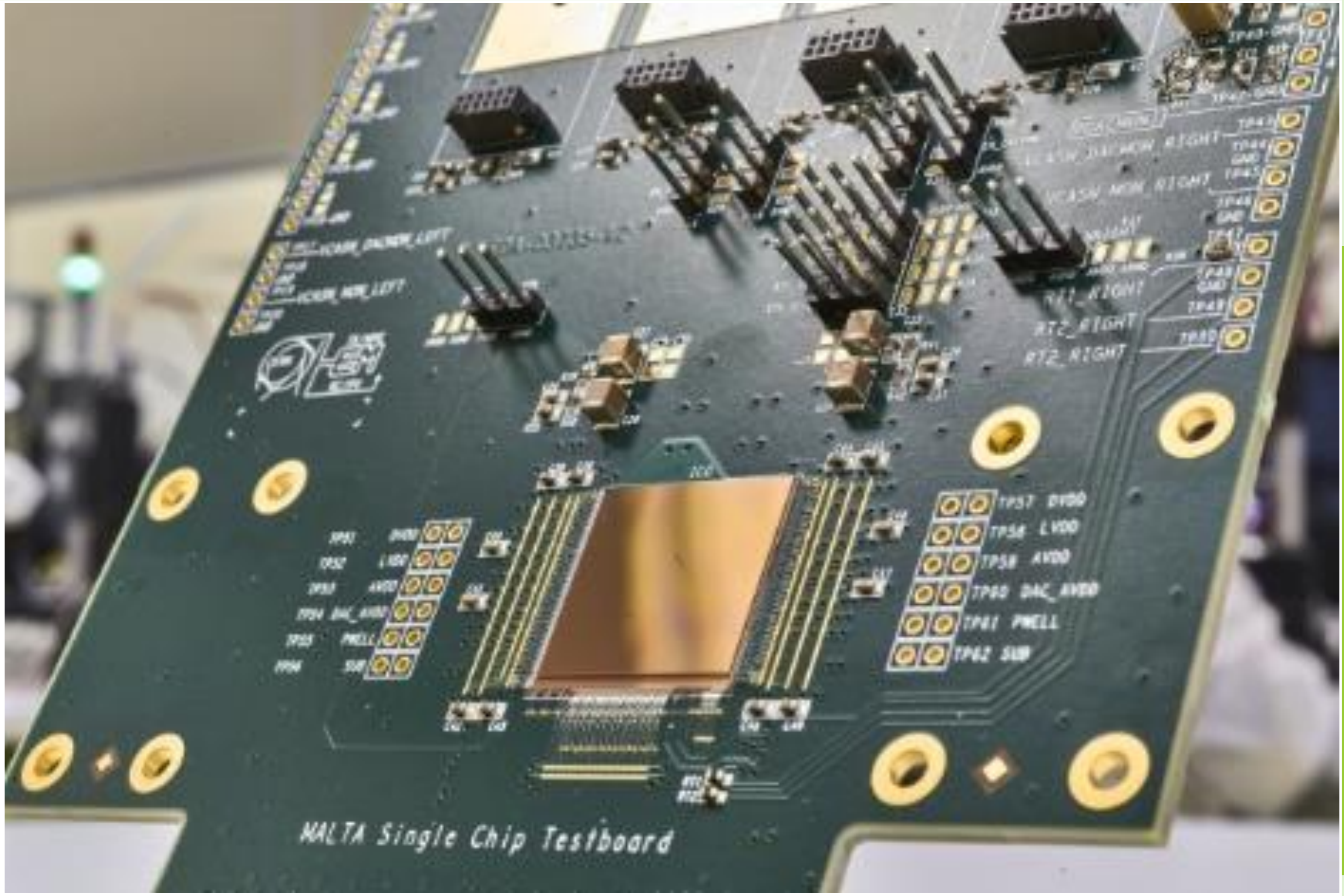


Single Chip V3 available, Double Chip V2 in production

MALTA carrier board

From V1 to V3

- Fix on interface with FPGA readout
- Separated bus forAVSS DVSS
- Probing vias
- Star ground connection
- Improved power filter
- Improved decoupling capacitors



Zero wirebonding failures due to PCB

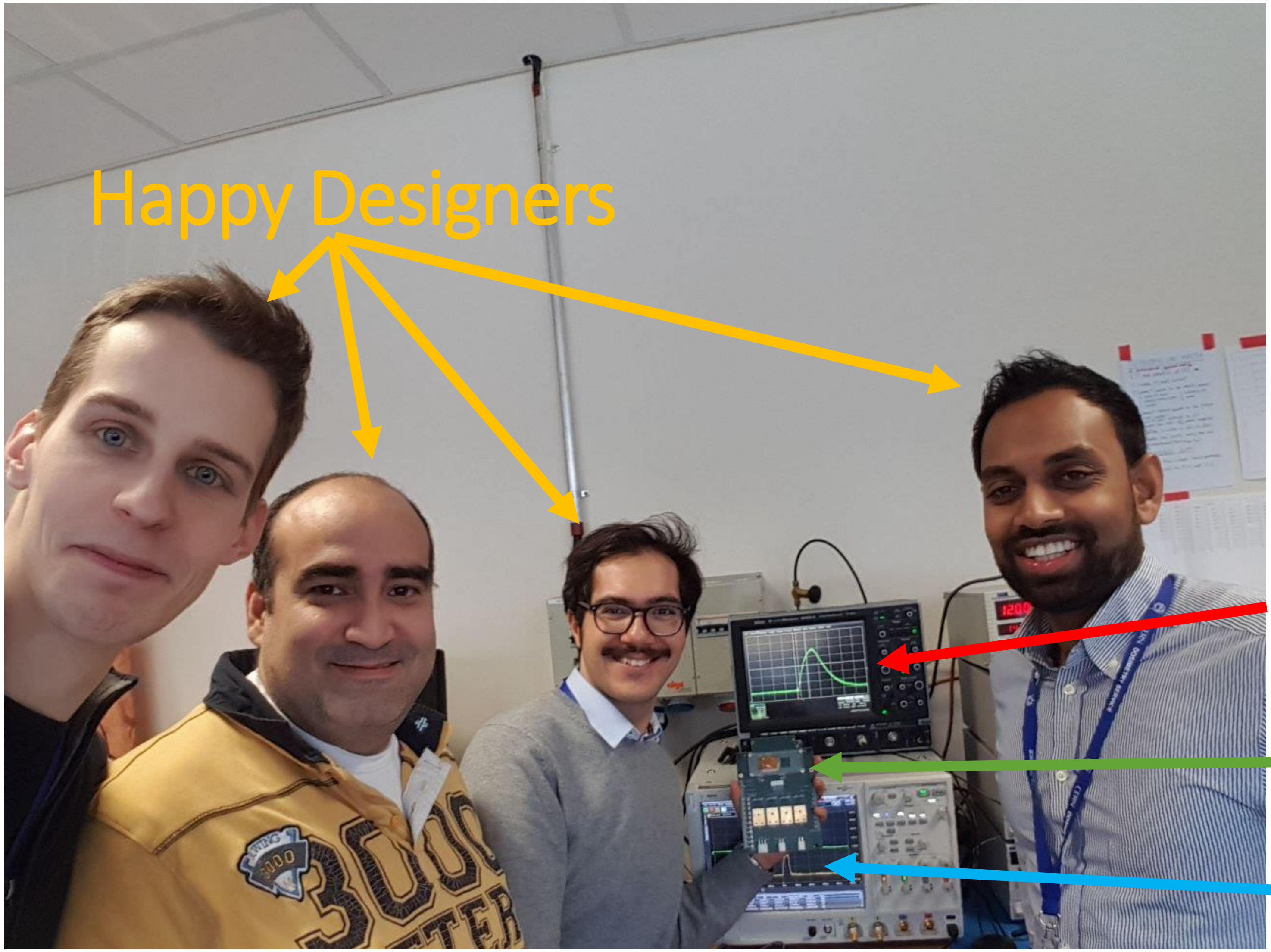
First signs of life from MALTA

ANALOG pixel output

MALTA (not the one under test)

Digital signal from read-out

First signs of life from MALTA

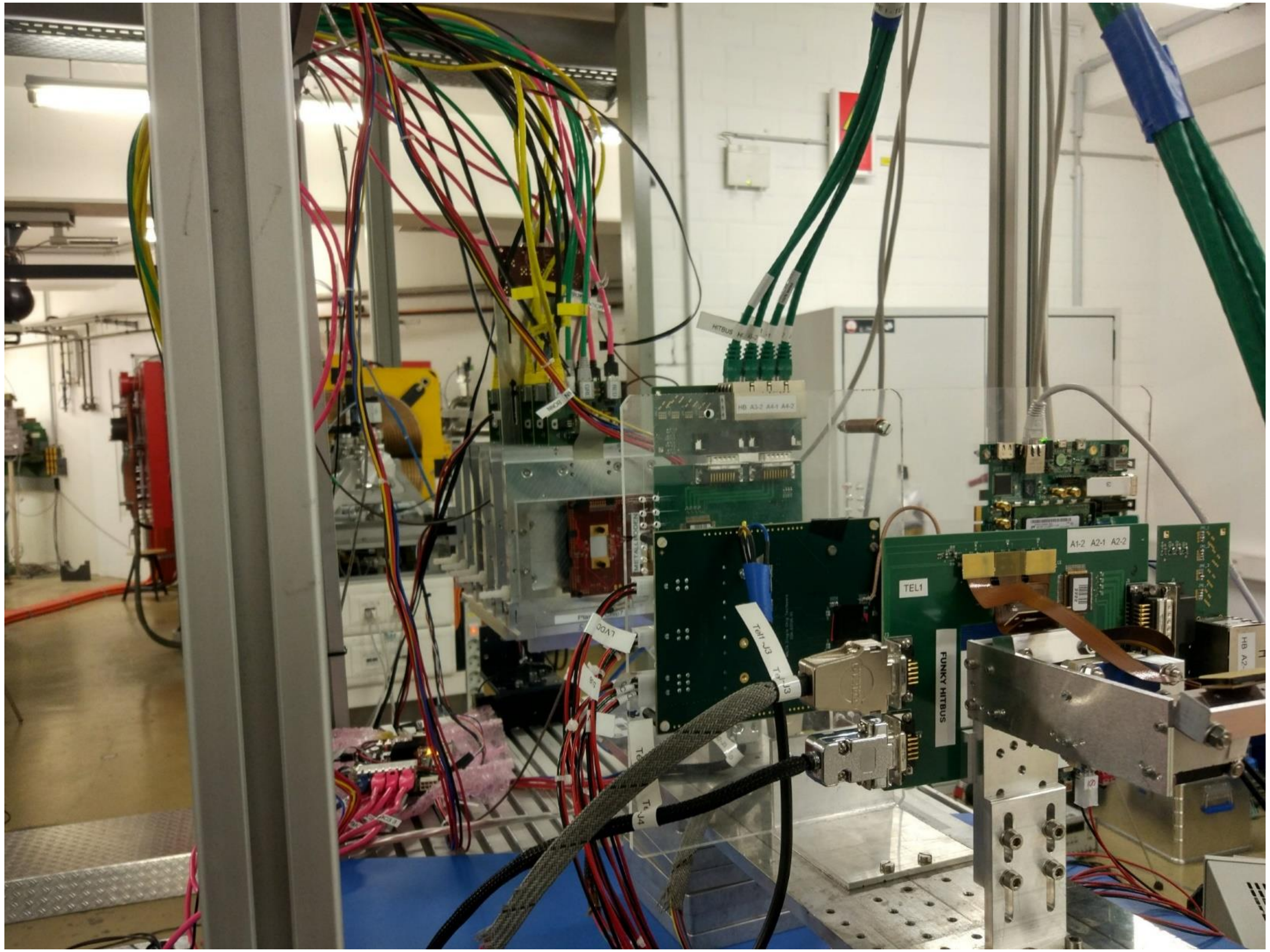


ANALOG pixel output

MALTA (not the one under test)

Digital signal from read-out

First test beam campaign

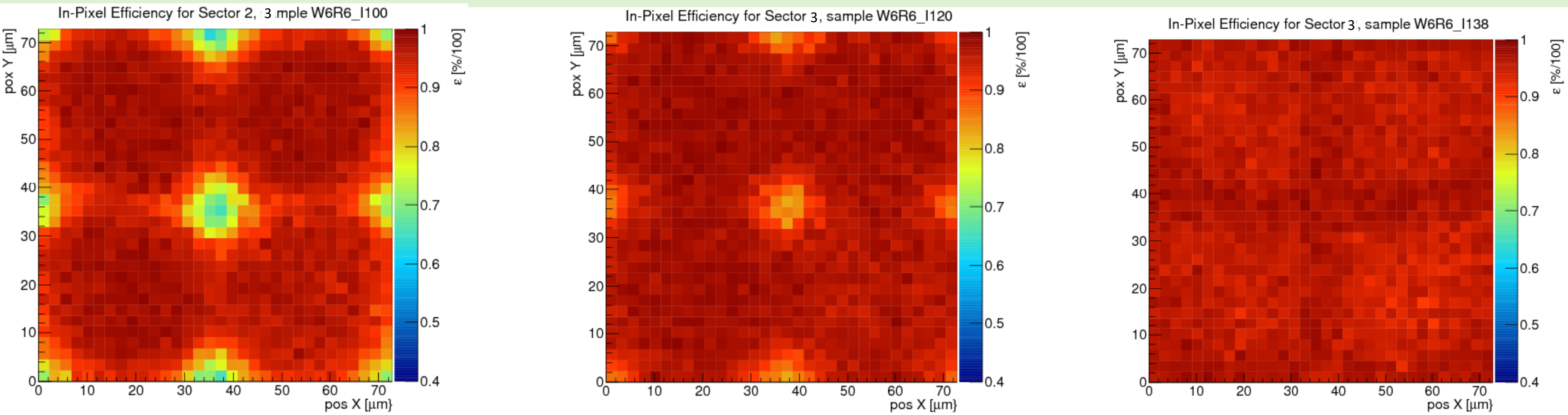


ELSA-BONN Exposed MALTA to a 2.5 GeV electron beam during 3 days

We took ~2.5 M usable events

SPS- CERN Down to in-pixel efficiency

Efficiency in testbeam before and after irradiation



Unirradiated: lowering the threshold gives full efficiency

Decreasing threshold from ~600 e^- to ~250 e^- (unirrad.)

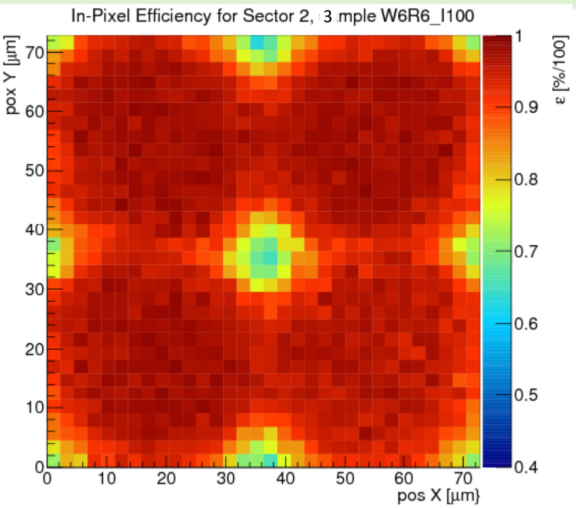
3

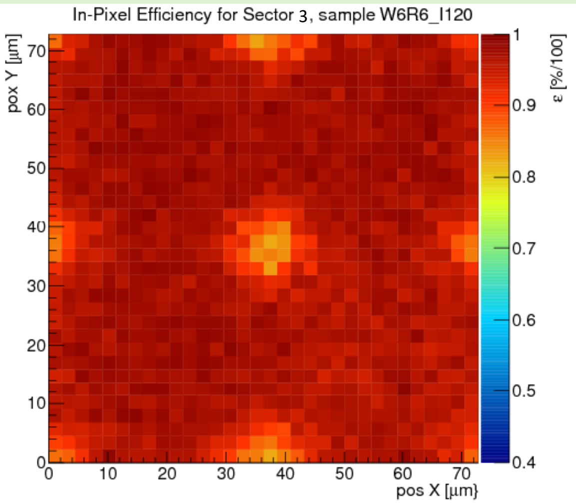
3

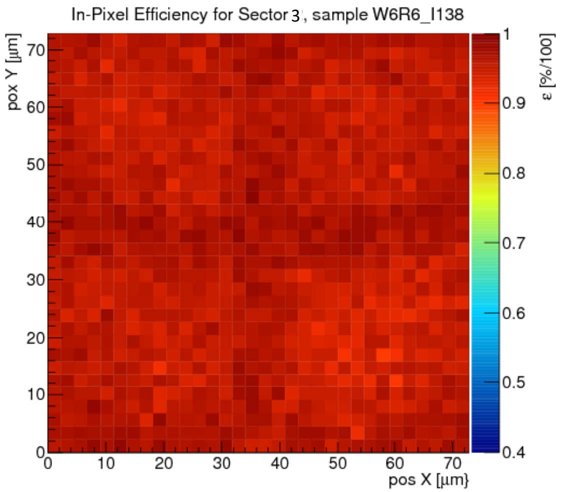
Cannot go lower with threshold because of RTS noise and masking issue

Solution for both under study.

Efficiency in testbeam before and after irradiation

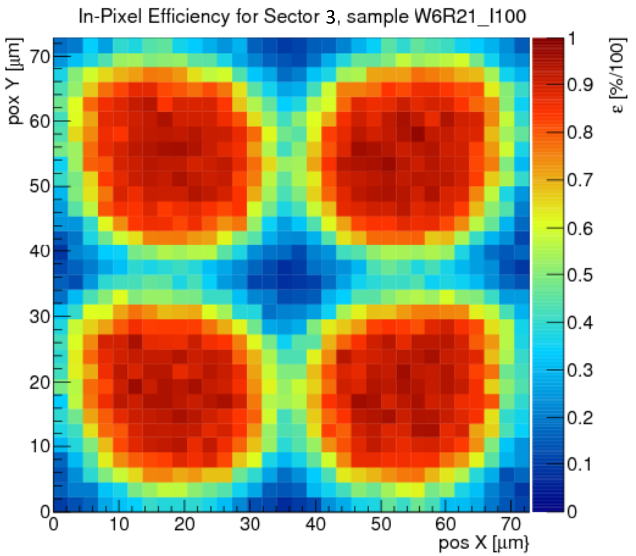


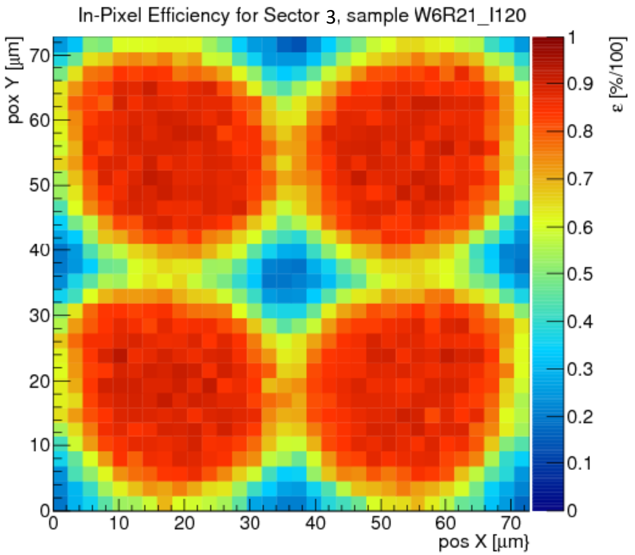




Unirradiated: lowering the threshold gives full efficiency

Decreasing threshold from ~600 e^- to ~250 e^- (unirrad.)/350 e^- (irrad.)





Could not reach lower threshold

(RTS + MASKING ISSUE)

Neutron irradiated 5×10^{14} neq/cm^2

inefficiency in pixel corners due to low lateral electric field

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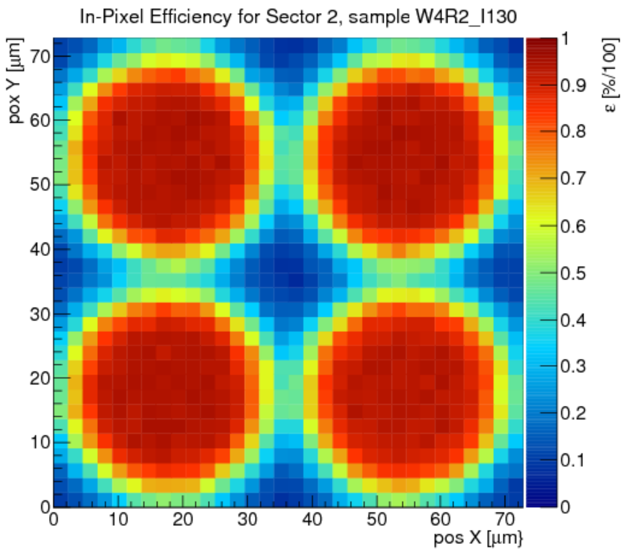
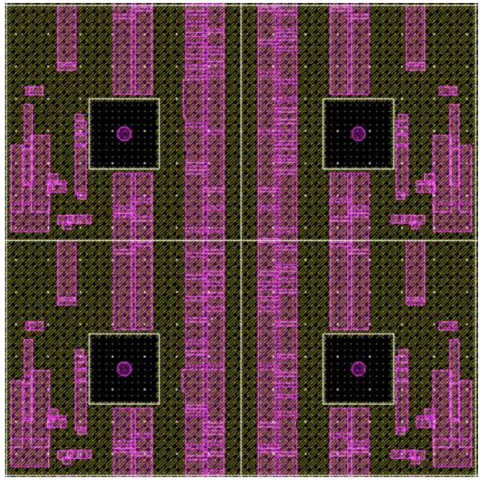
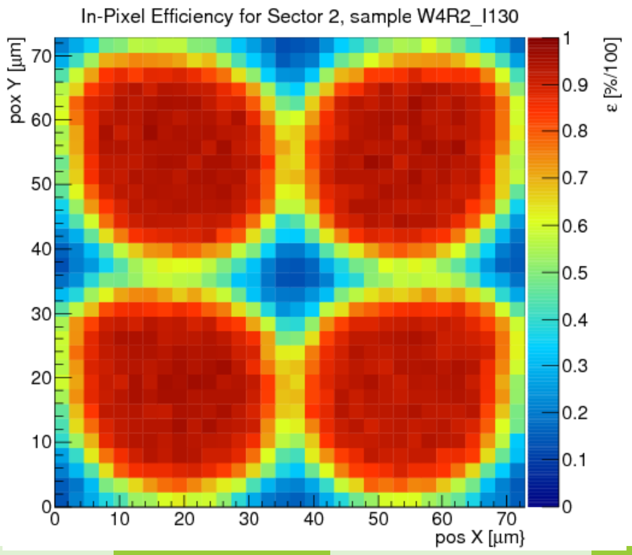
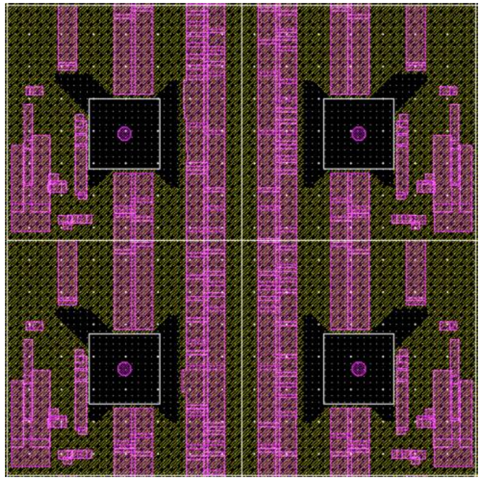
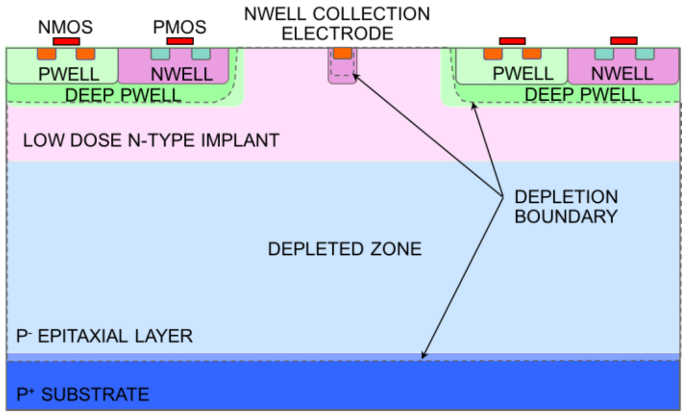
Efficiency vs. deep p-well coverage



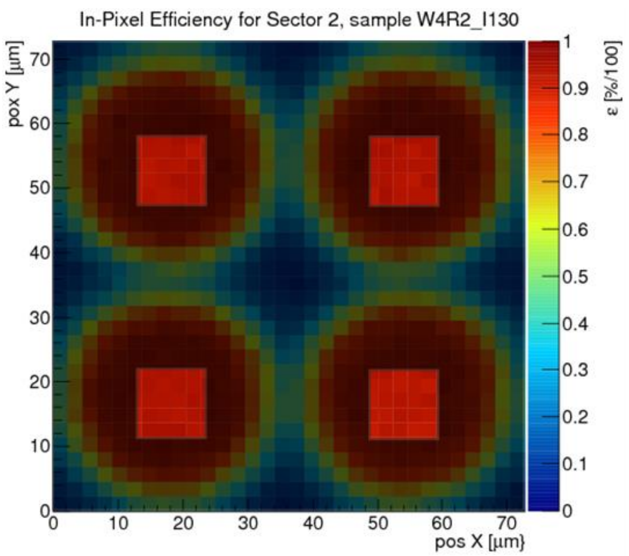


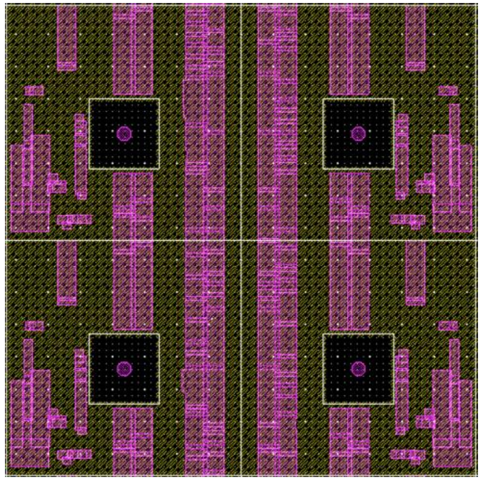


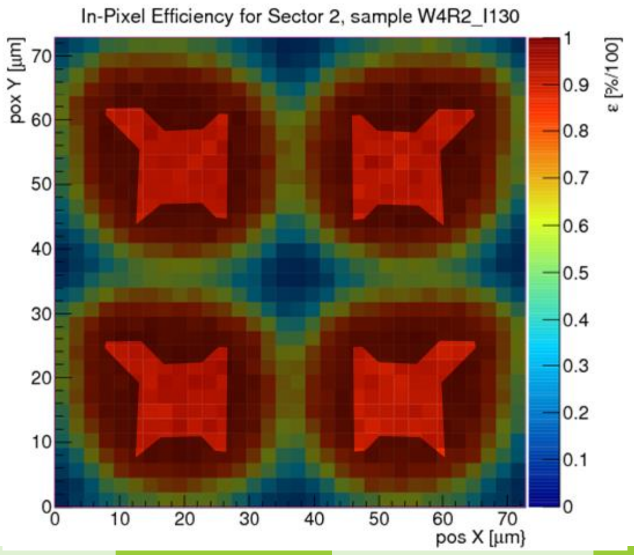


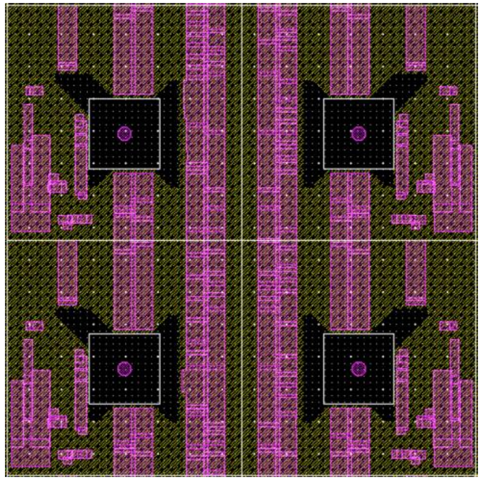


Efficiency vs. deep p-well coverage

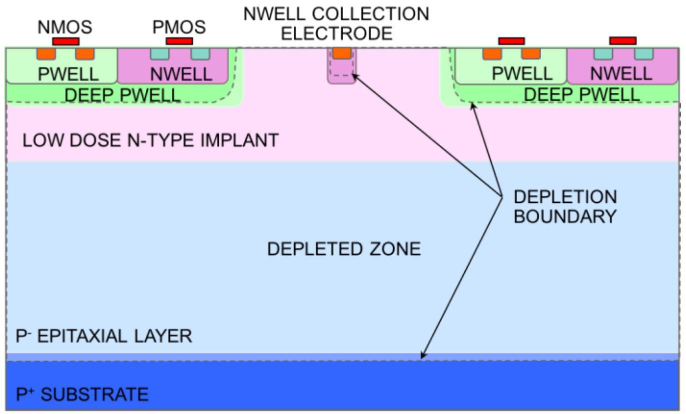








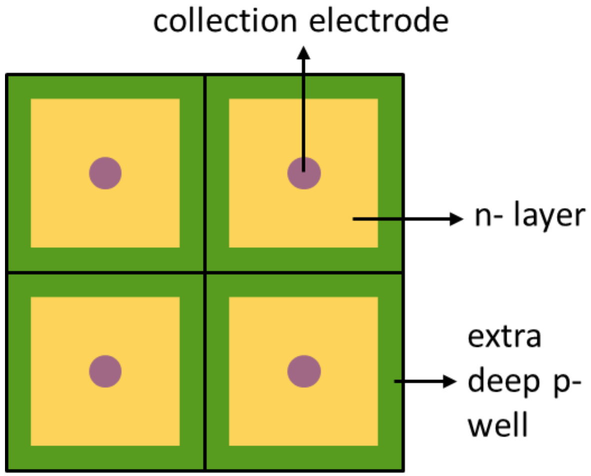
- Deep p-well only needed under n-wells of PMOS transistors
- In-pixel efficiency can be correlated to deep p-well coverage around the collection electrode
- Removed deep p-well results in higher overall efficiency due to higher lateral electric field



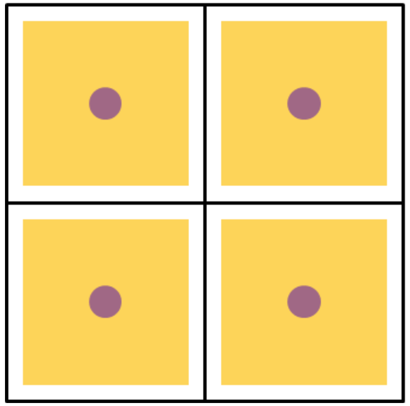
Pixel design improvements

Additional “extra-deep p-well” layer

- Already known by TowerJazz: no process R&D needed



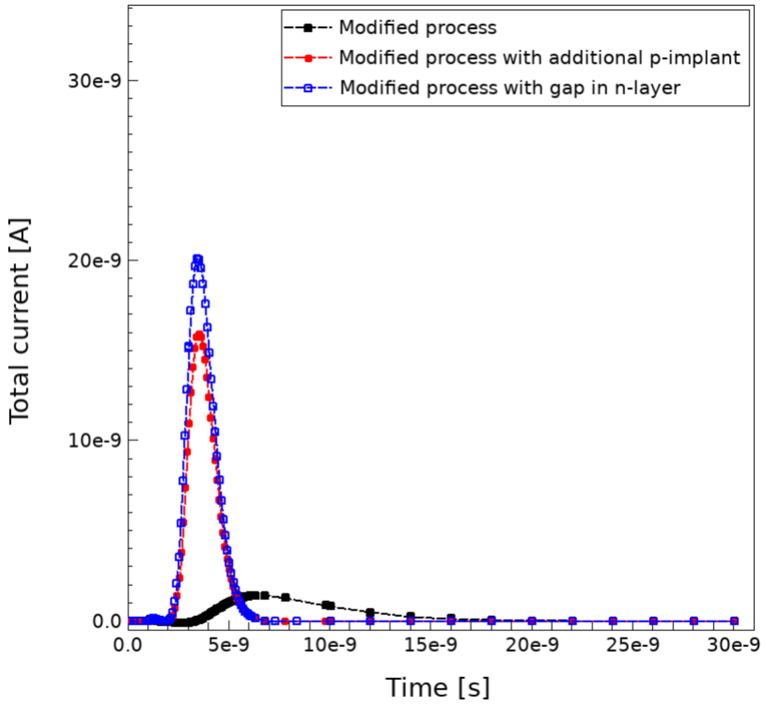
2x2 pixel layout



Gap in the n- layer

- requires only a change of the existing mask for the n-layer

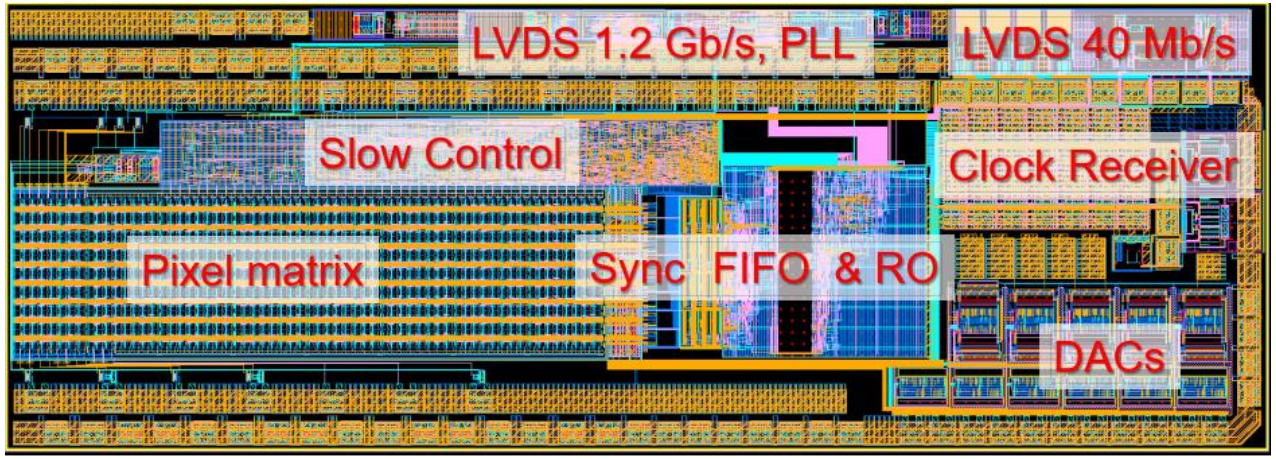
After irradiation simulated current pulse



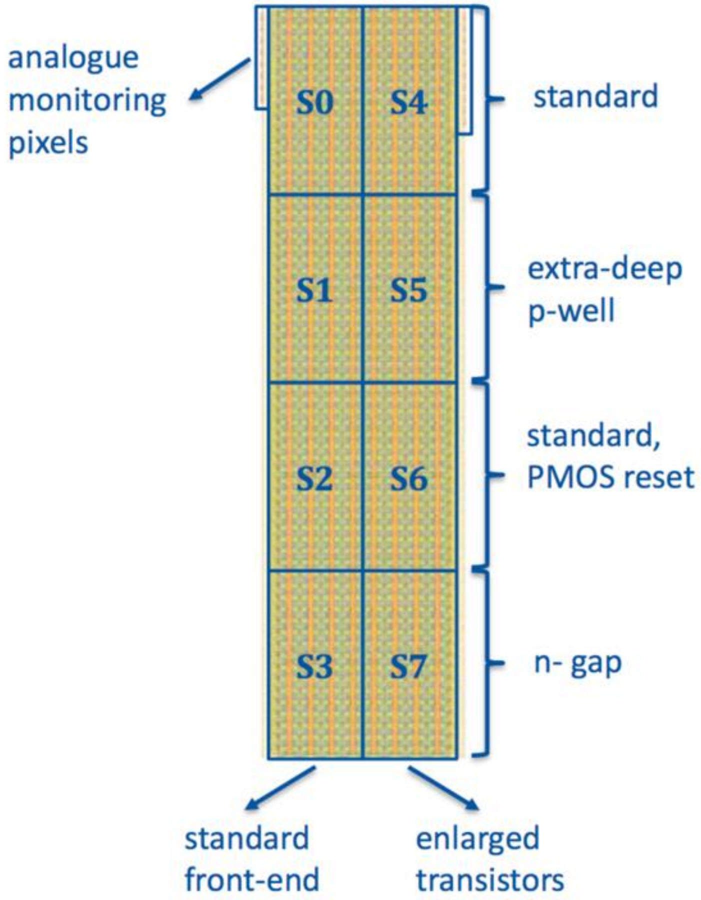
Magdalena Munker

Mini MALTA pixel matrix

- Pixel size: 36.4 µm x 36.4 µm
- 64x16 pixel matrix includes 8 sectors with splits on analogue front-end design, reset mechanism and process



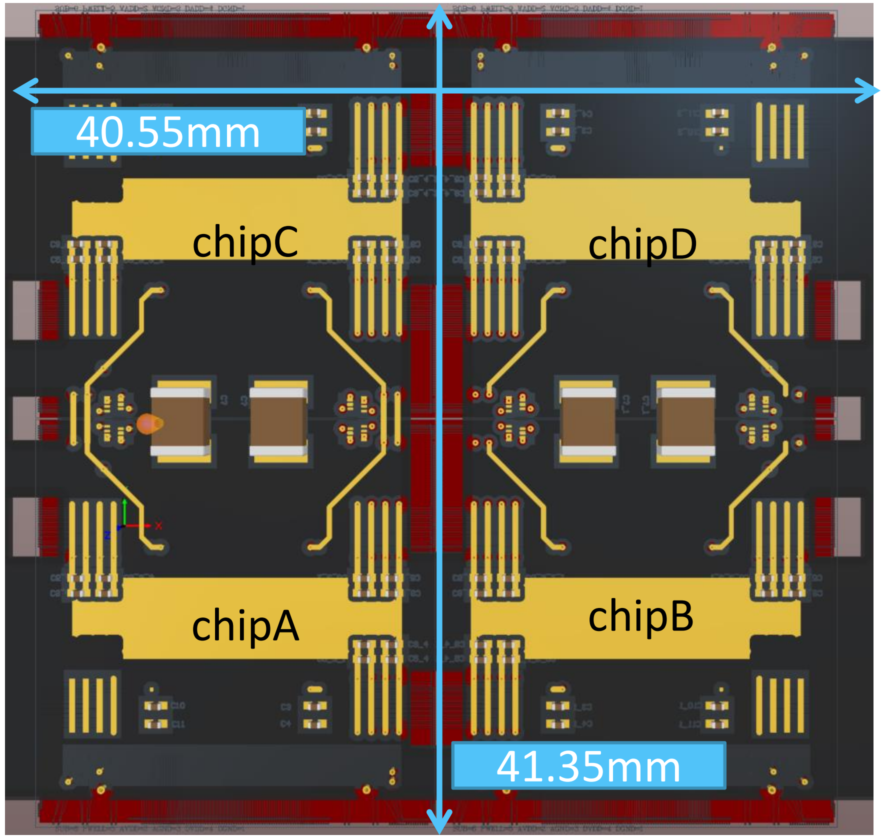
Mini MALTA with synchronization
and fixes for improved chargecollection



CMOS Quad-Module design

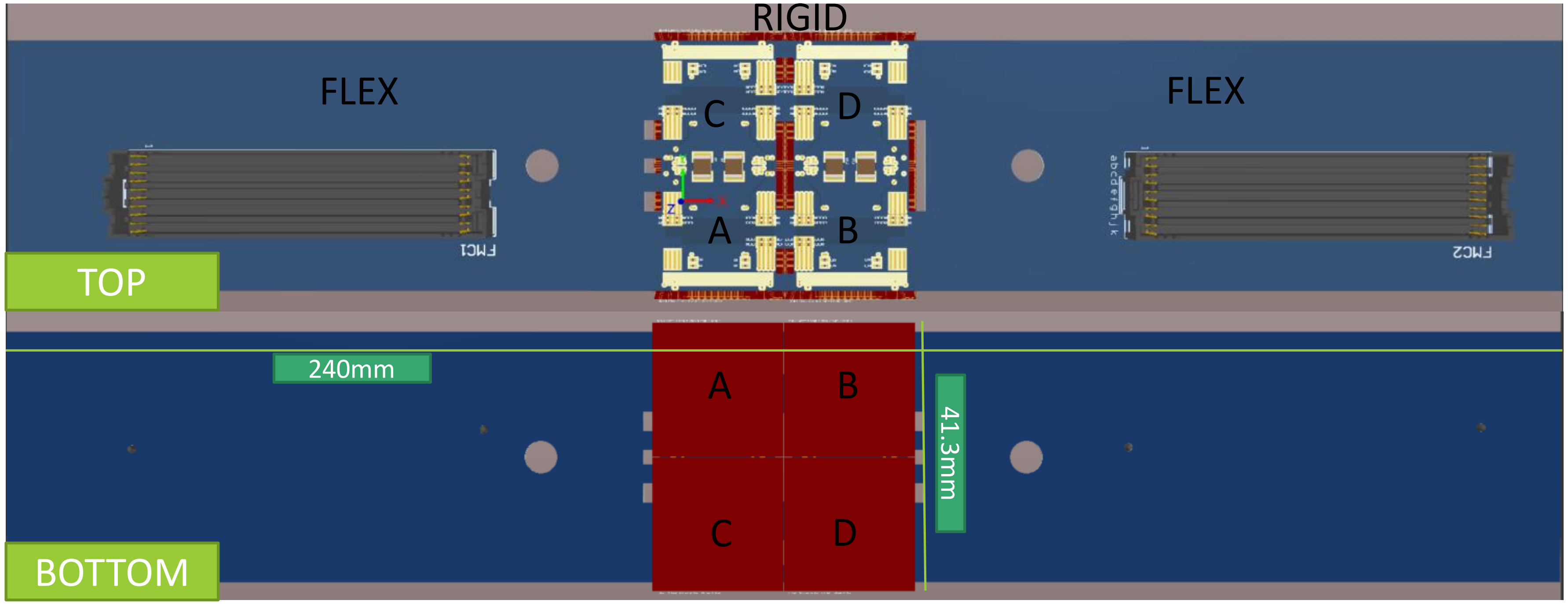
The ATLAS ITk sensors will be organized in quad modules.
In the case of the hybrid pixel, one sensor of around 4x4 cm^2 will be bonded to four 2x2 cm^2 front-end chips

MALTA is the first large scale monolithic chip that allow build a compatible Quad-Module, assembling four detectors in a single FLEX



Under design

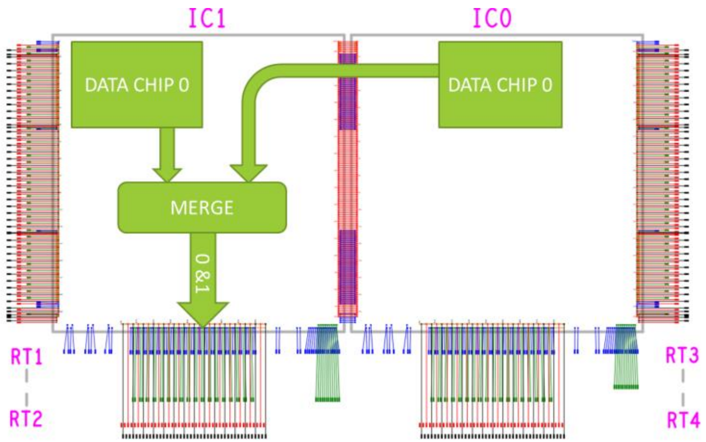
MALTA functional adaptor Card



- 2 FMC connectors: interface to VITEX 707 - compatibility with single chip MALTA readout.
  - Chip ABCD partial readout.
- Assembly holes for JIG. Compatible with Milano JIG.
- Holes for wirebonding.
- Two independent power connector on left and right side.
- Chip 0 and Chip123 can operate independently in parallel.

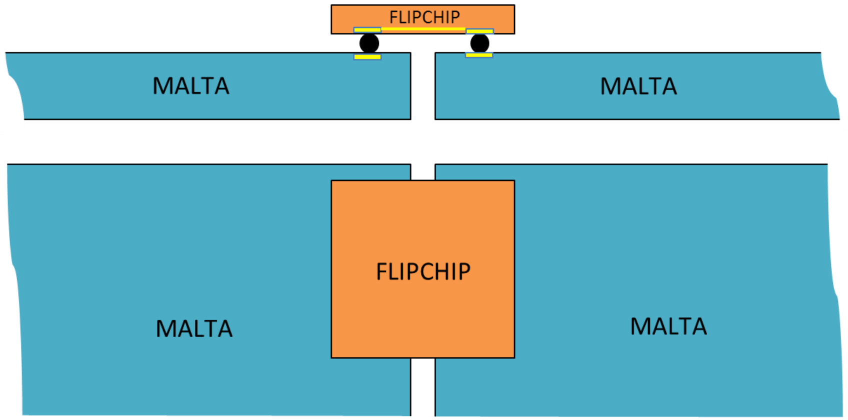
Parallel R&D on MALTA

Chip to Chip communication



MALTA can transmit power and data asynchronously to a neighboring chip (via CMOS pad), merging the data of multiple pixel matrix in just one parallel output

Flip chip connection

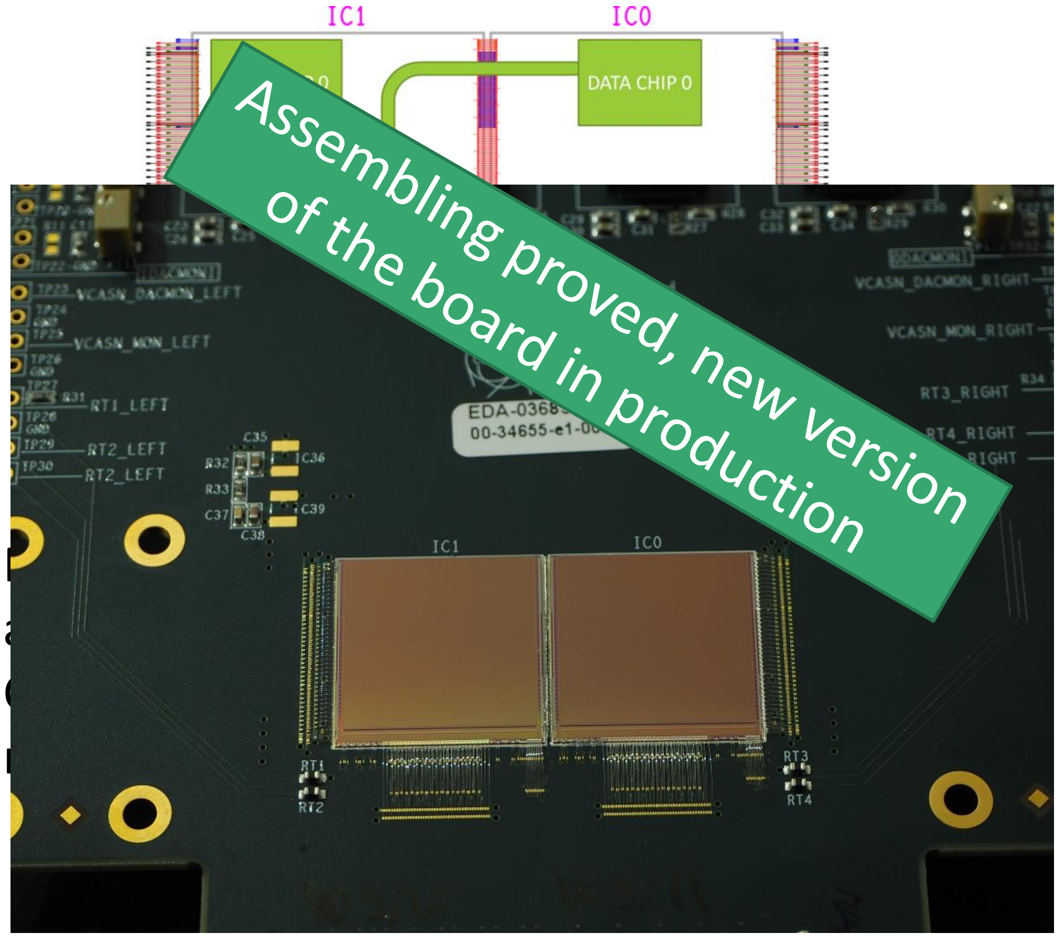


Connection between neighboring chips using flip chip

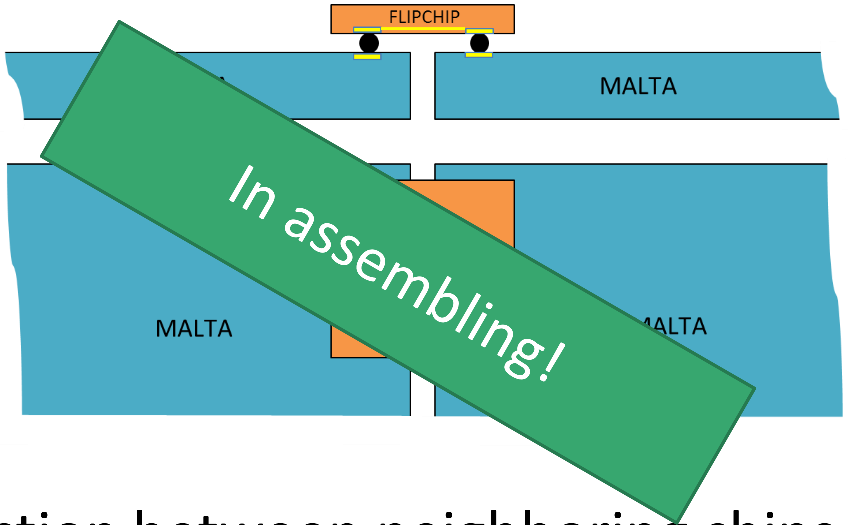
- Better for assembling
- Allow additional electronics in the flipchip

Parallel R&D on MALTA

Chip to Chip communication



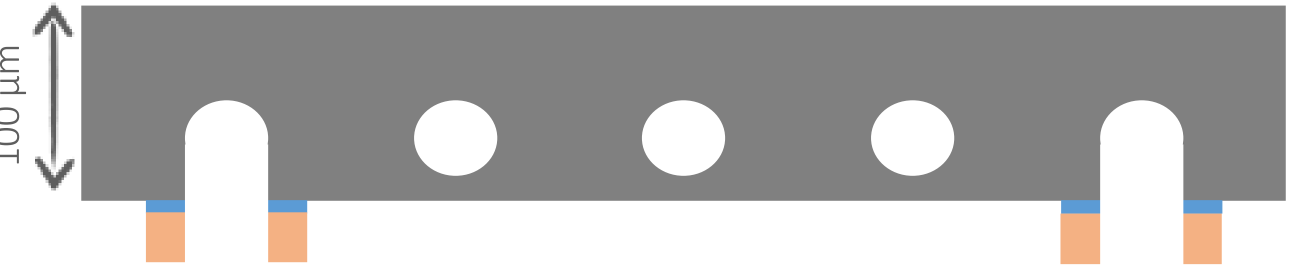
Flip chip connection

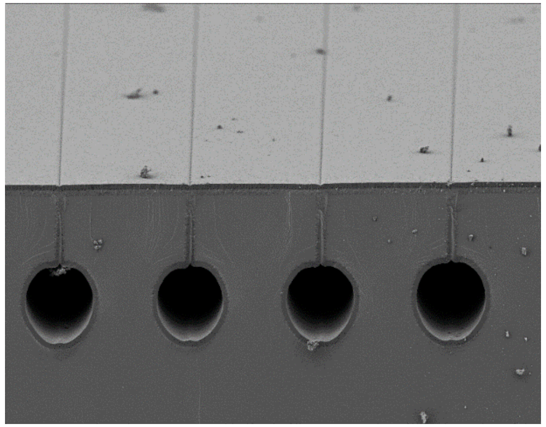


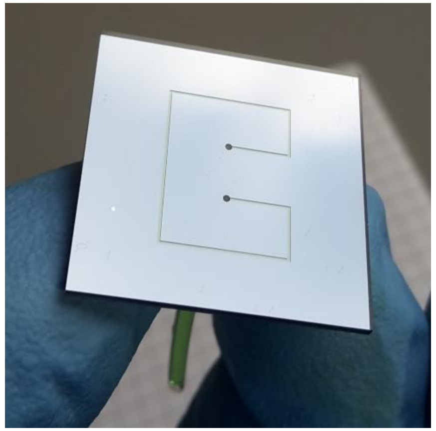
Connection between neighboring chips using flip chip

- Better for assembling
- Allow additional electronics in the flipchip

Microfabrition of channels







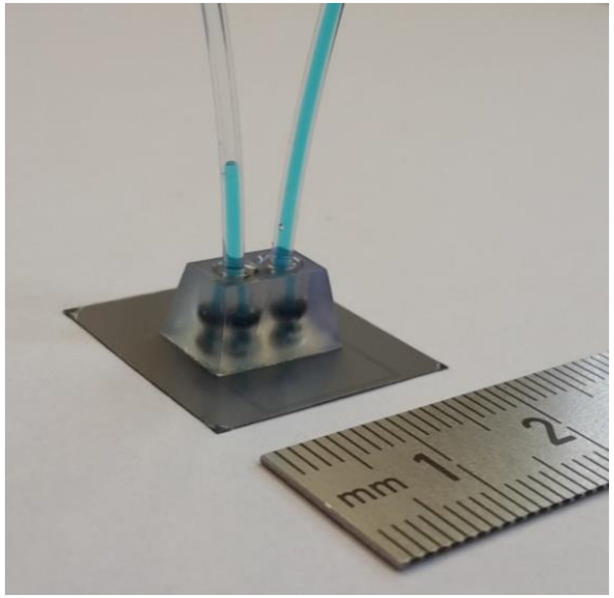
A CMOS-compatible microfabrication process was developed at CERN to embed microfluidics into silicon dies.

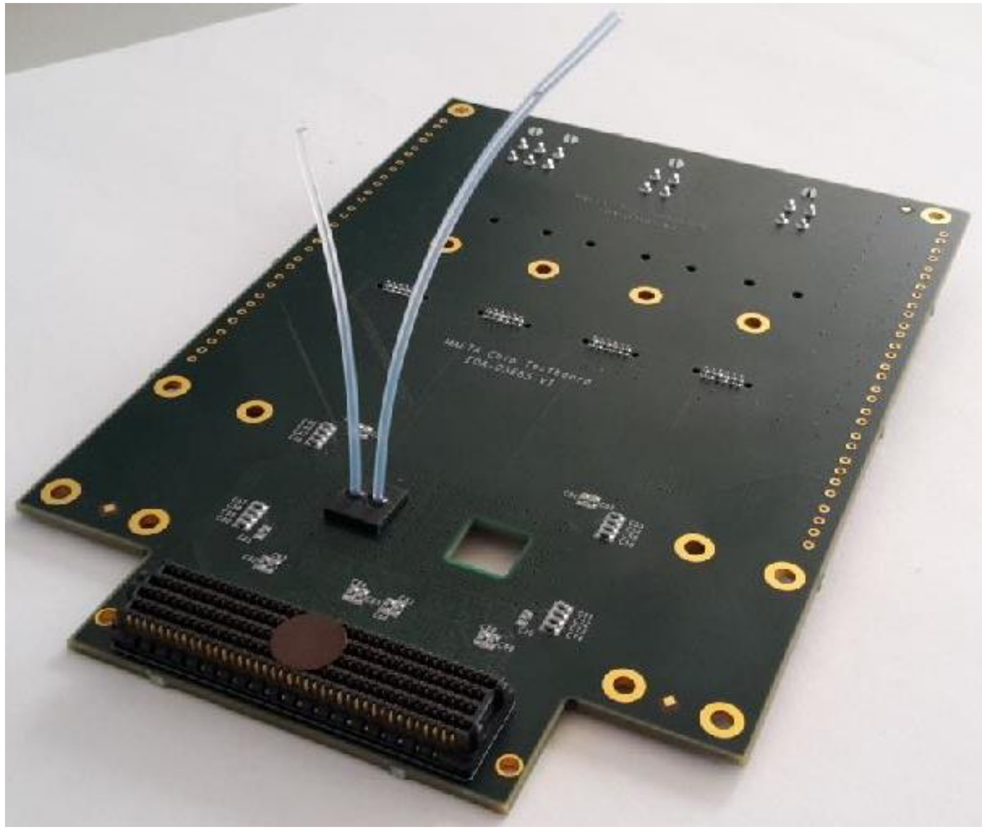
This process allows to fabricate cooling microchannels on the backside of monolithic pixel detectors.

A demonstrator is currently being produced by post-processing functional MALTA chips in the class 100 (ISO5) MEMS cleanrooms of EPFL.

Jacopo Bronuzzi, Riccardo Callegari, Roberto Cardella, Clémentine Lipp, Alessandro Mapelli, Petra Riedler

Embedding Microchannels into MALTA

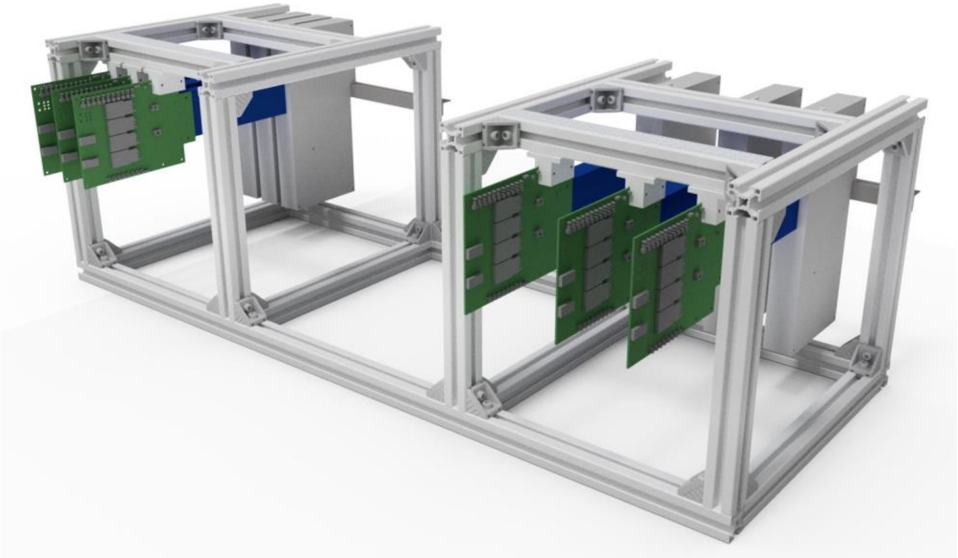


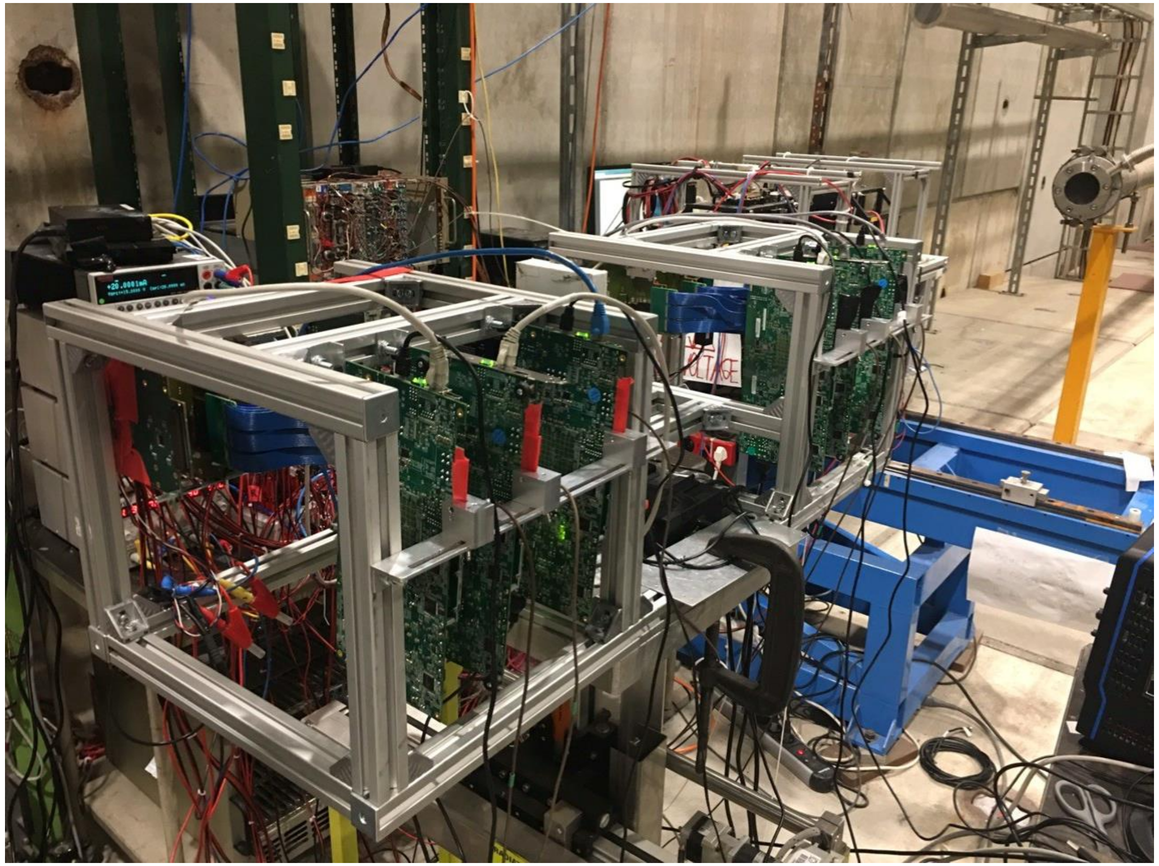


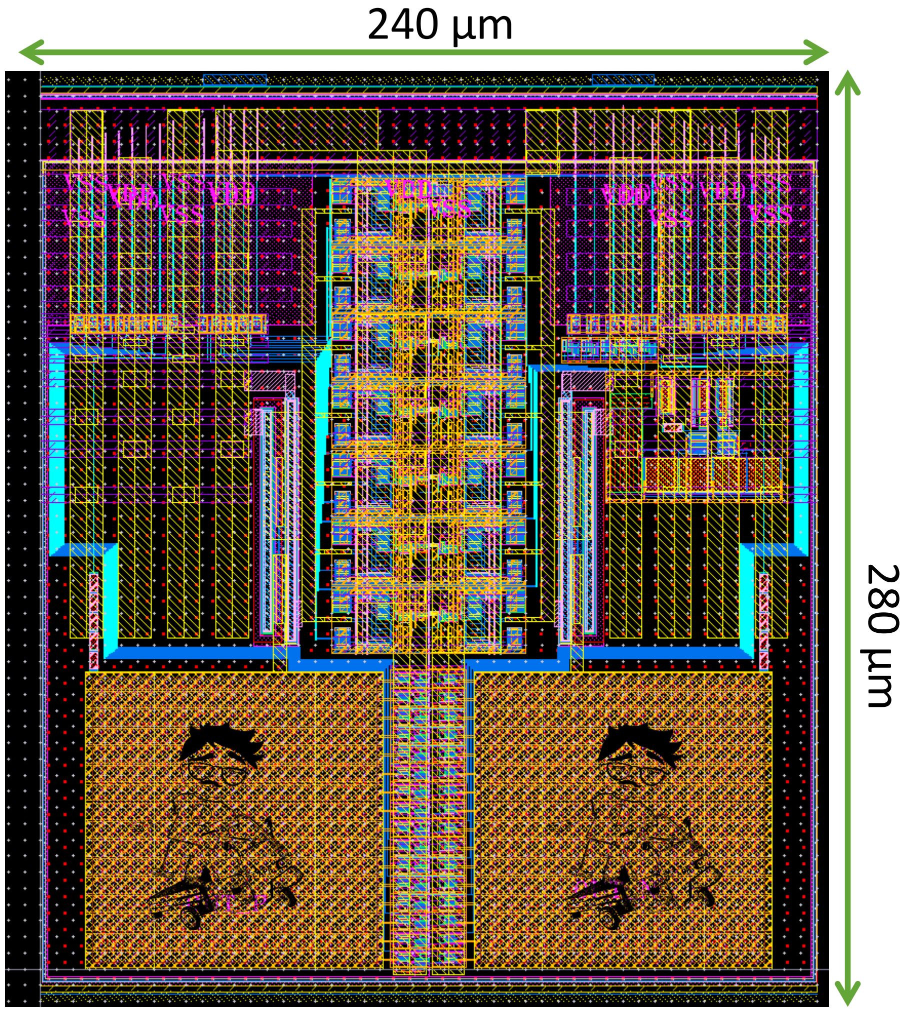
In the coming days a new batch of **4 MALTA chips will be equipped with microfluidic connectors and capillaries**. They will be inserted into a test read-out board and wire-bonded. A full electrical and thermal characterisation campaign will be pursued.

Malta Telescope

6 MALTA chip-based planes
2 Scintillators
4um resolution



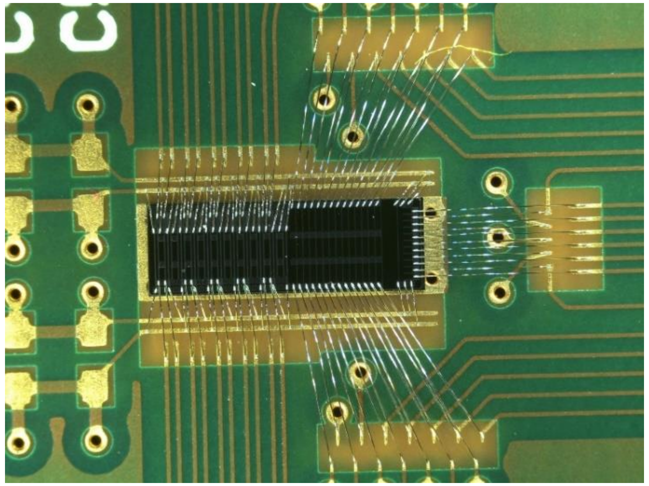




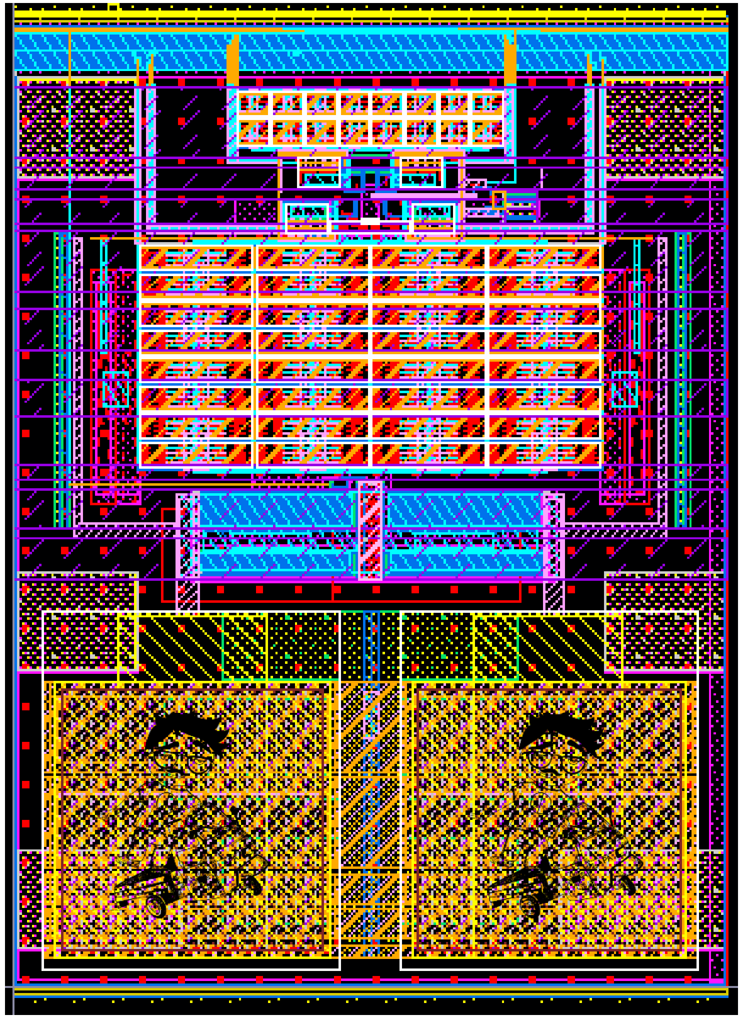
5Gb/s

- 280 X 240µm^2 (2 pad pixel pitch)
- Tunable DC current (7x 0.8mA)
- Modular capacitive coupled pre-emphasis: 16 blocks driving 25fF each.
- Vcm feedback control at 0.8V.
- External 100 Ω differential termination
- 40 drivers integrated in MALTA (up to 2Gb/s)

Dedicated testchip



LAPA Receiver



5Gb/s

- 320 X 240 {2 pad pixel pitch) μm^2
- Internal selectable 100 Ω termination resistor

SPEC	Min	Max	Tested
VCM	0.7 V	1 V	0.75 V
Vdiff	0.3 V	-	0.4 V
Term Res	-	-	100 Ω
Bit rate	-	-	5 Gbit/s

Power	Current [mA]	Power [mW]	Input
Static	2.69	4.84 V	-
Dynamic	-	0.44	5 Gb/s
Total	-	5.28	5 Gb/s
Bias Static	0.94	1.7 V	-
RX+Bias	-	6.98	5 Gb/s

LAPA eye diagram measurement

5Gb/s

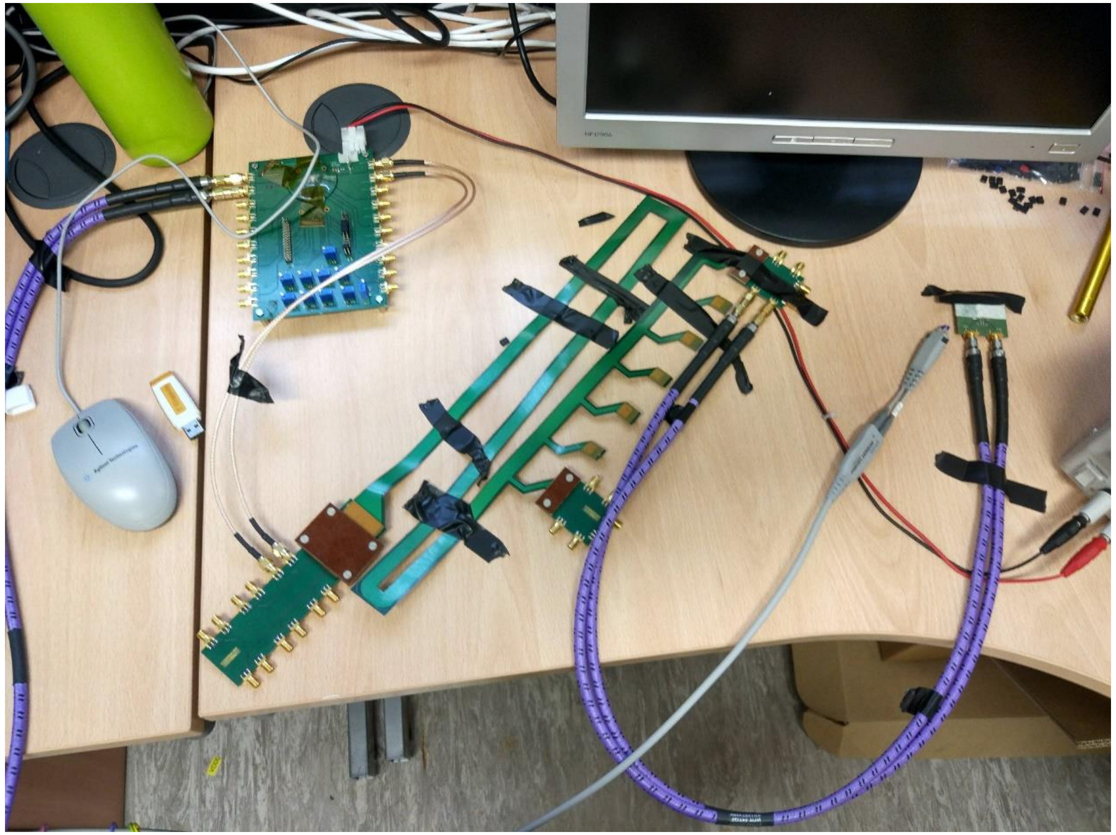
1.28Gb/s (ITk specification)

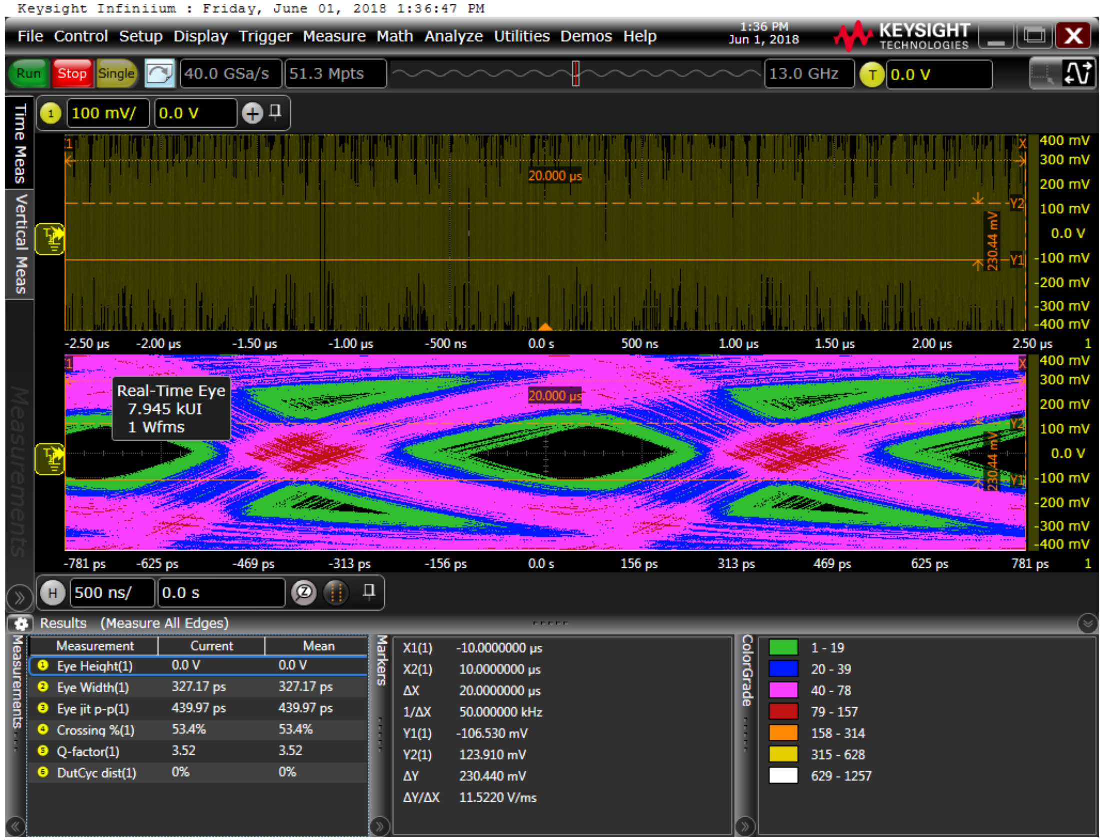
Jitter$_{p-p}$= 71ps

Jitter$_{p-p}$= 38ps

LAPA @1.28 Gbit/s on FLEX ITk prototype

Flex for data transmission out of the ITk system (length~5m)





New LAPA carrier with termination on board in production

Conclusions

The MALTA CMOS pixel sensor was developed in view of the ATLAS High-Luminosity upgrade.

The chip has been extensively characterised in lab measurements and testbeam, and shows promising results in terms of front-end performance and readout capability, but needs further improvement:

The small collection electrode sensor suffers from degraded efficiency in the pixel corners after irradiation to 10^{15}neq/cm^2, and this is being addressed by means of improvements in in the process.

The fixies have been implemented in a new prototype matrix called MiniMALTA

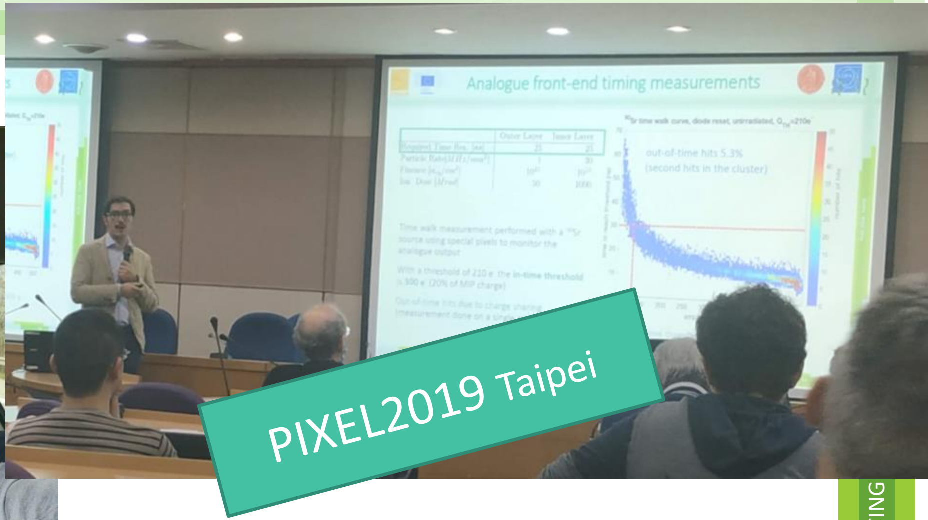
The LAPA LVDS driver and receiver have been characterized up to 5Ghz, confirming the design specification.

Several R&D on monolithic pixel sensors are in progress using the MALTA chip, such as buried channels cooling and chip to chip data communication.

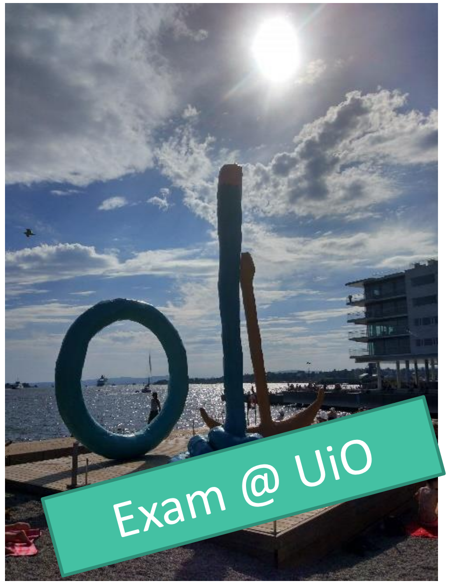
My Year


Guiding in ATLAS cavern


ELSA- TESTBEAM

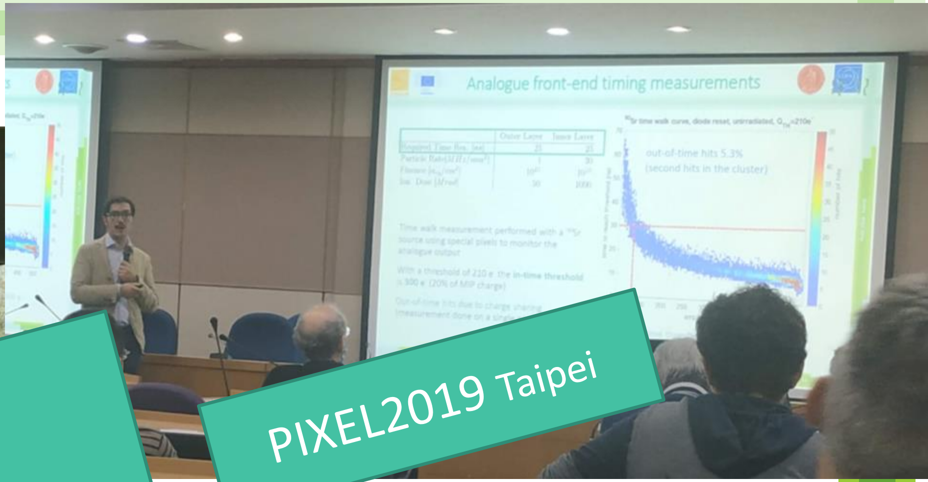

Analogue front-end timing measurements
PIXEL2019 Taipei


University of Glasgow


Exam @ UiO

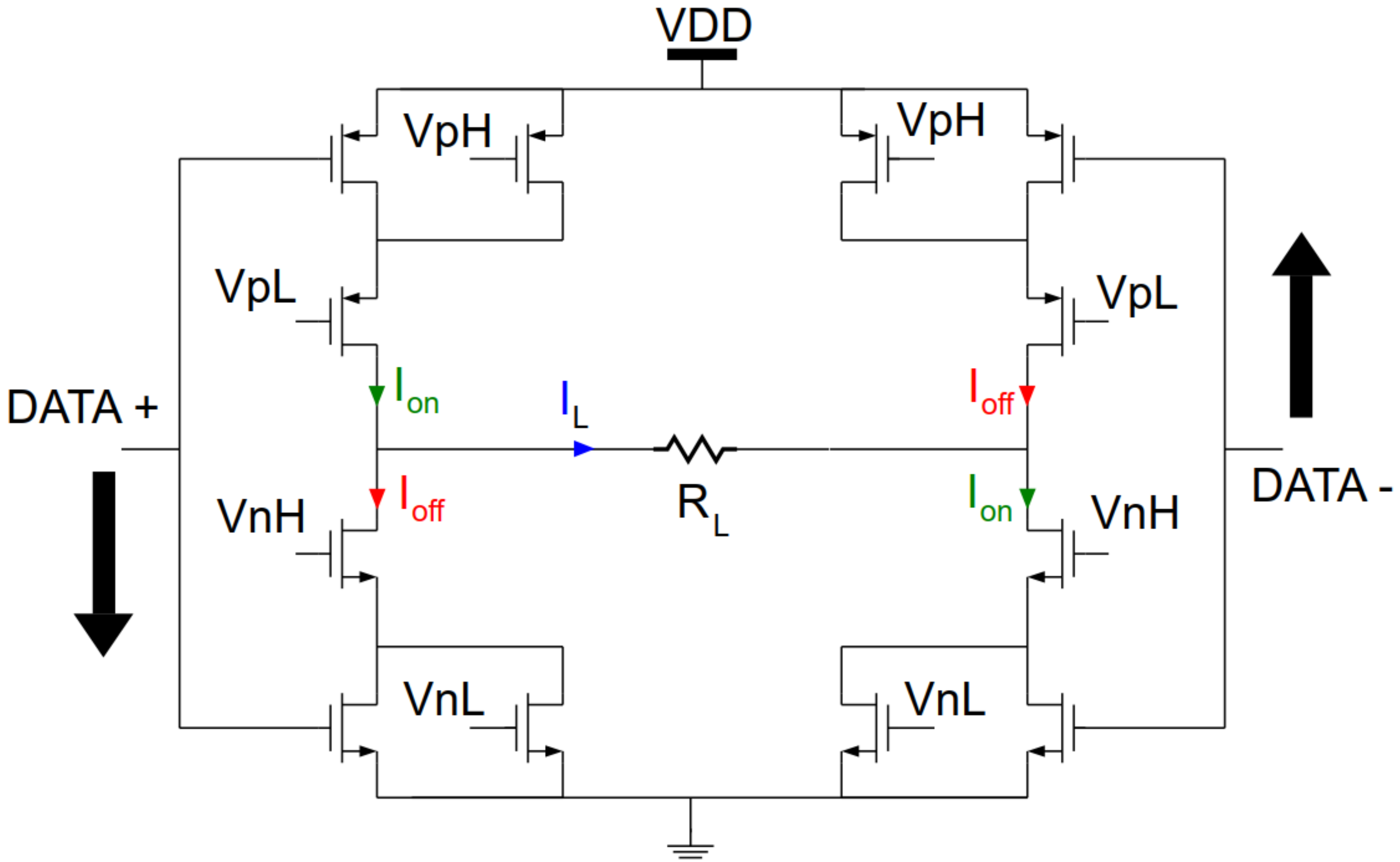

IMEC - COURSE

My Year



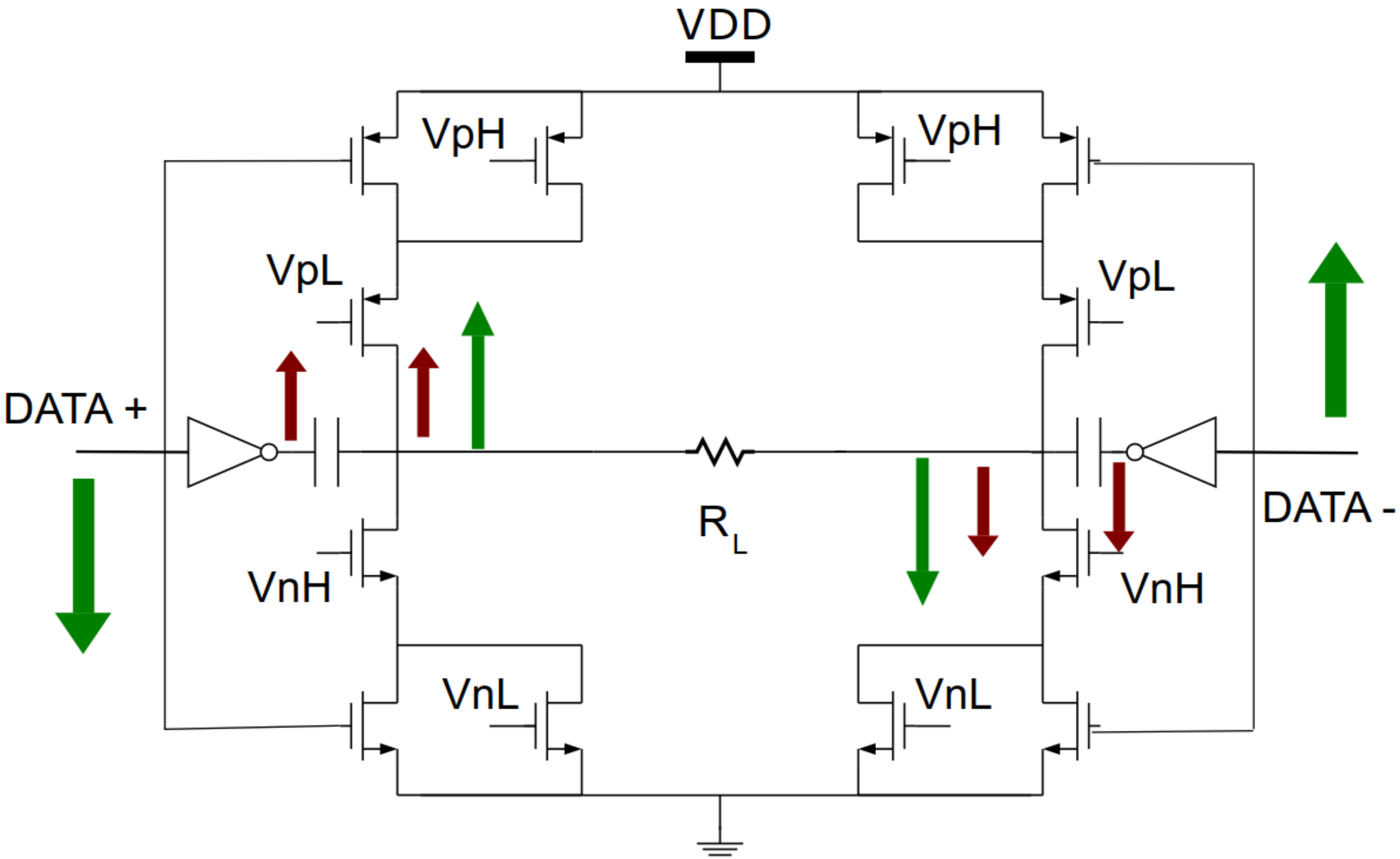
Thank you for the attention

LAPA H-BRIDGE



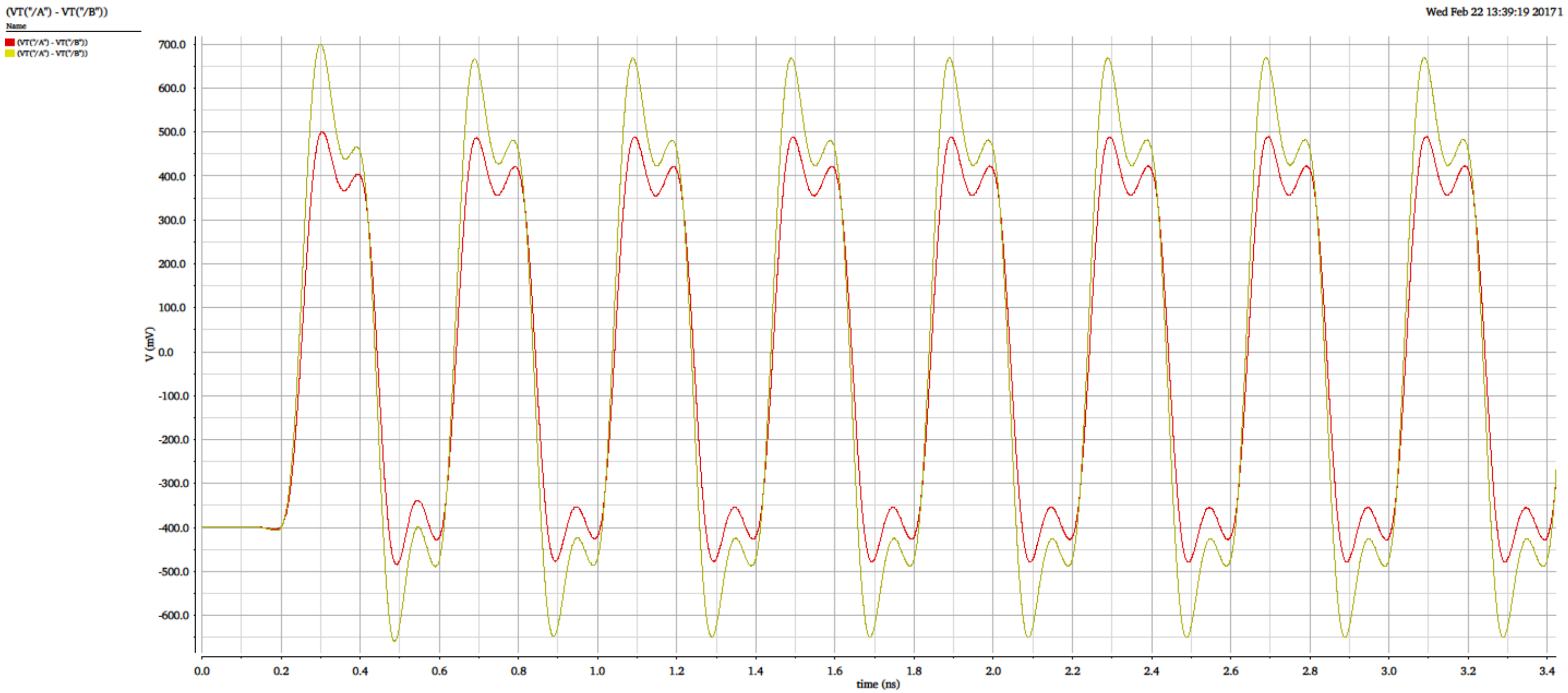
7 HBRIDGE blocks of 0.8mA - max: total 6mA

LAPA-PRE-EMPHASIS



16 BLOCKS driving 25fF coupled with the output pad

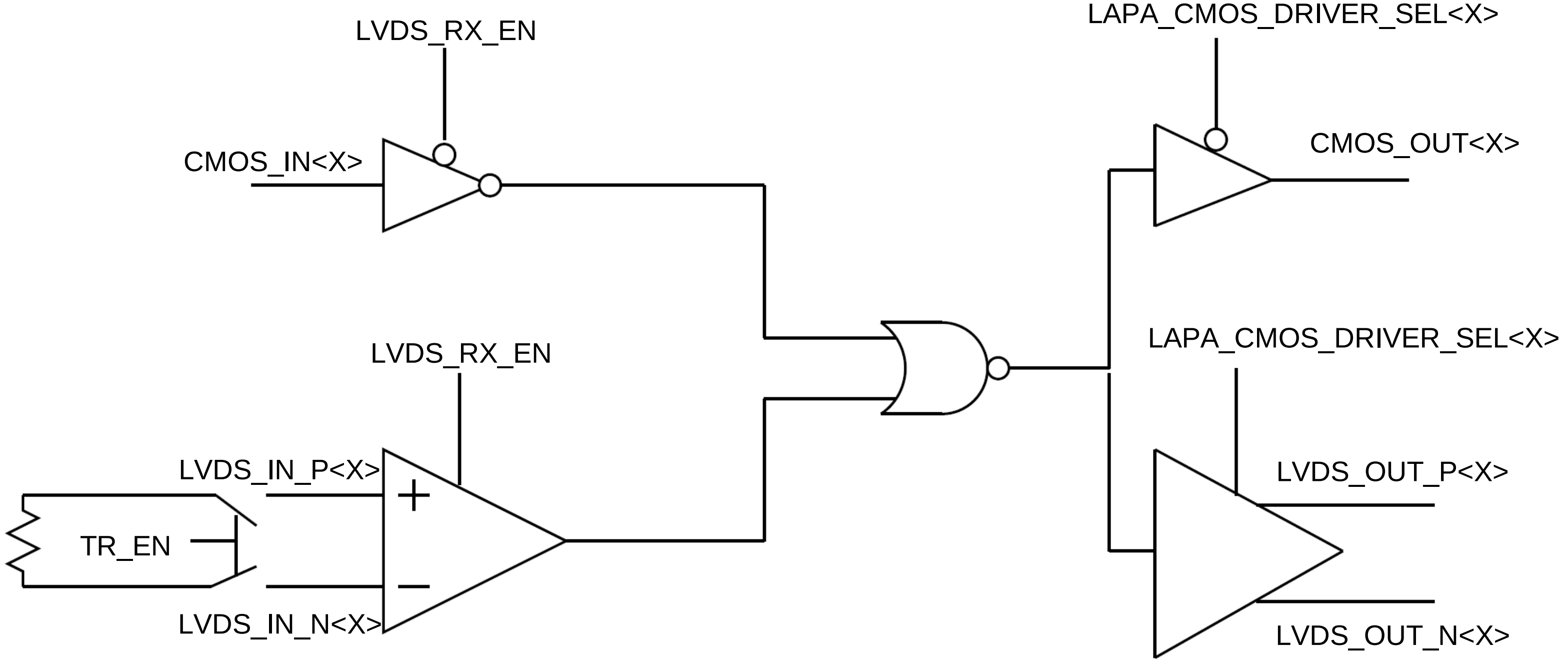
Pre Emphasis Simulations



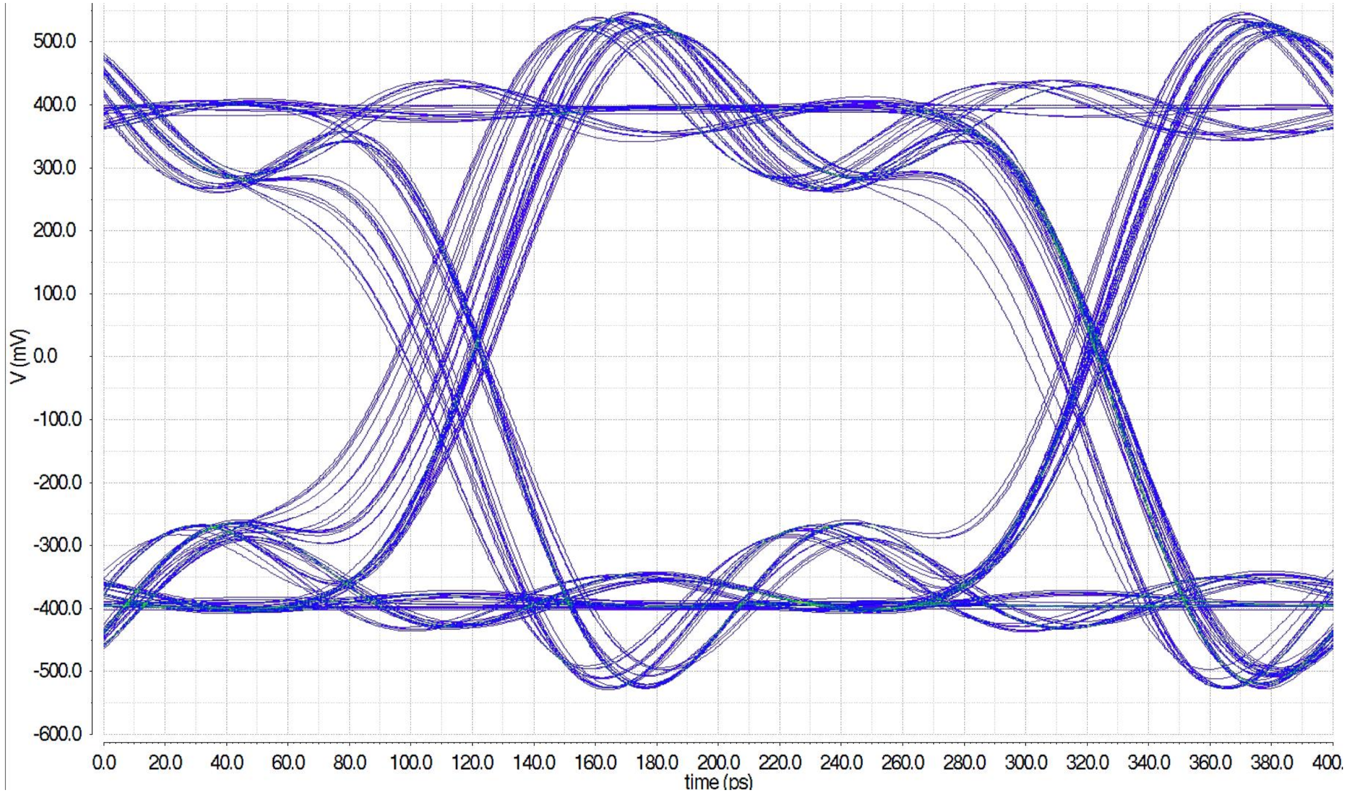
PRE ♯	PwSH $[mW]$	PwDig $[mW]$	PwToT $[mW]$
8	7.2	18.6	26.8
16(max)	7.2	25.4	33.6

Simulations of the LVDS OUTPUT

LAPA Single Channel Schema



LAPA TESTCHIP SIMULATION



2.5GHz LVDS IN – LVDS OUT. 100Ω termination. 1pF load.

Simulated jitter=45ps

Preliminary power consumption

Expected static power consumption

Static	Current [mA]	Power [mW]
5 Hbridge	4	7.2
7 Hbridge	5.2	10

Measurements on test chip

Static+Dynamic 1.28Gb/s	Current [mA]	Power [mW]
5 Hbridge	6	10.8
7 Hbridge	8	14.4

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