Bias circuit and FE design for small electrode monolithic sensors

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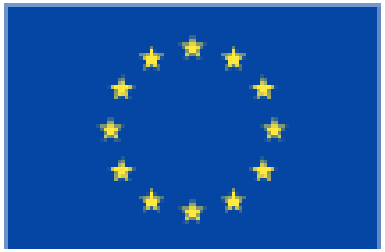


OUTLINE

- **TowerJazz 180nm technology**
- **Malta Powering scheme**
- **New DAC concept**
- **DACs implementations**
  - Voltage DAC
  - Current DAC
- **FE simulations**
  - Threshold dispersion and ENC
- **Training and courses**

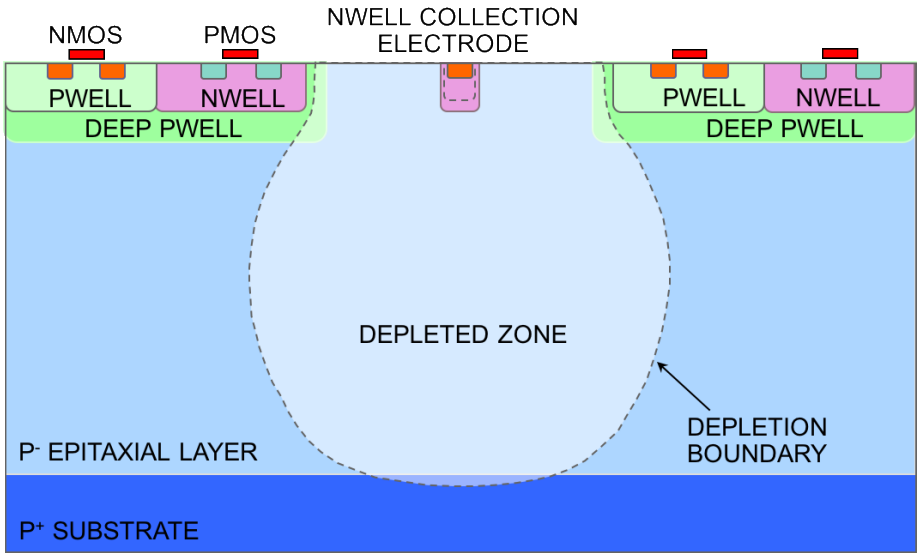
Sensor in the TowerJazz 180nm technology

STANDARD PROCESS

Small collection electrode design with high resistivity (> 1 kΩ cm) p-type epitaxial layer (25 µm → MIP ~1500 e^-)

Deep p-well shielding n-well to allow **full CMOS**

Reverse bias (~6 V): reduce input capacitance and increase depletion volume

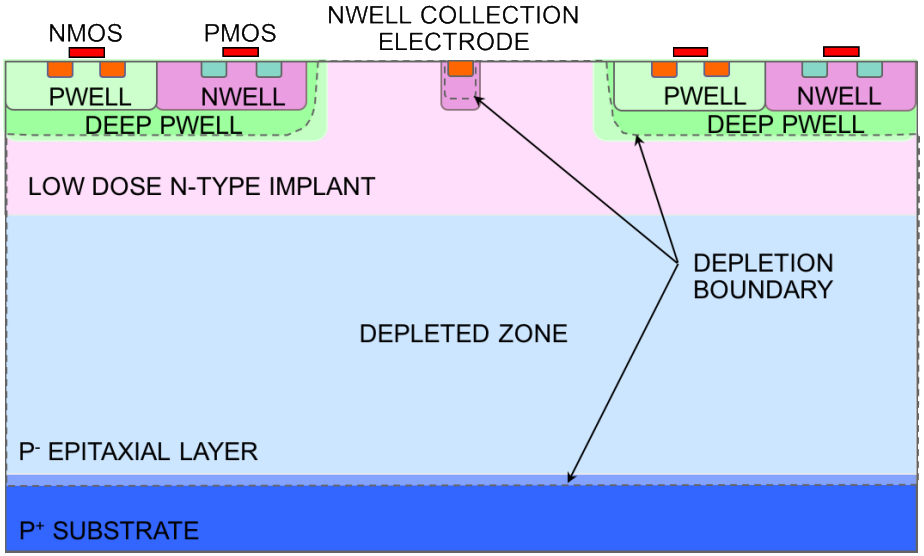


MODIFIED PROCESS

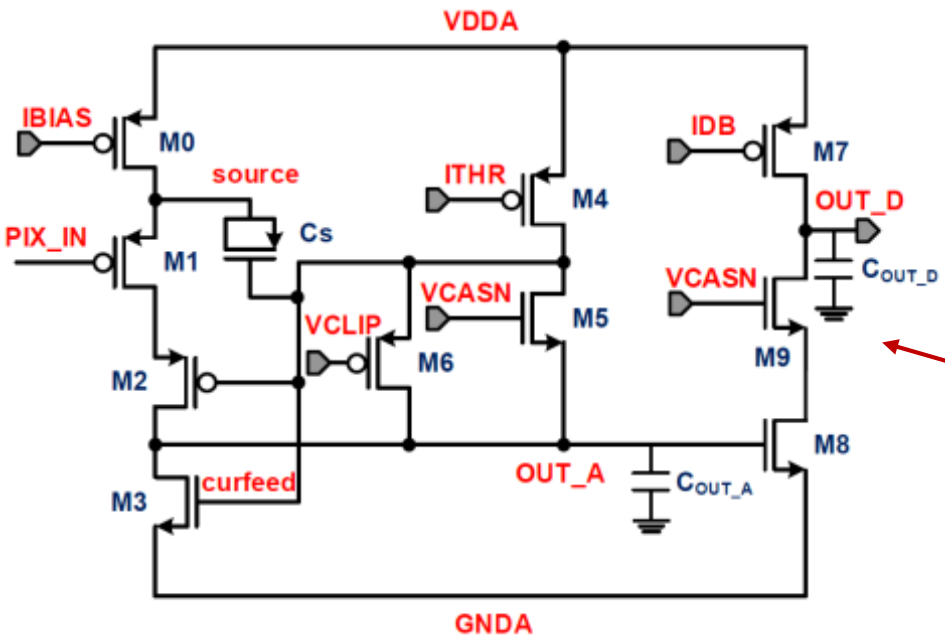
Adding a **planar n-type layer** to improve depletion under the deep p-well near the pixel edges

A fully depleted epitaxial layer results in faster charge collection and **better radiation tolerance**

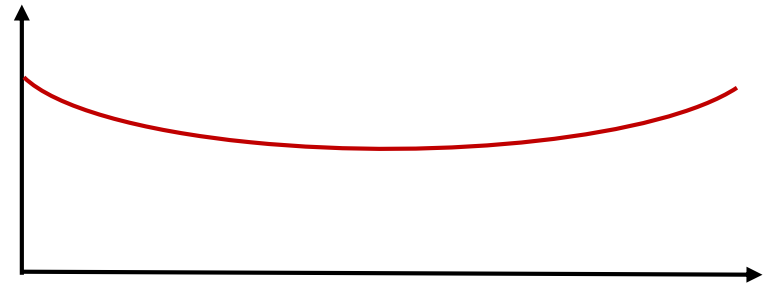
No circuit or layout changes required

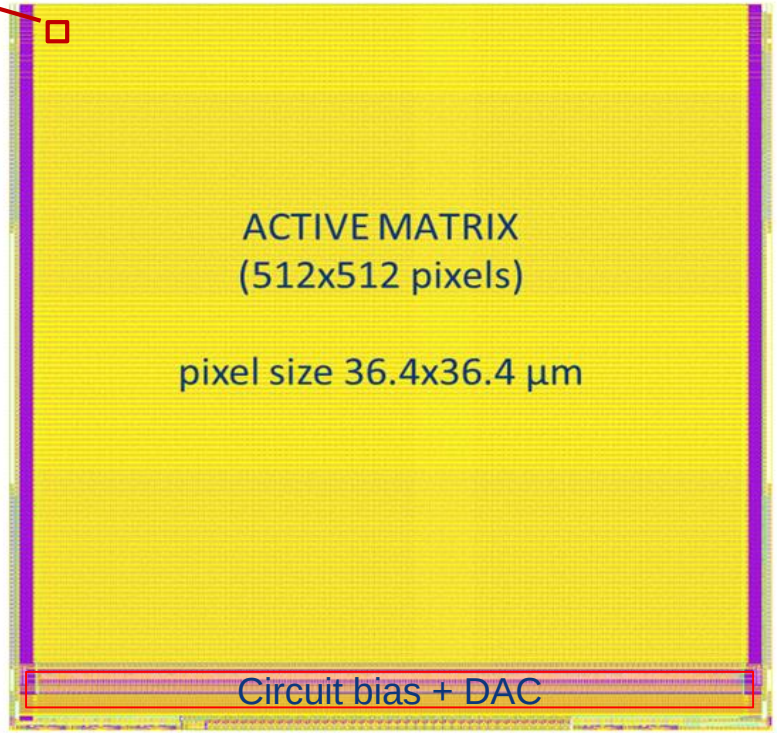


MALTA Powering scheme



VDDA voltage drop



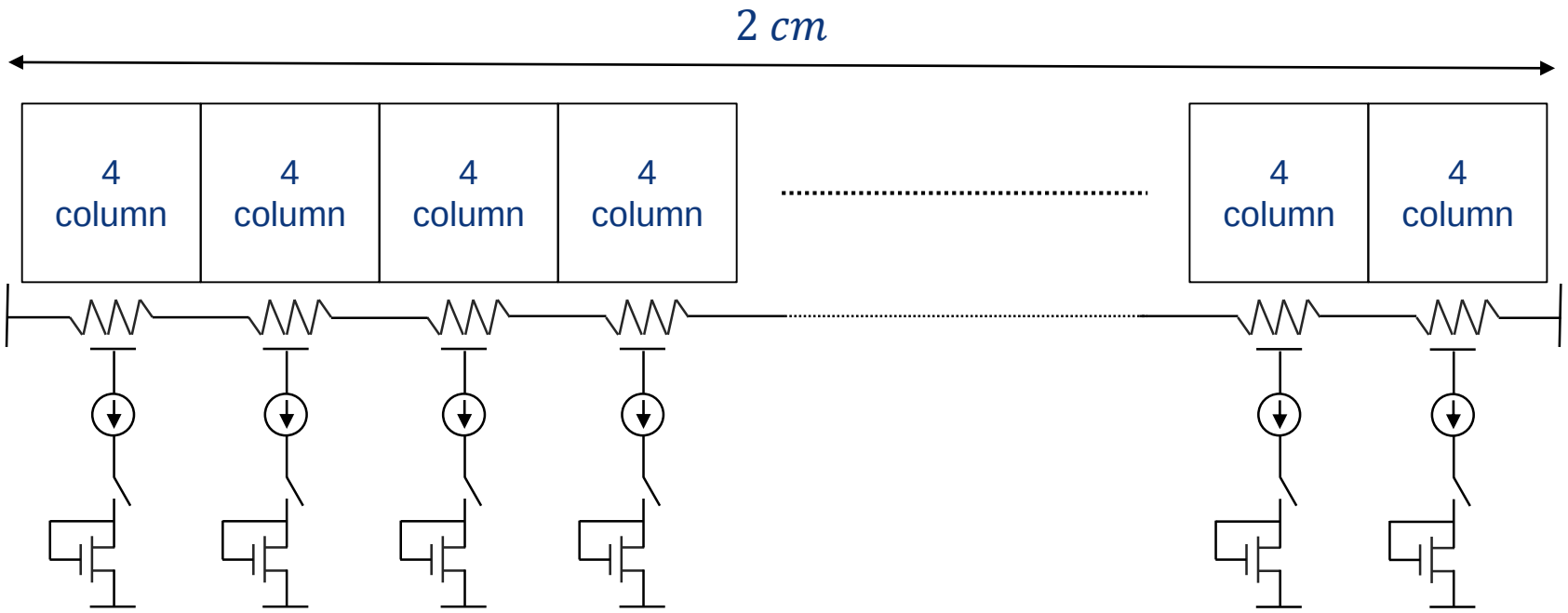


Supply voltage provided from the left and right sides

Front-End current ~ $0.5\ \mu A$

Large voltage drop on the supply in the middle of the matrix (10 ~ 20 mV)

MALTA DACs concept



Modular design:

- Current and voltage DACs distributed at the bottom of the column

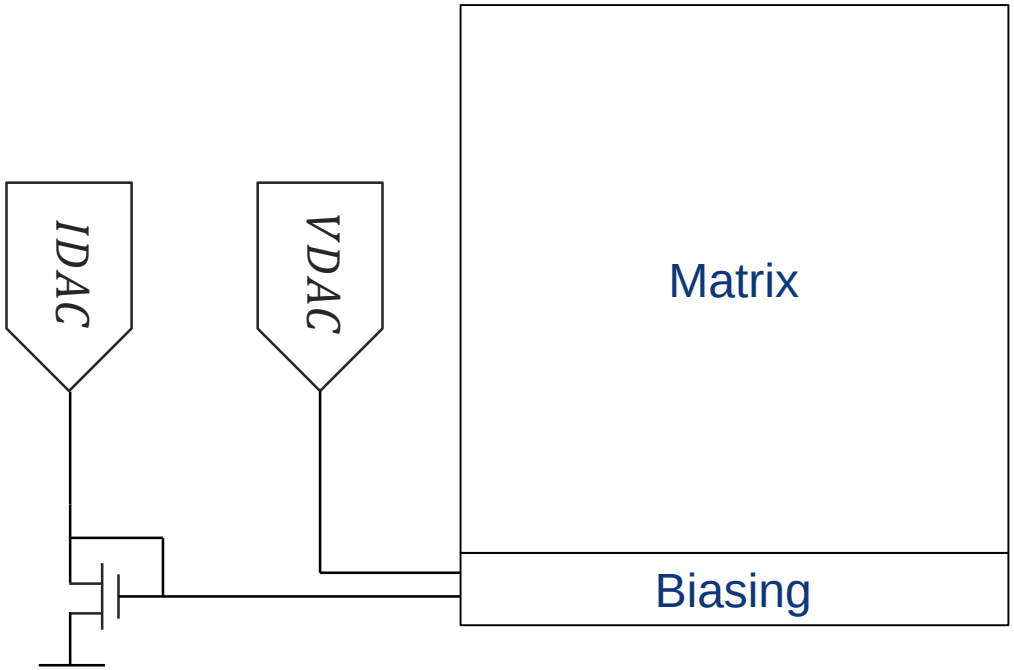
-Number of bits depends on Matrix width

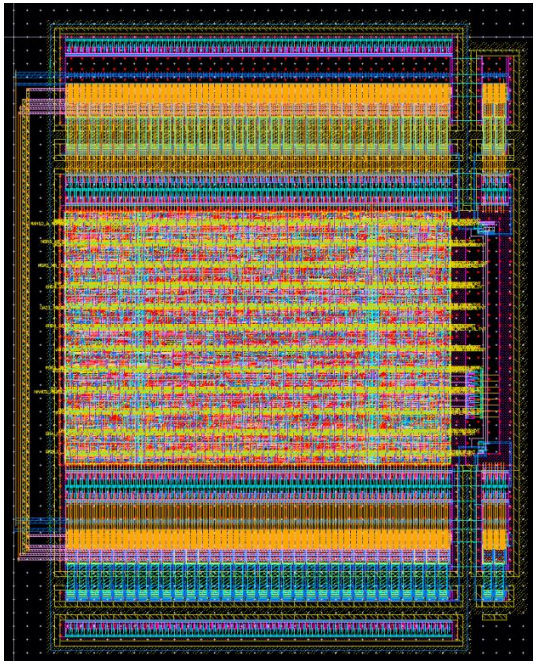
1 unit every 4 columns

512 columns / 4 = 128 => 2^7 => 7 bit

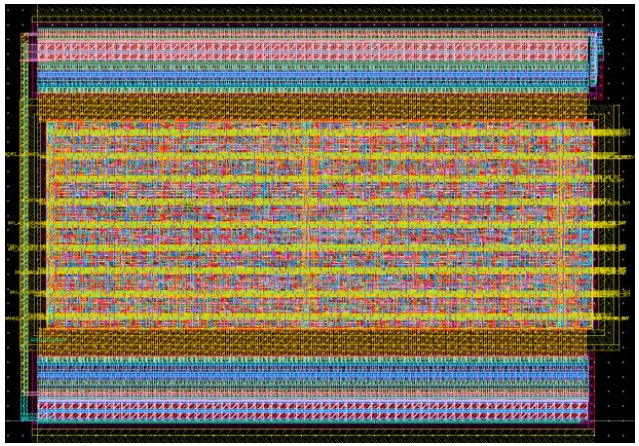
- Not flexible layout to increase DAC resolution or number of DACs

MiniMALTA DACs concept

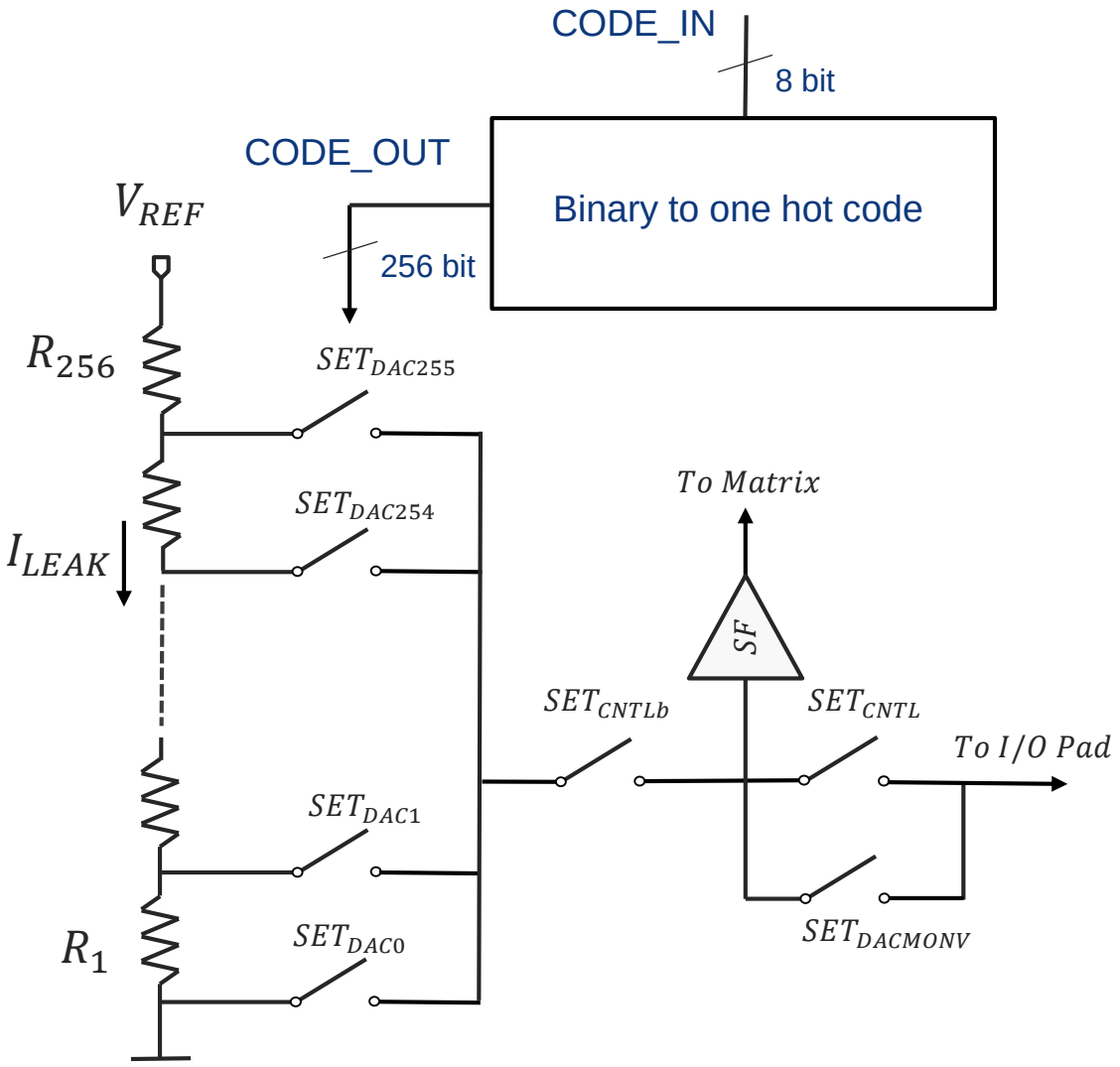




Non Modular design:
- Local DACs implemented to save space ($\sim 5\ x$)
-Number of bits independent from the Matrix width (8 bits DACs implemented)
-Easy to increase the number of DACs and biasing lines towards the FE
-Flexible layout



Voltage DAC – Implementation



Resistor string

One Hot Encoding

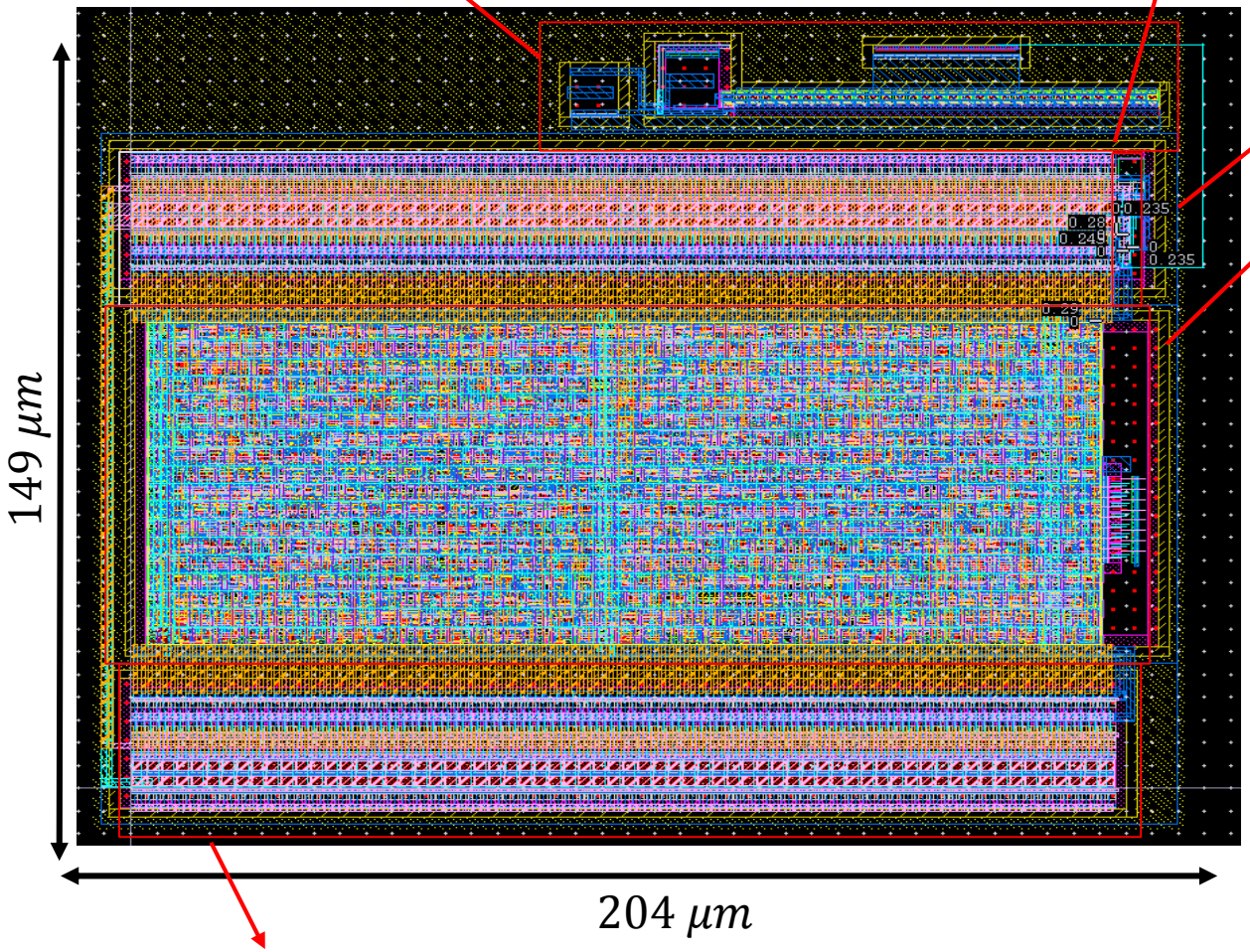
8 $bits$ resolution (0 ~ 1.8 V)
$LSB \approx 7.03mV$

One resistor for each DAC to guarantee a better modularity.

Possibility to override and monitoring the DACs.

VDACs outputs buffered to cope with the leakage current in the pixels.

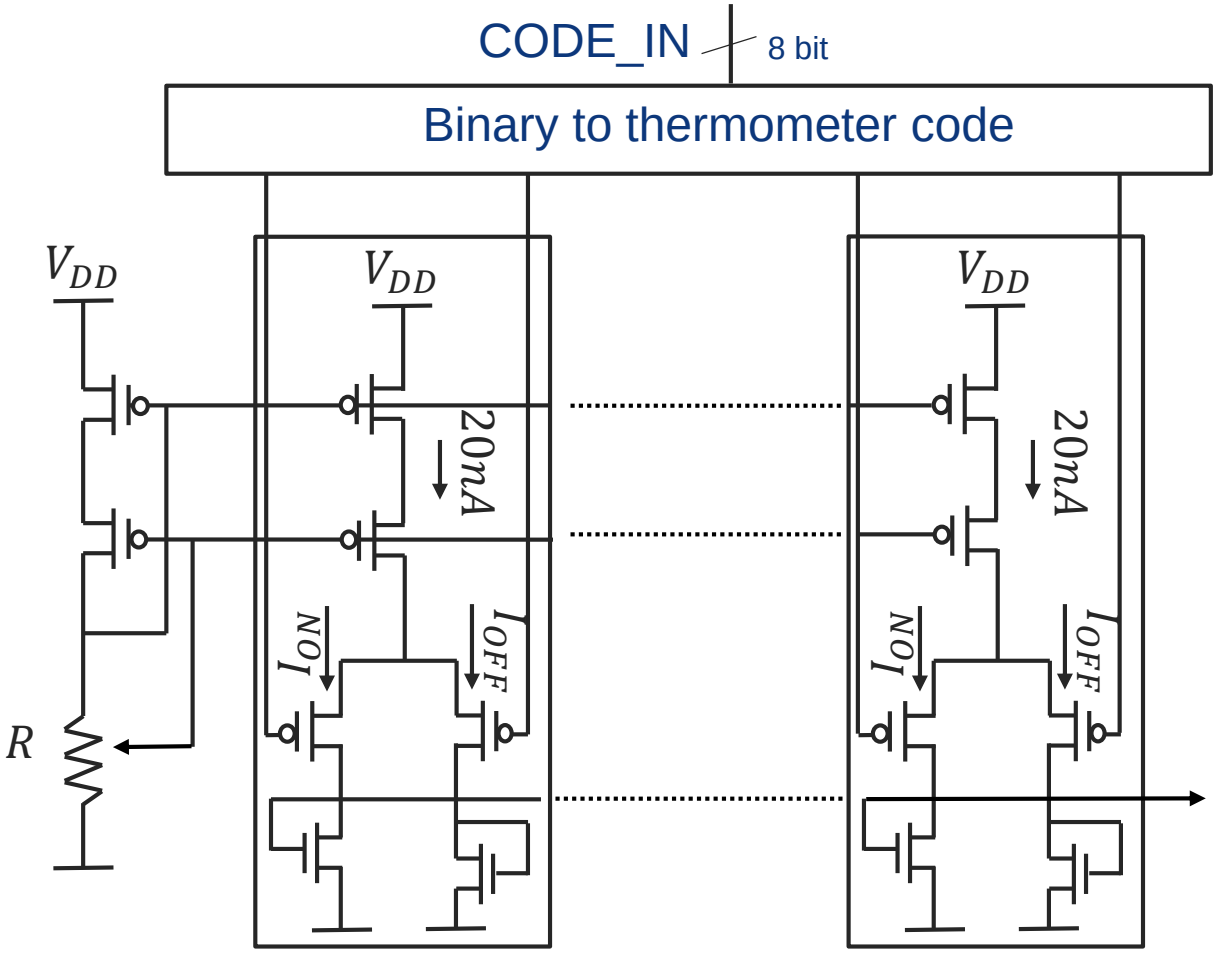
Voltage DAC – Structure layout



SPECIFICATION

POWER	$32\ \mu W$
AREA	$204\ x\ 149\ \mu m^2$
DNL_MAX	2.25 % of LSB
INL_MAX	1.5 %

Current DAC - Implementation



pMOS current source array

Thermometer encoding

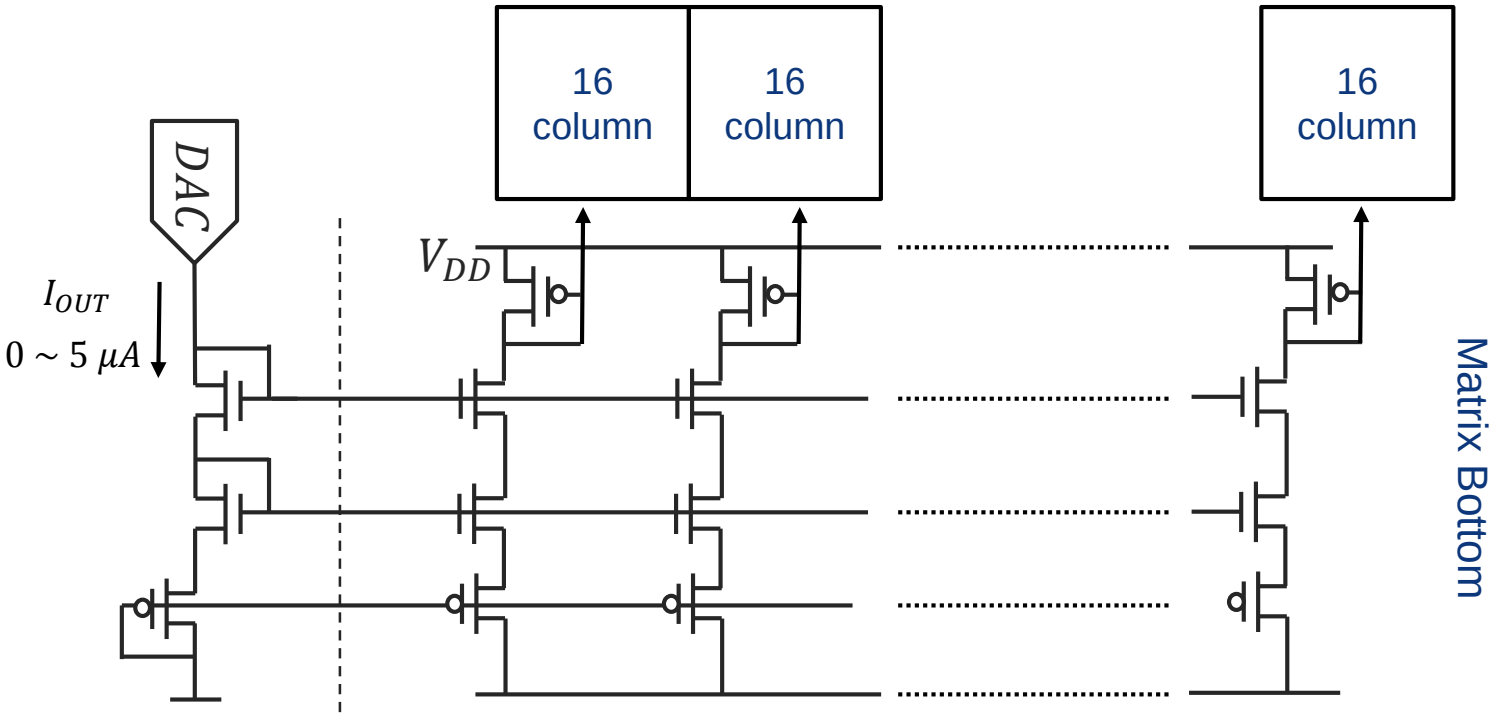
8 bits resolution (0 – 5uA)
$LSB \approx 20\,nA$

Cascode to guarantee a better linearity

TID effects depend on biasing voltage: same load on both I_{ON} and I_{OFF}.

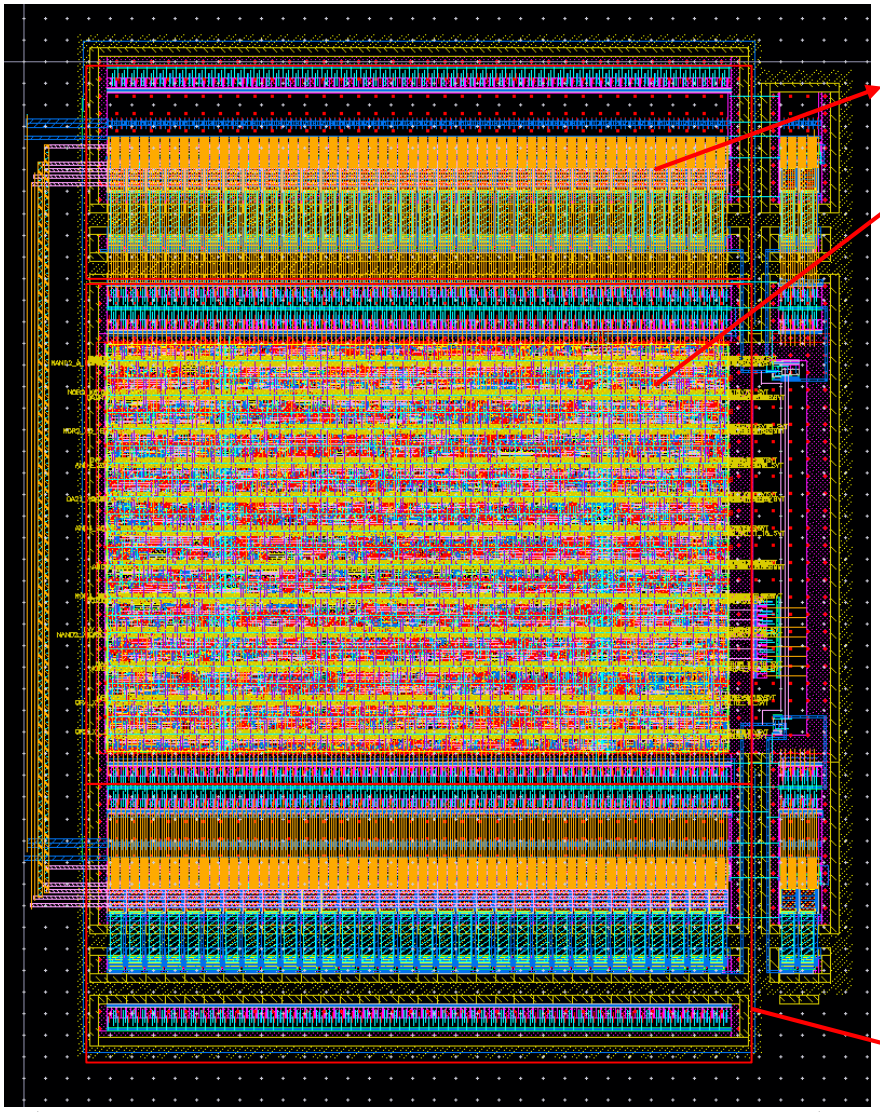
Possibility to use it with a Bandgap reference for PVT independence.

Last biasing stage - Implementation



Last biasing stage distributed under the matrix as in MALTA.
Cascode to guarantee a better linearity.
PMOS on ground to have ground uniformity despite voltage drops.
Biasing structure distributed at the bottom of the matrix all over the matrix.
Additional current mirrors to adjust the current ranges for the different biasing currents.

Current DAC – layout



IDAC Current sources from 256 to 129

8-Bit Thermometer Decoder

Same current reference used for all the IDAC on the chip

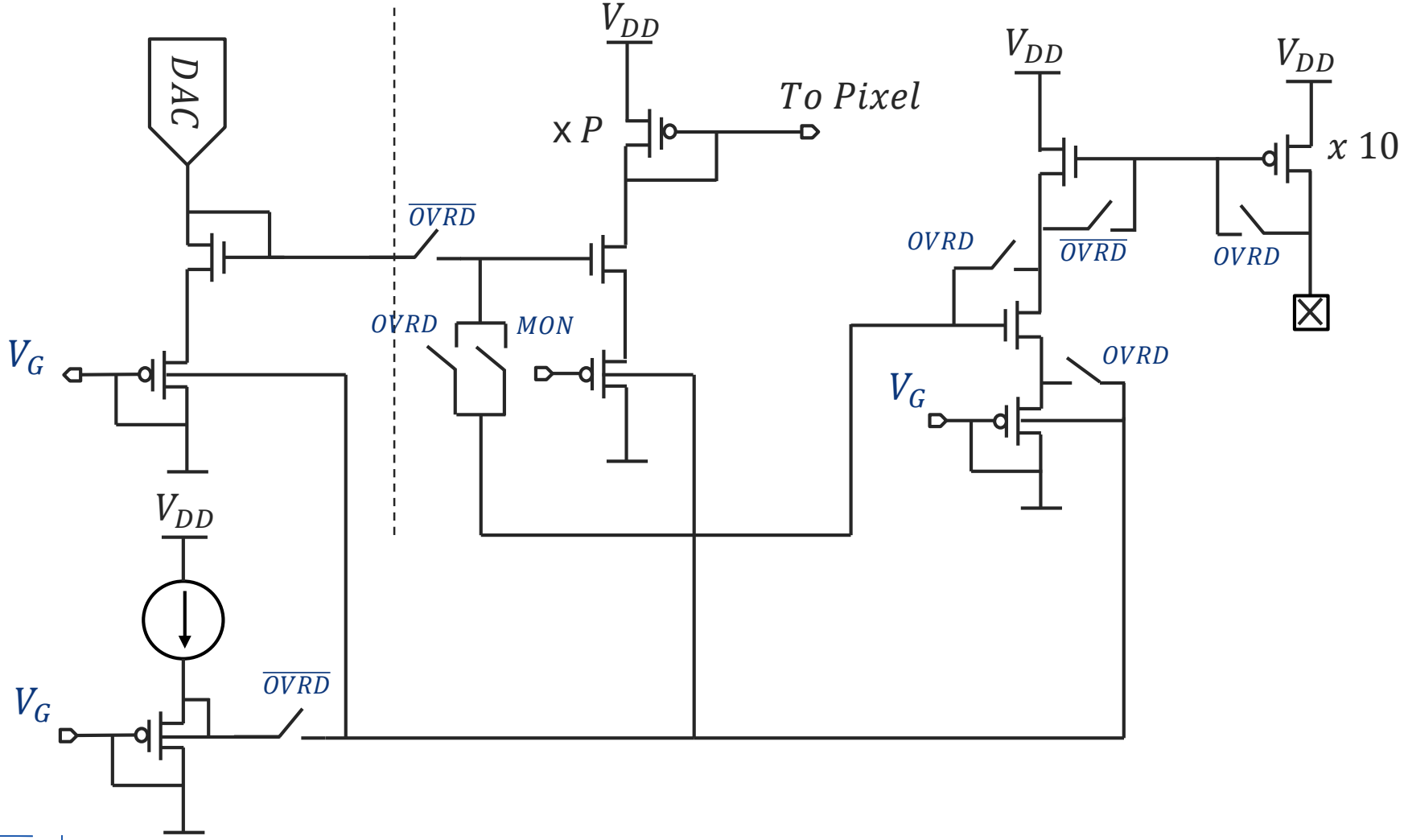
SPECIFICATION

POWER	$14\ \mu W$
AREA	$192\ x\ 237\ \mu m^2$
DNL_MAX	5.6 % of LSB
INL_MAX	3 %

IDAC Current sources from 128 to 1

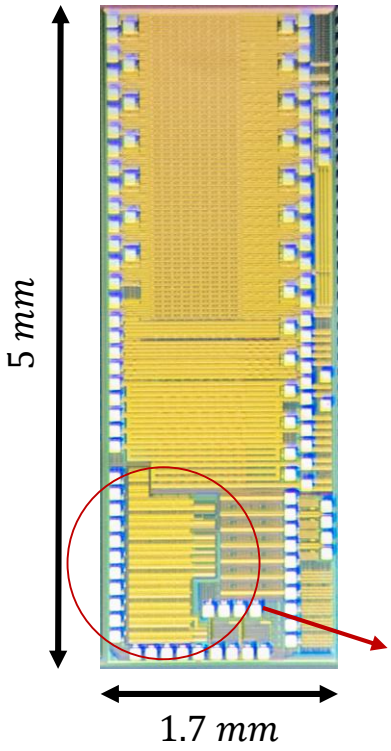
OVERRIDE-MONITORING

Circuit for override and monitoring implemented under the PADs, through a system of switches.



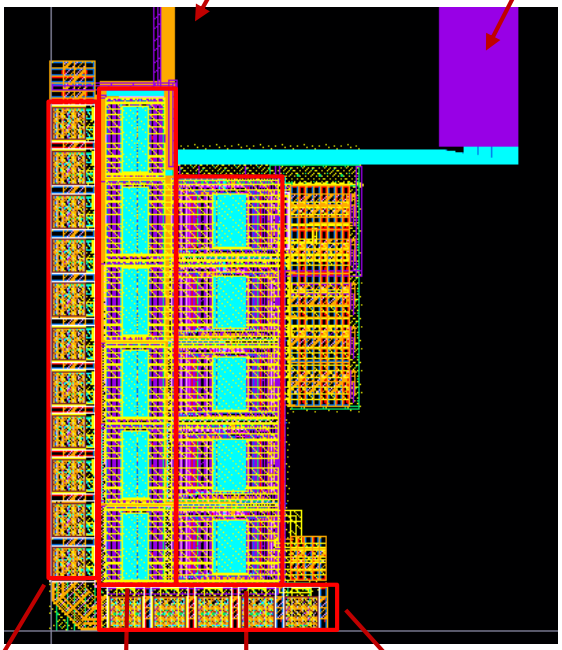
Integration in MiniMALTA and testchip

MiniMalta :



Analog interconnection between DACs and biasing structures

Digital Control lines



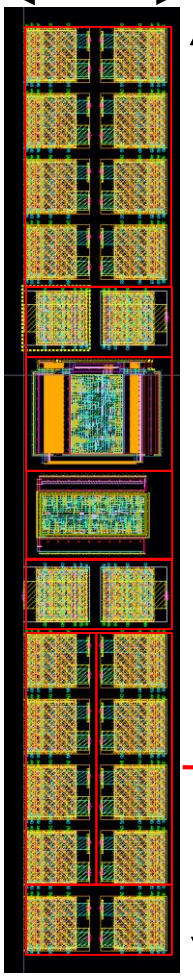
PAD OVRD & MON I/V

IDACs

VDACs

SUPPLY & SUB

Test-chip implemented as a baseline solution in case of malfunctioning on MiniMalta



Common input CODE Pads

AVDD

IDAC

VDAC

AVSS

Controls and outputs IDAC

SUB

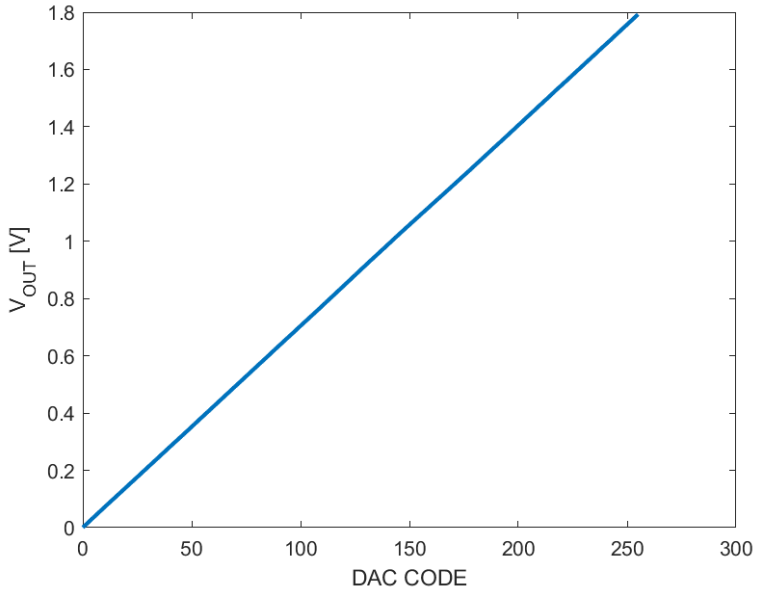
Controls and outputs VDAC

DACs testing

MPW submitted in August 2018 and arrived on 7th January 2019.

MiniMalta DACs tested in monitoring mode.

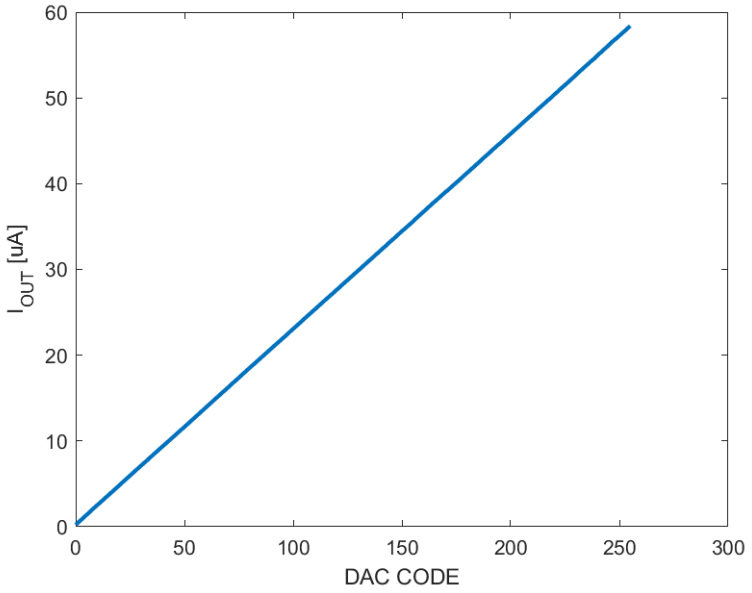
VDAC



$INL_{MAX} = 1.5\%$

$DNL_{MAX} = 5\%$ of LSB

IDAC

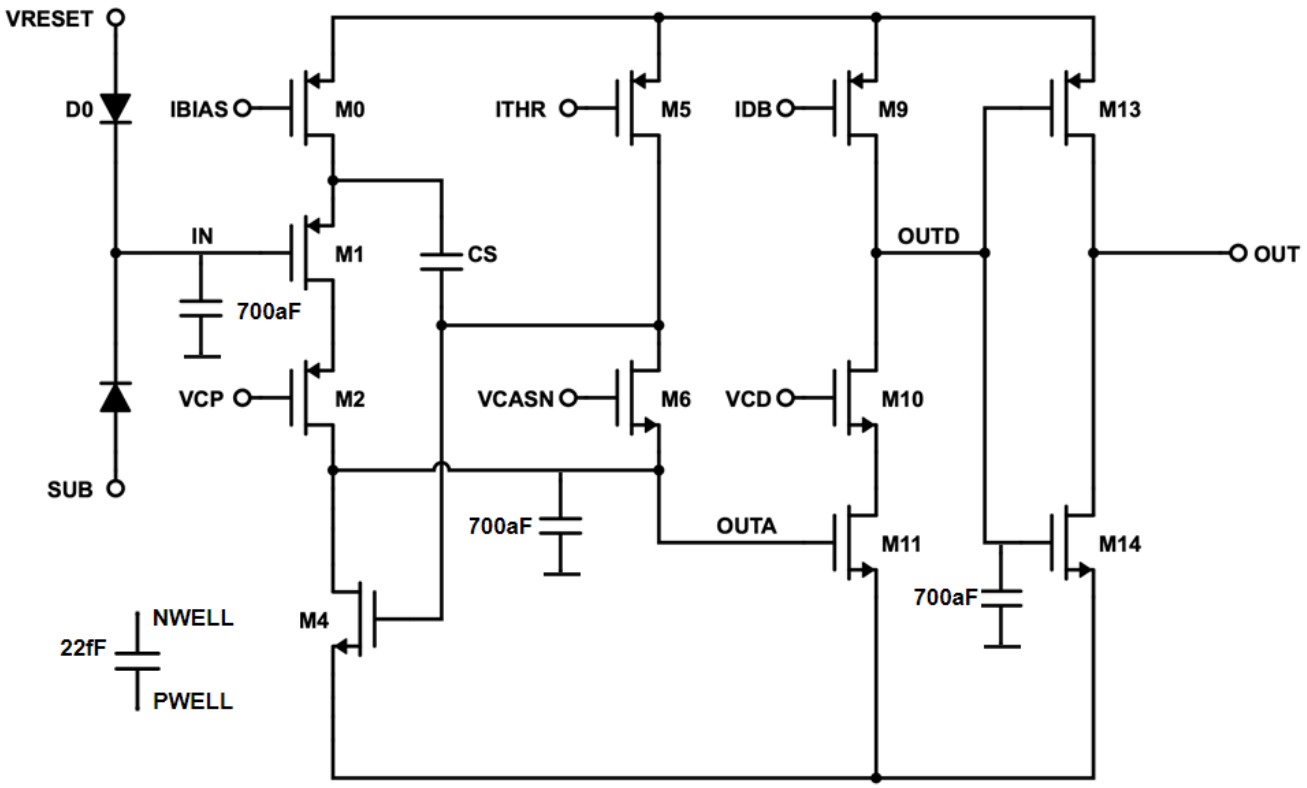


$INL_{MAX} = 2\%$

$DNL_{MAX} = 10\%$ of LSB

FE developments

FE simulations to improve Mismatch (threshold uniformity) and ENC (Equivalent Noise Charge)



FE schematic and configuration as in MALTA.

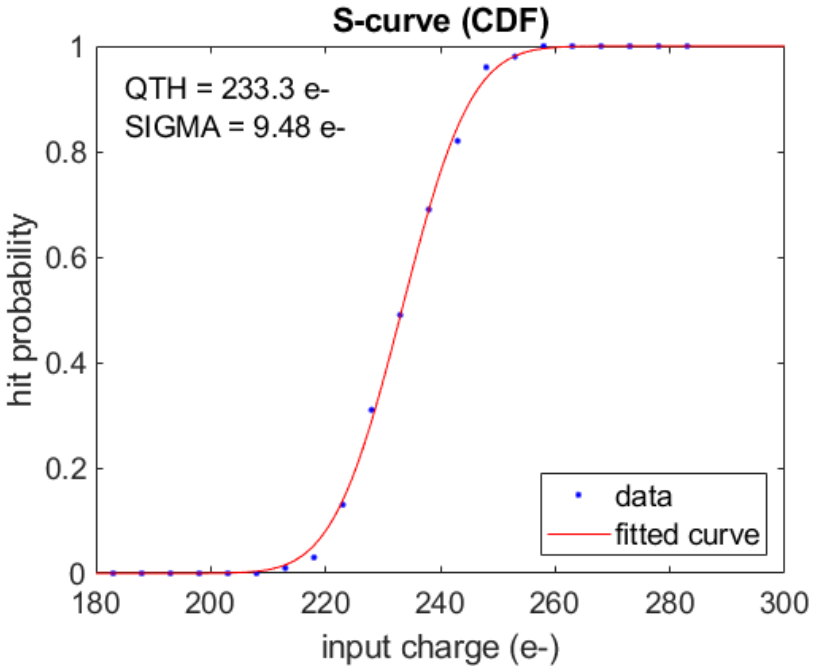
Parasitic routing capacitances and well capacitances in test-bench cell.

Simulations performed both in diode and PMOS reset case (with PSP model to have a better model of the noise)

Simulation performed with $I_{LEAK} = 200\,pA$ (typical value after irradiation).

FE developments

MISMATCH



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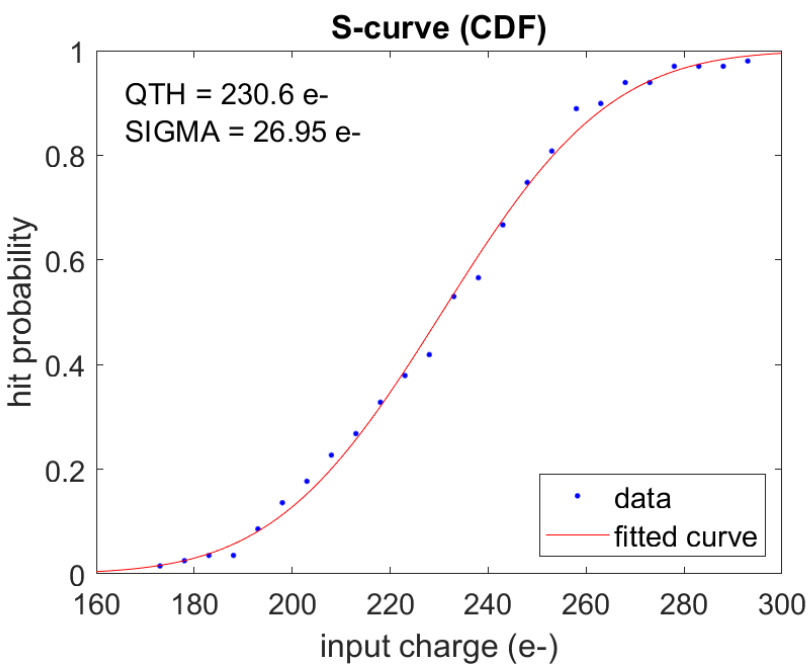


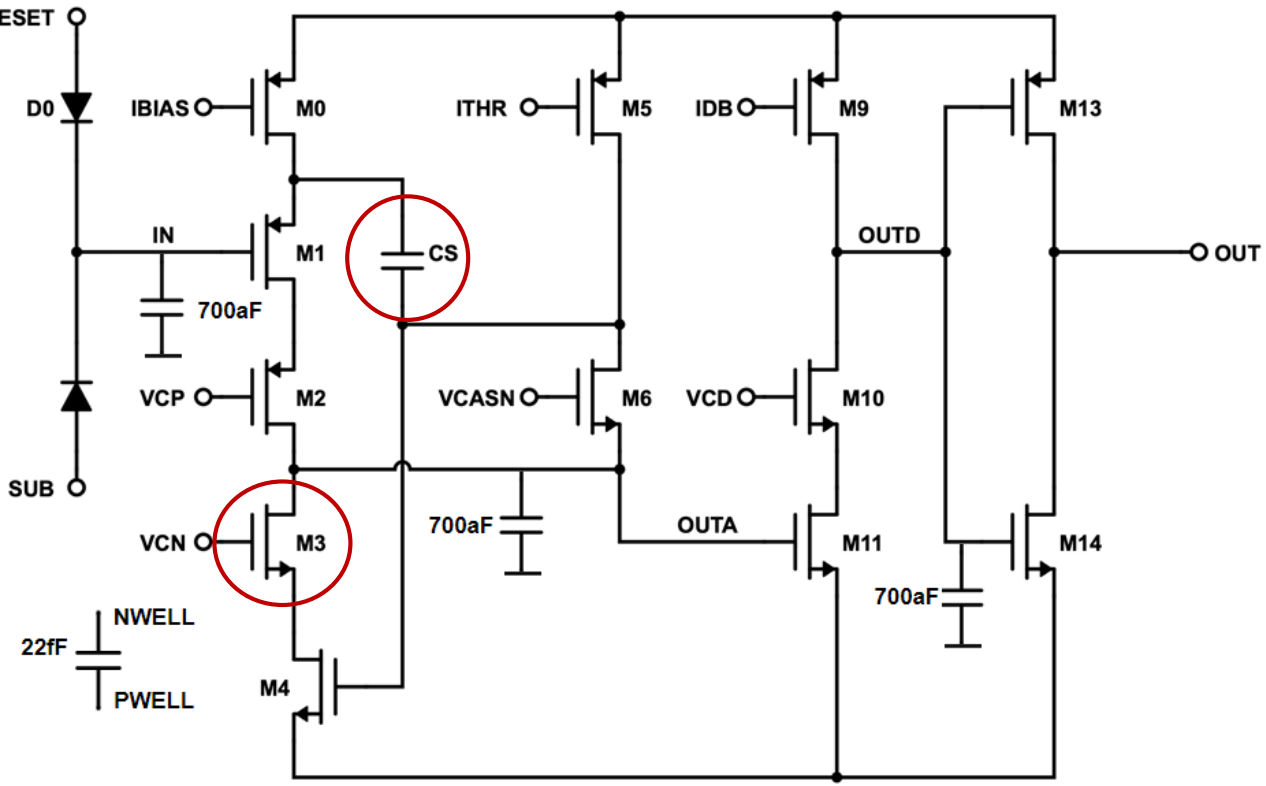
Main Mismatch source is the input transistor of the discriminator

Main ENC source is the input diode shot noise (dependent on I_{LEAK})

$$\sqrt{\left(\sigma_{IN}\cdot\frac{\mathrm{dA_Q}}{dQ}\right)^2+\sigma_1^2+\sigma_{VTH}^2}\cdot g_m=\sigma_I$$

To decrease the σ_{QIN} it is necessary to increase the gain

New FE schematic



Filtering capacitance twice as before.

Cascoded NMOS at the bottom of the first stage.

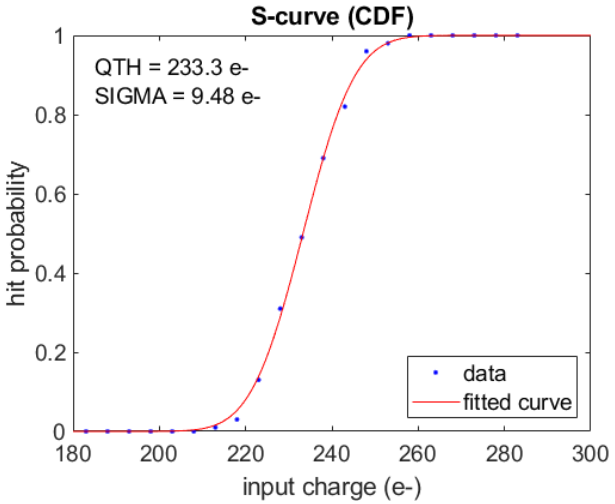
↓

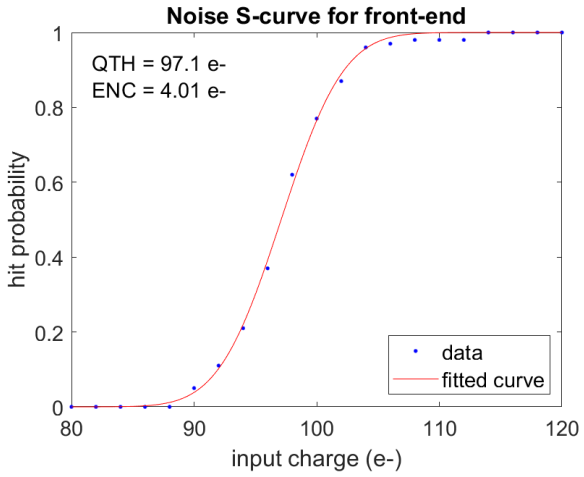
Steeper gain curve.

Area overhead ≈ 10 %

New FE results

MISMATCH





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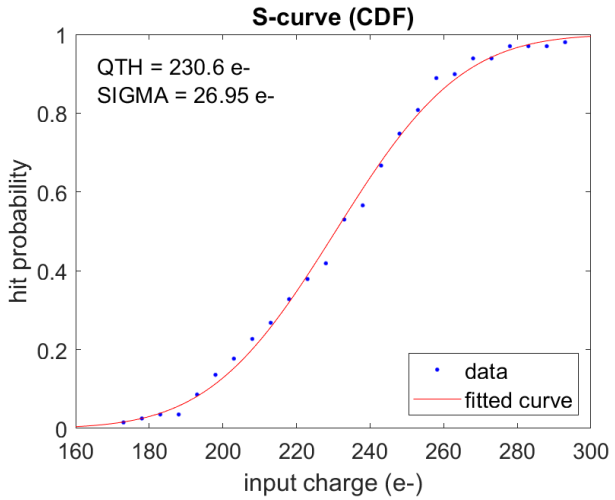

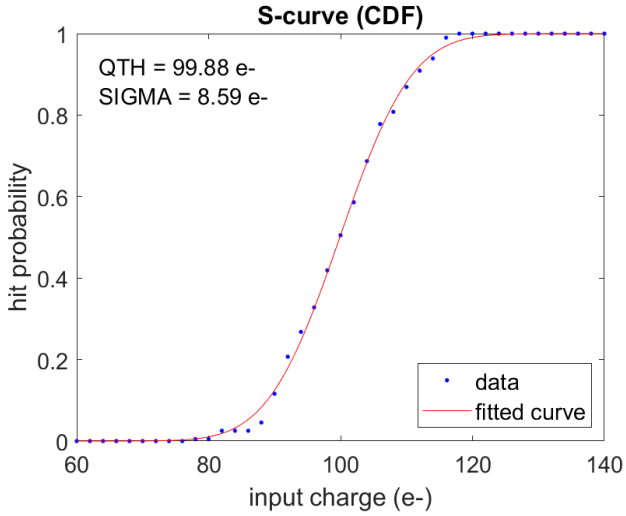

Training and Courses

EPFL courses:

-Advanced Analog CMOS IC Design
-PLL and Oscillators

Europractice course at IMEC, Leuven:

Digital physical implementation flow (feat low power)

PRINCE2 at The Academy, Eindhoven:

Intensive course on project management

Training course on Entrepreneurship at CERN, Geneva:

Course on business planning and modelling

Thank you for the attention