OXIDE-OXIDE BOND PROCESSING AND CHARACTERIZATION FOR EARLY STAGE, CHIP-TO-CHIP, CU/SIO2 HYBRID BOND RESEARCH

STREAM WP5: TECHNOLOGY INTEGRATION

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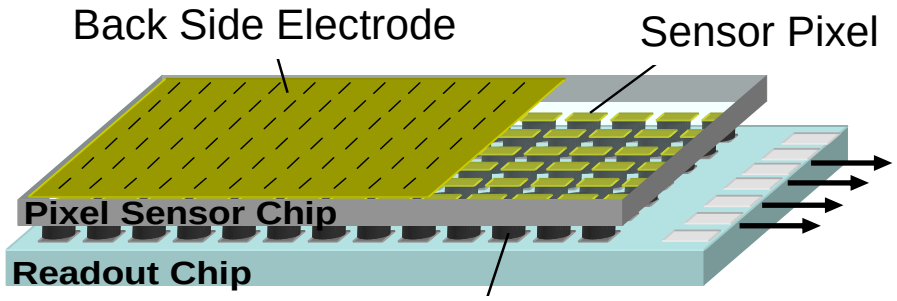
10.01.2019

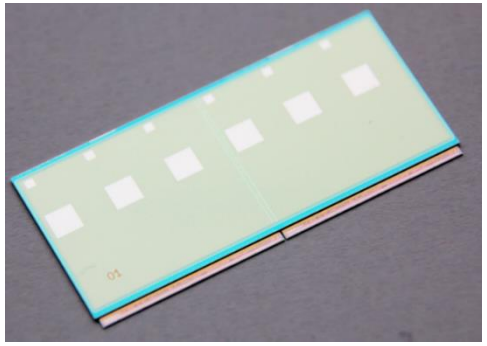
Agenda

- Introduction
  - Motivation
  - Mechanism
- Process Flow
  - Chip Handling
  - Cleaning
  - Planarization
- Evaluation Methods
  - Activation
  - Bond Reliability
  - Planarity

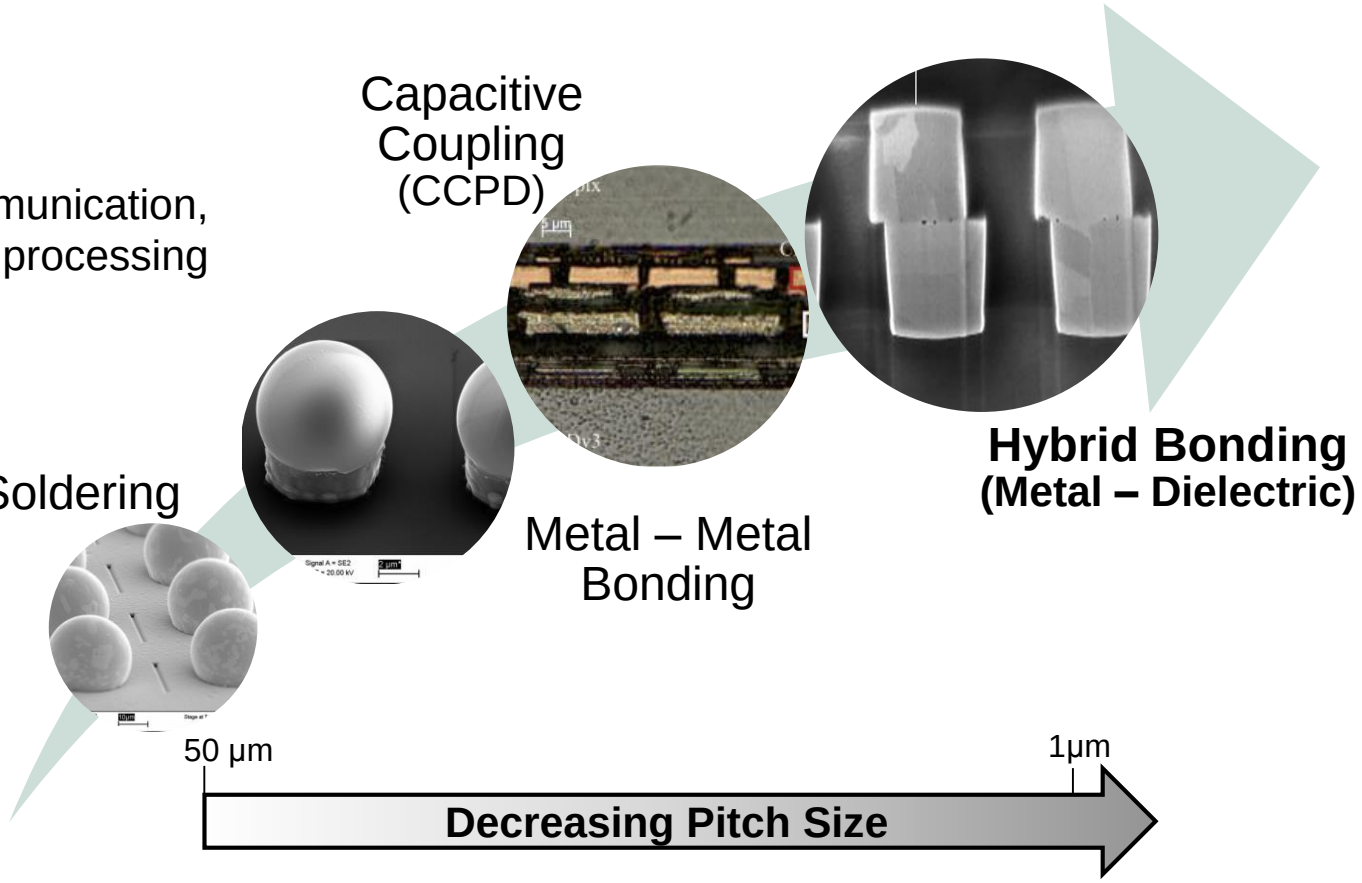
Bonding of Hybrid Pixel Detector Modules



Communication,
Data processing

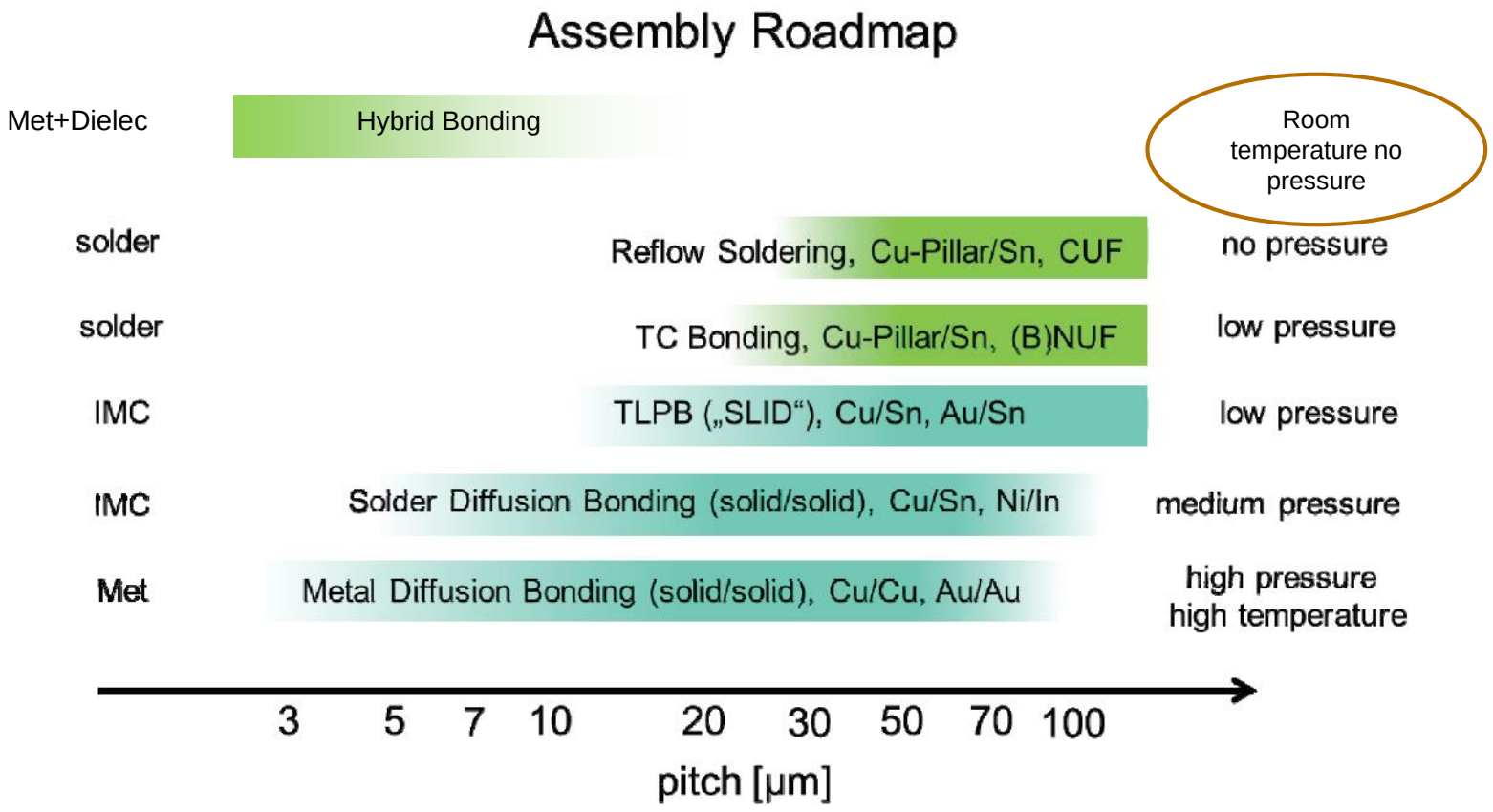


ATLAS FE-13/FE-14 Pixel Detector Modules



Hybrid Bonding: Motivation

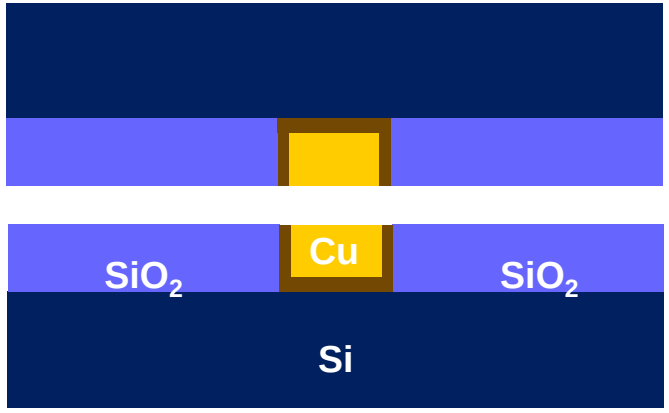
- Ultra fine **pitch**
- Compatible with **3D integration**
- Safe for **temperature-sensitive** applications
- Reduced bonding **time**
- Increased **reliability**
- Reduced **packaging** volume
- High **throughput**
- Increased **spatial resolution**
- Fast **signal processing**
- Efficient **charge collection**



H. Oppermann, K.-D. Lang, "Tackling Low Temperature Bonding in Fine Pitch Applications," LTB-3D, p. 41, 2017

Hybrid Bonding: Mechanism

- Dielectric silicon dioxide over CMOS with patterned metal interconnects
- Hydrophilic oxide-oxide bonding + Cu-Cu Inter-diffusion



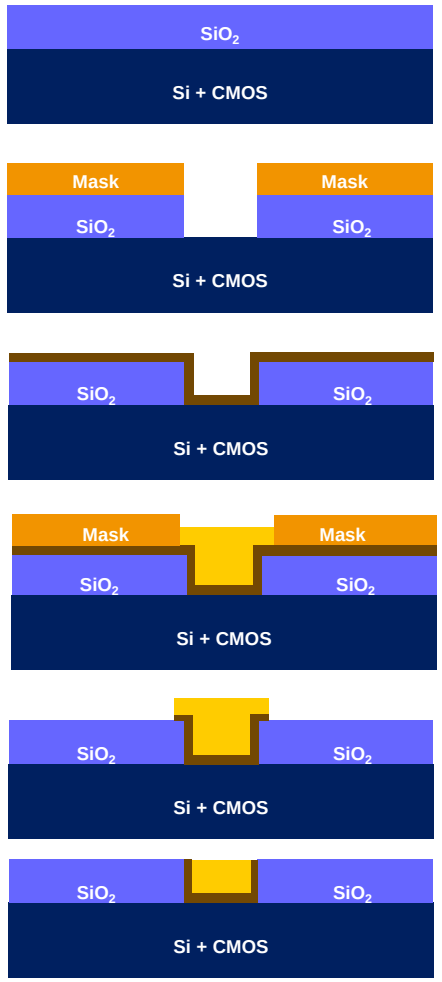
I. Hybrid Bonding
- Room-temperature
- No pressure
- Instant

II. Post-bond Annealing
- Up to 200˚C
- 1 hour or less

critical surface criteria:

sub-nm roughness | contaminant-free | active

Hybrid Bonding Microfabrication Process Flow



Oxide Application/Growth

Lithographic Dry Etch

Plating Base Sputter

Metal Electrodeposition

Plating Base Etch

Metal, Oxide Chemical Mechanical Planarization

Dicing

Chip Handling

Clean

Activate

Bond

Anneal

Phase I — Working Concept Development

Phase II — Characterization
Chip-level, thermal oxide

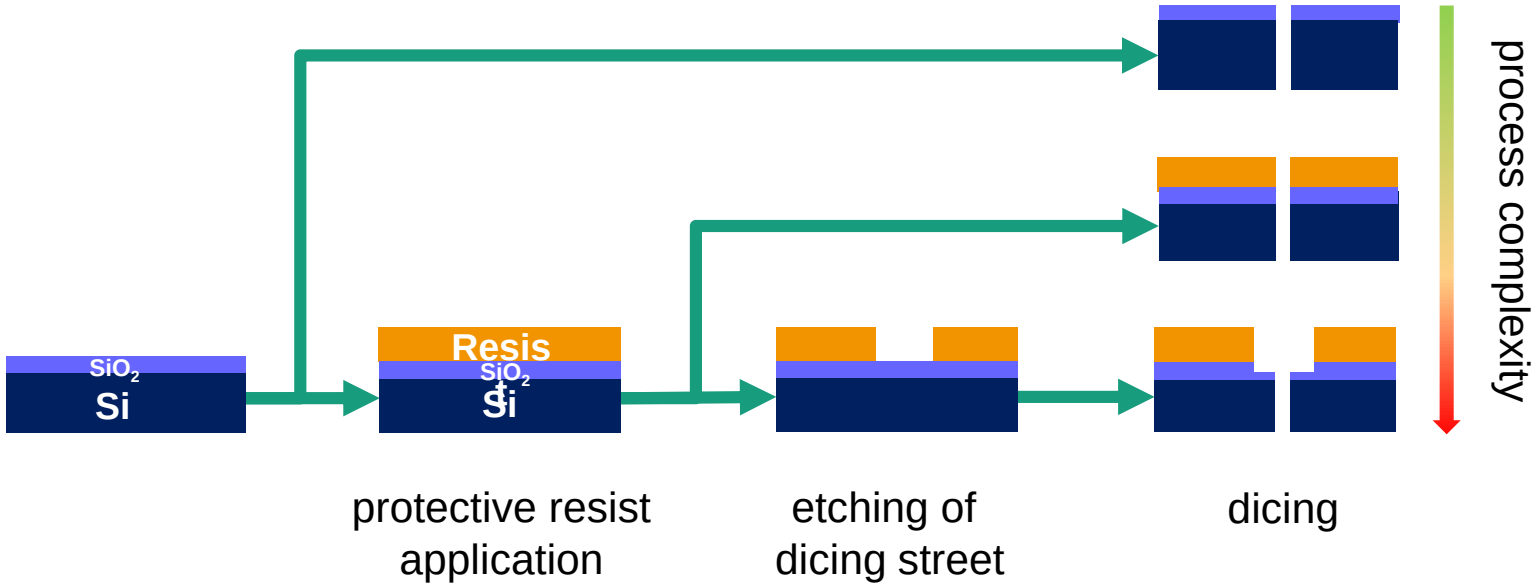
Phase III — Planarization
Wafer-level, PE-CVD oxide

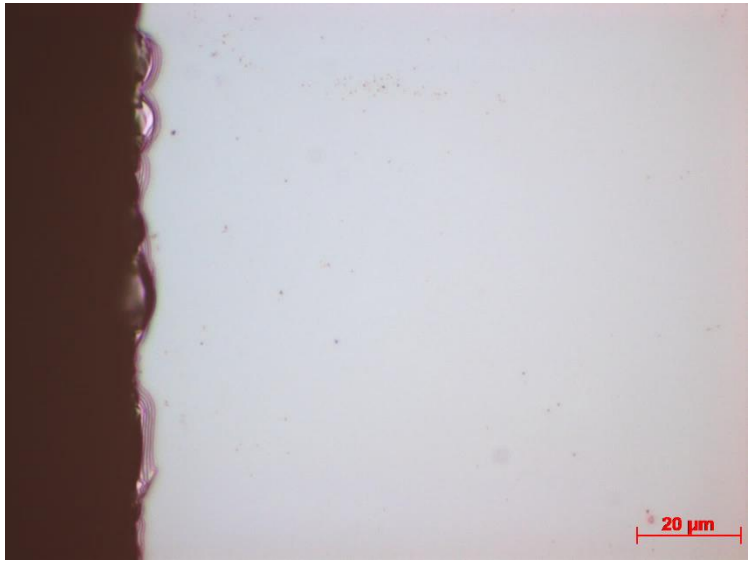
Phase IV — Concept Extension
Chip-level, Cu+PE-CVD oxide

Chip Handling: Preventative Measures

Dicing
Chip Handling
Clean
Activate
Bond
Anneal

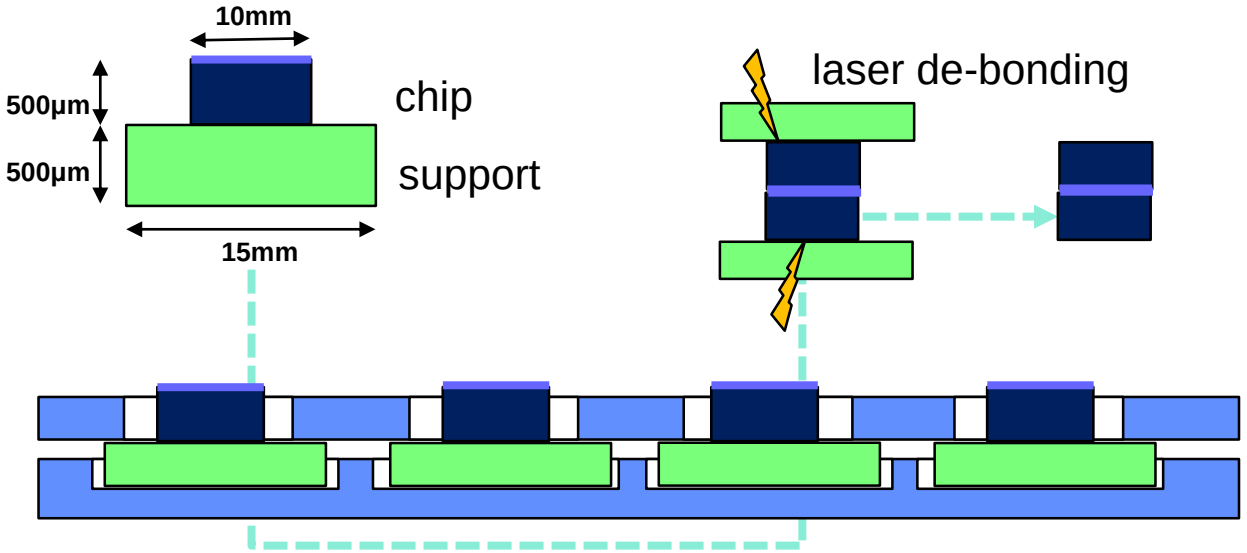
- Dicing stage generates most particle contaminants that are not easily removed
- Oxide chipping and non-planarity caused by dicing prevent bonding

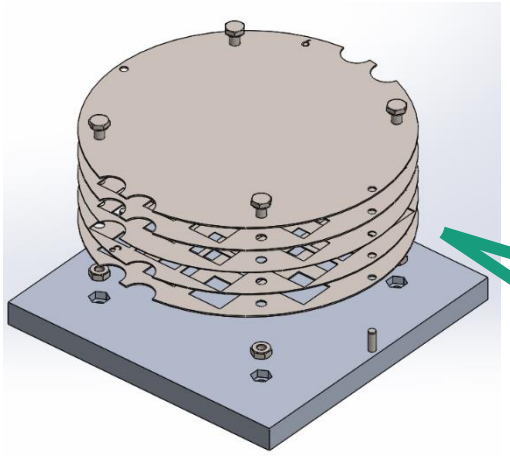


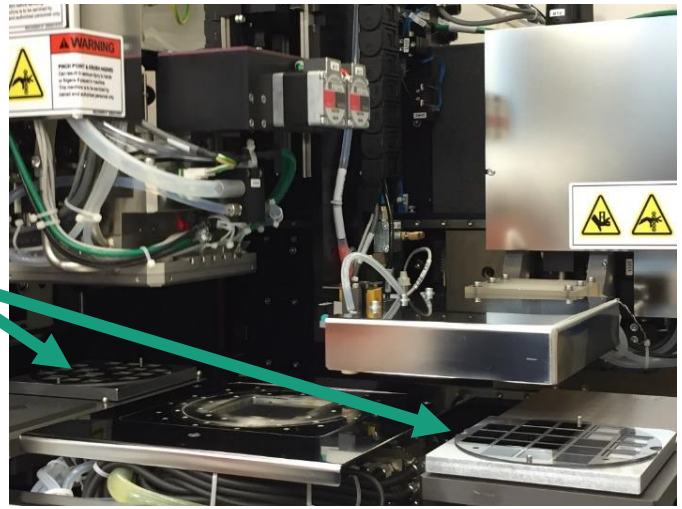


Chip Handling: Tool

- Contact-less chip cleaning, activation, bonding and storage
- 100 mm (4”) modular, stacked tool and baseplate; compatible with downstream wafer processing equipment (cleaning, activation, P&P)







Cleaning

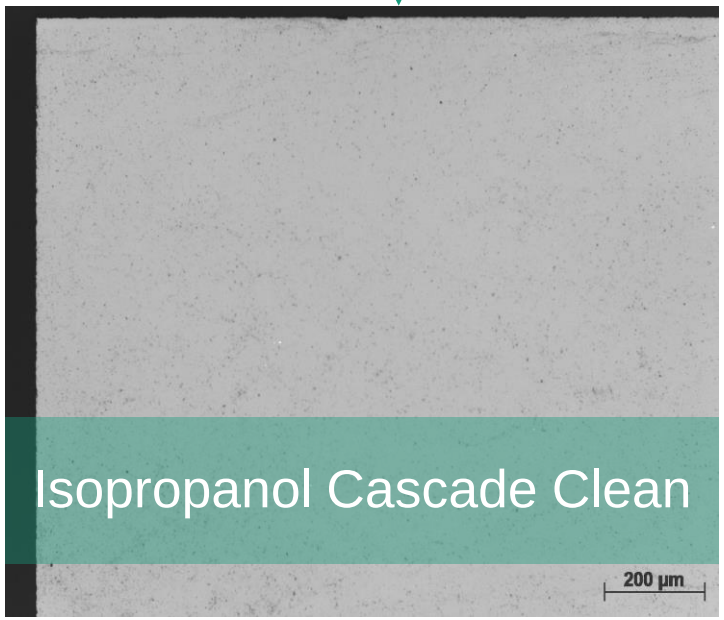
Wet

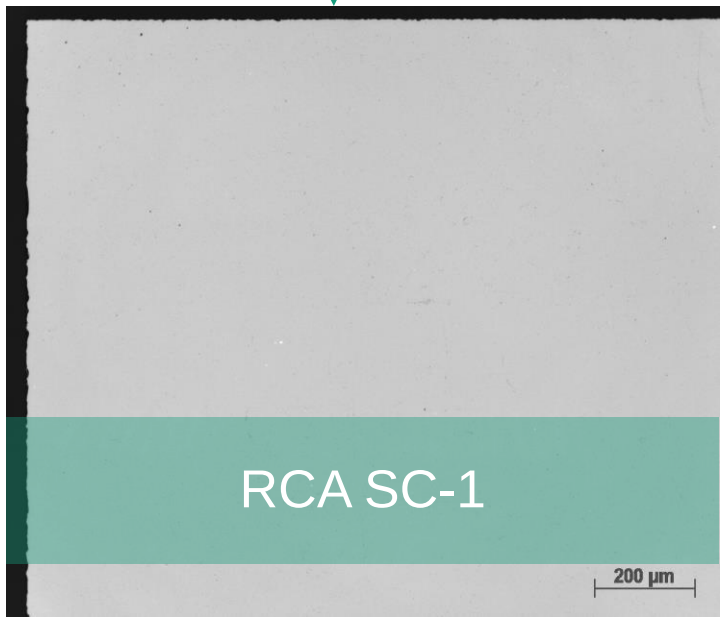
Isoprop. / DI Water Clean

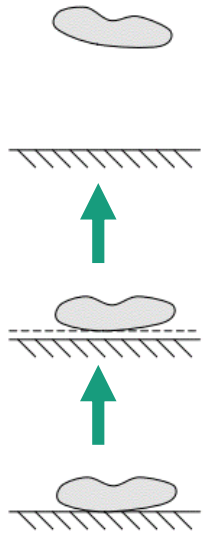
Alkaline Chemical Clean

Dry

Plasma Surface Treatment







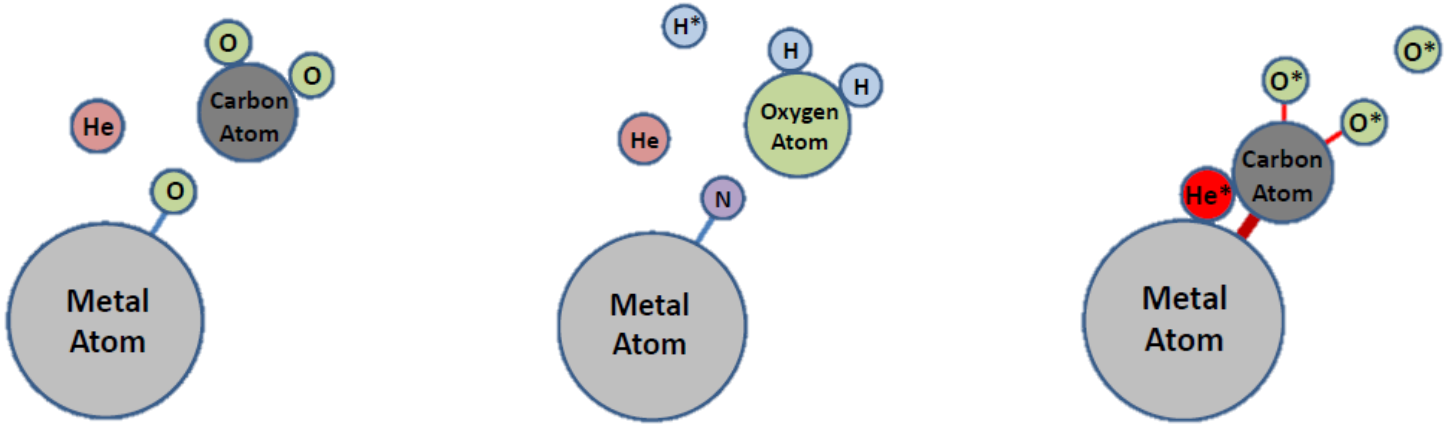
electrostatic repulsion

surface etch

Surface Activation by Ontos7 Atmospheric Plasma System

Dicing
Chip Handling
Clean
Activate
Bond
Anneal

- Surface atomic modification by reaction with activated gas-phases
- Quicker, more sensitive and less cross-contamination than vacuum Reactive Ion Etching (RIE) plasma

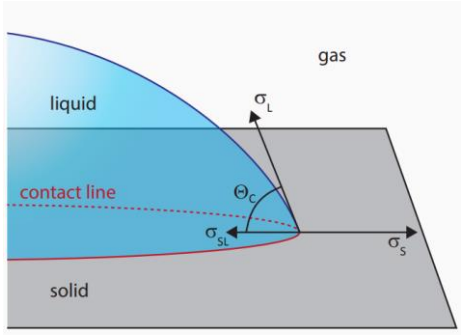


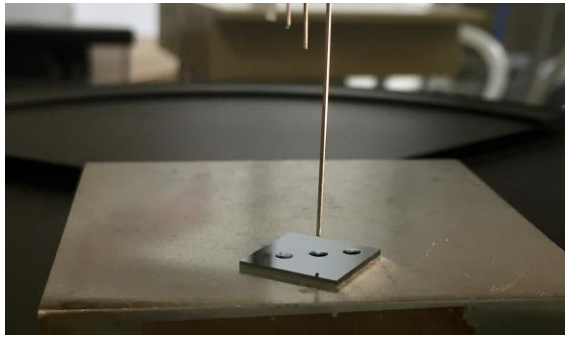
surface wetting oxide removal organics removal

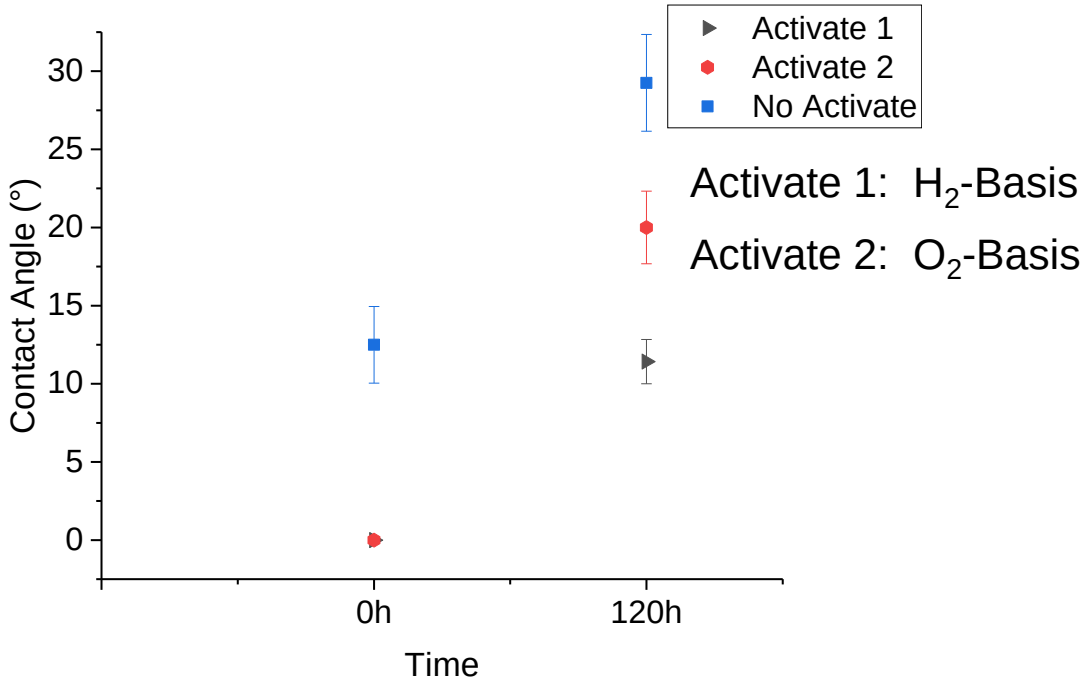
Setna, LLC ©

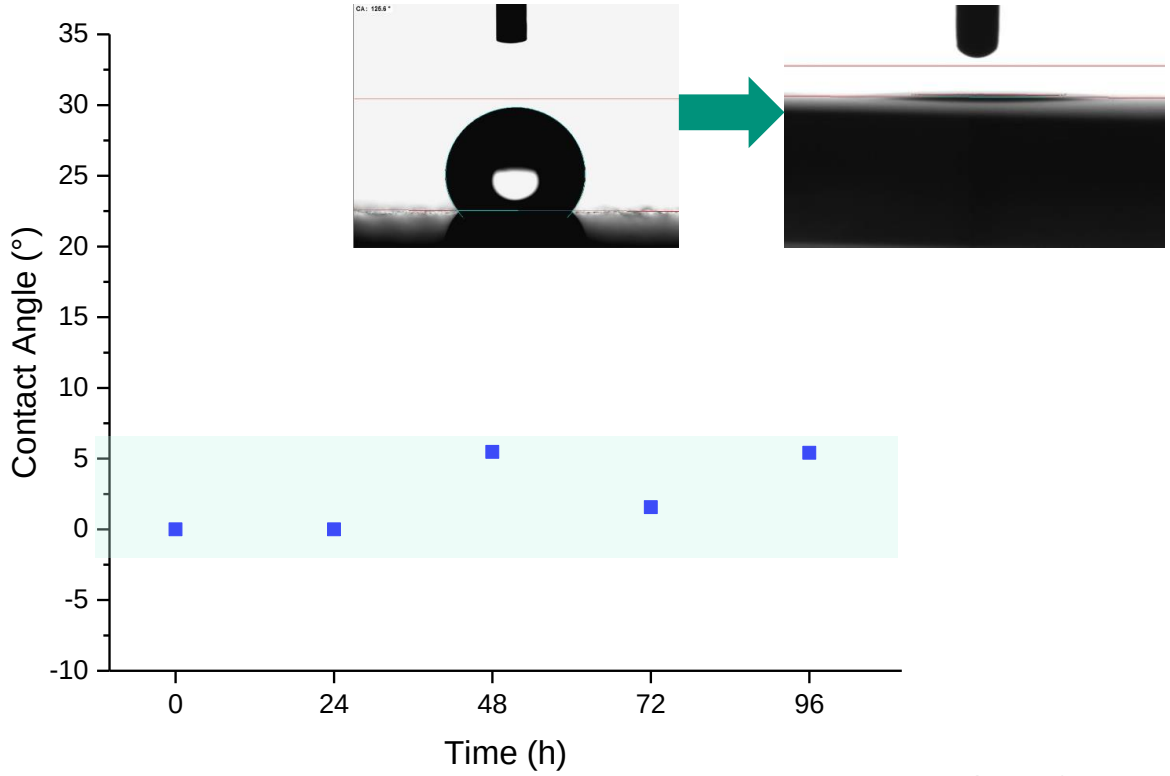
Evaluating Surface Activation: Contact Angle Measurement

- Hydrophilicity increases with H_2 gas phase content
- Hydrophilic up to 96 h (4 d) after activation



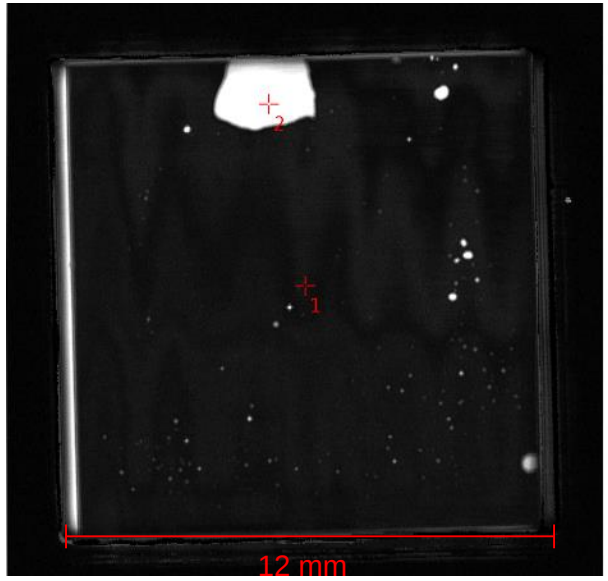


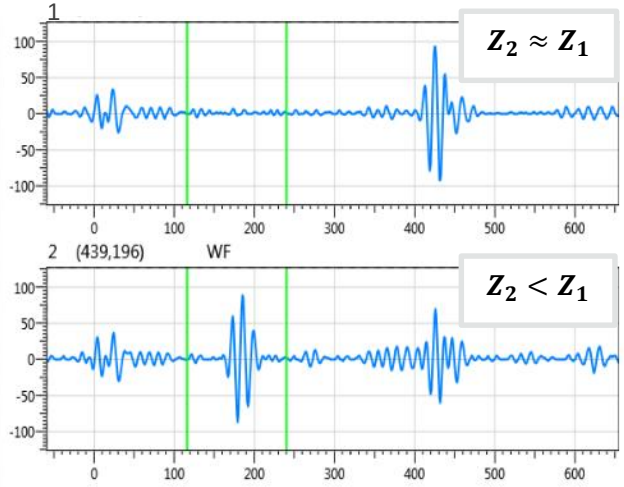




Evaluating Bond Reliability: Scanning Acoustic Microscopy

- Analysis of bond area from binary image for **quantitative comparison** of bond quality

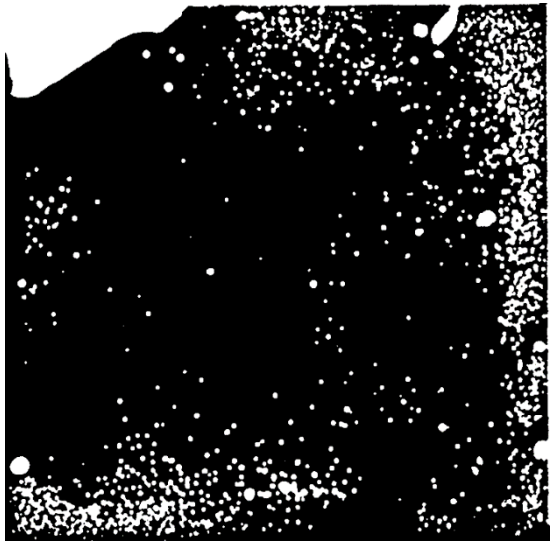




$$Z = \rho \cdot V$$

density velocity

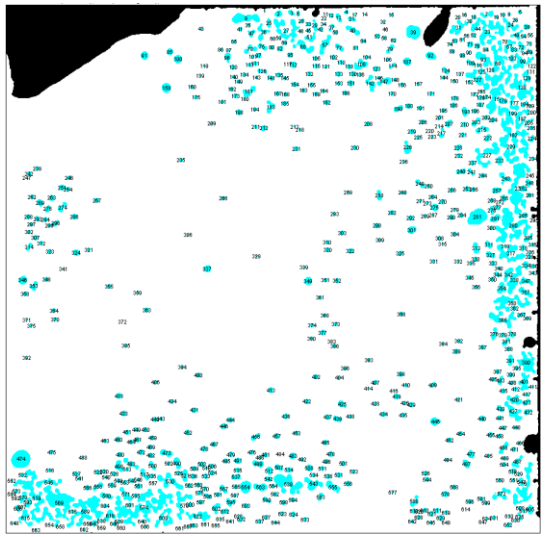
Bonded Area %



87% ■

13% □

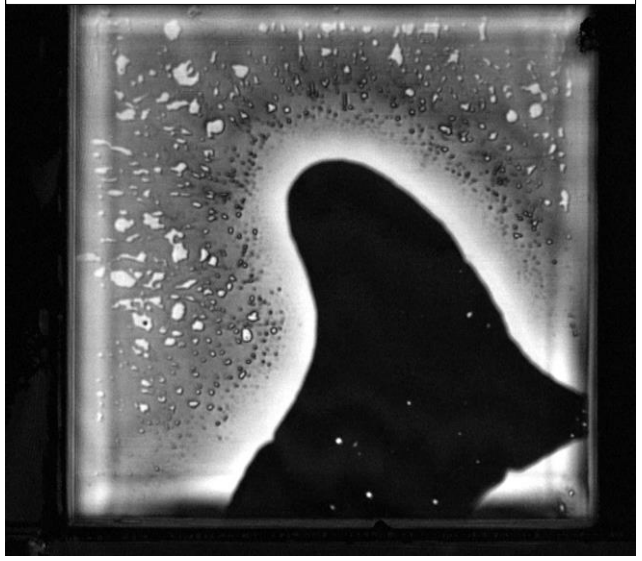
Void Quantity & Size



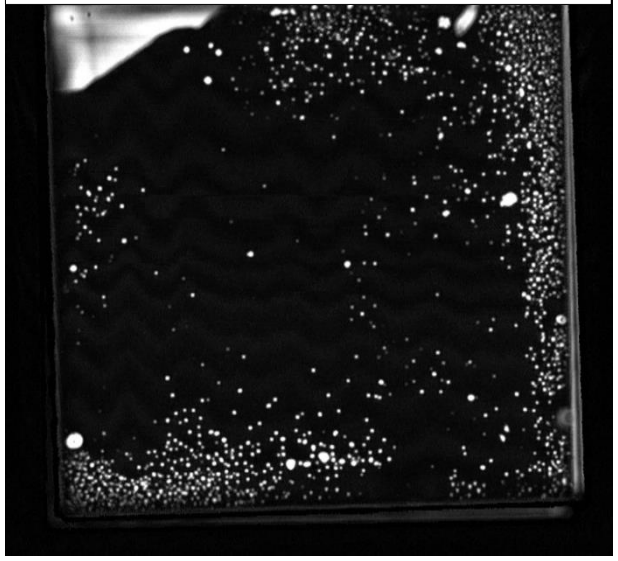
Evaluating Bond Reliability: Scanning Acoustic Microscopy
Cleaning Comparison

- Direct correlation between cleaning efficiency and bonded area [%]

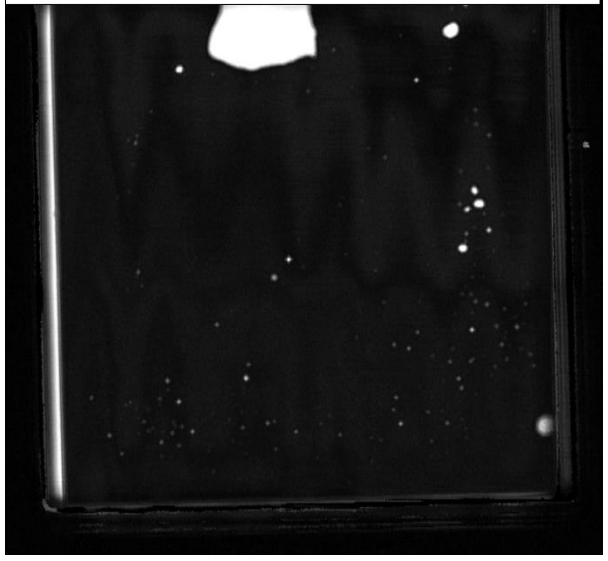
Isopropanol Bath: < 25%



RCA SC-1: > 85%

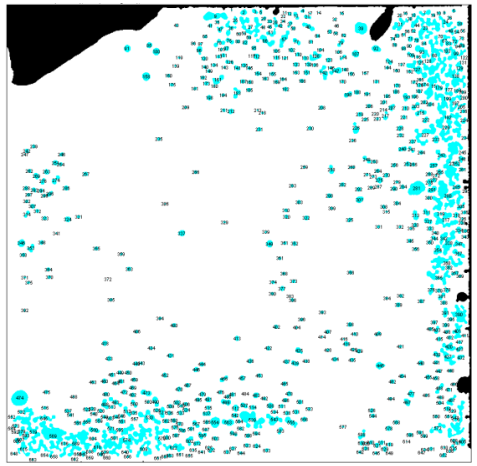


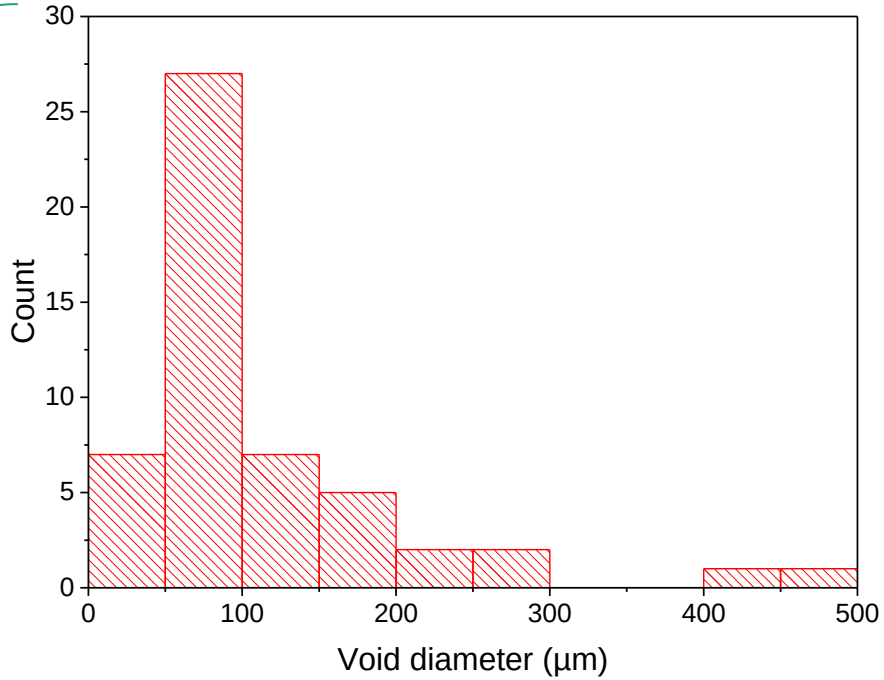
Ultrasonic Bath: > 95%

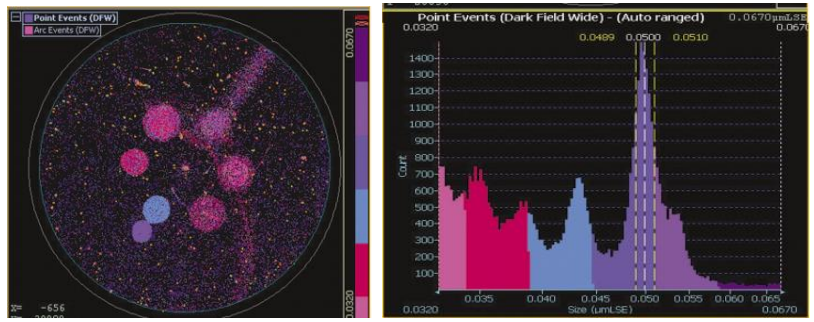


Evaluating Bond Reliability: Scanning Acoustic Microscopy

- Highest count void diameter in 50-100 µm bin
- Corresponding particle size to generate void:
  - 5 – 10 nm *(ProSys, Inc., CEA, EV Group)*
- Higher resolution surface inspection system (30 nm)
- Particle contamination prevention strategy







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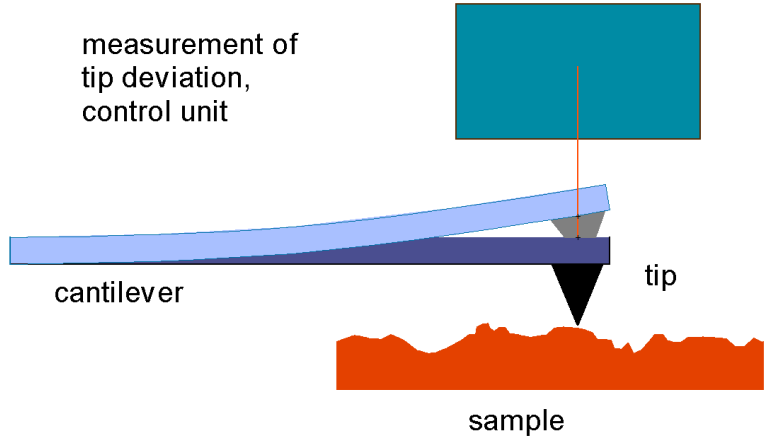
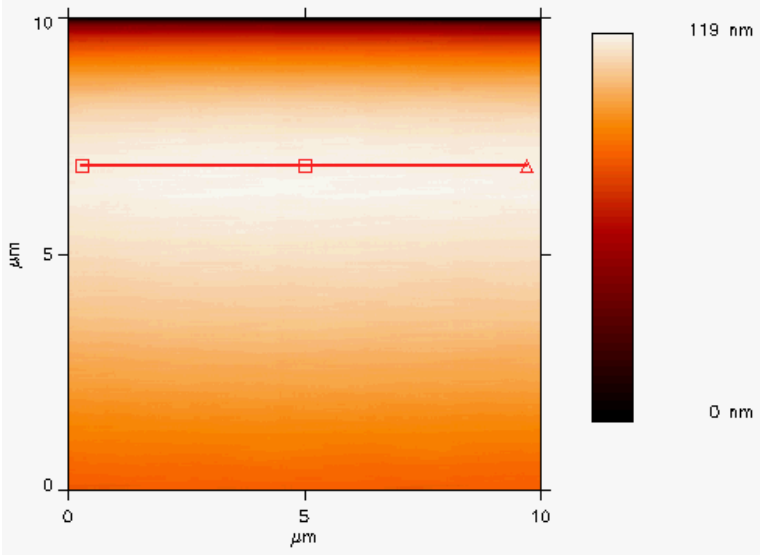
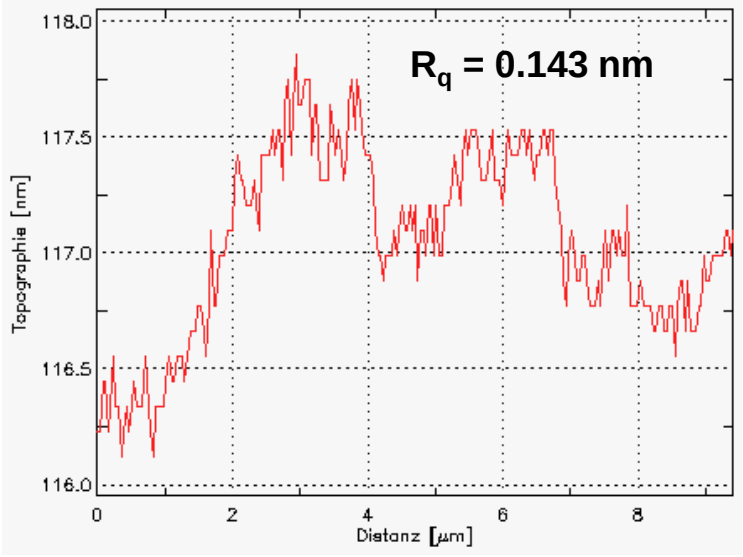
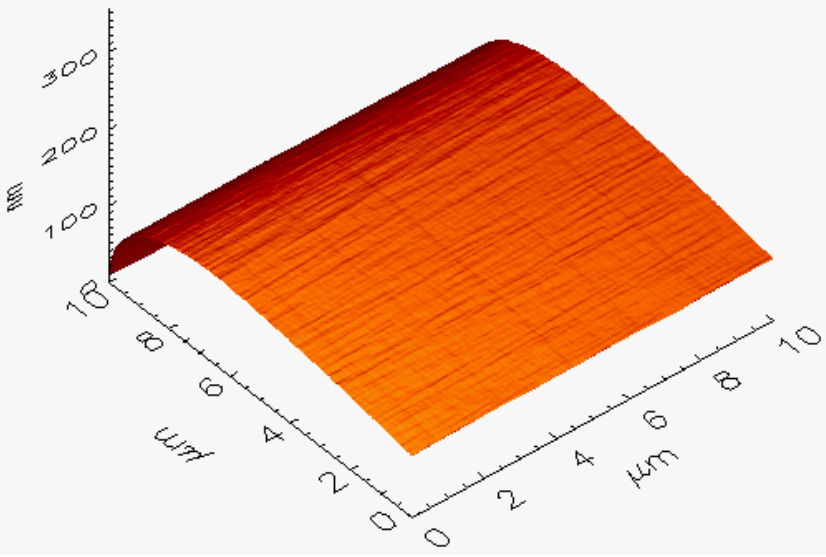
Evaluating Planarity: Atomic Force Microscopy (AFM)



- Scanning probe microscopy; non-contact mode
- Sub-nanometre atomic roughness critical (thermal oxide Rq < 0.2 nm)

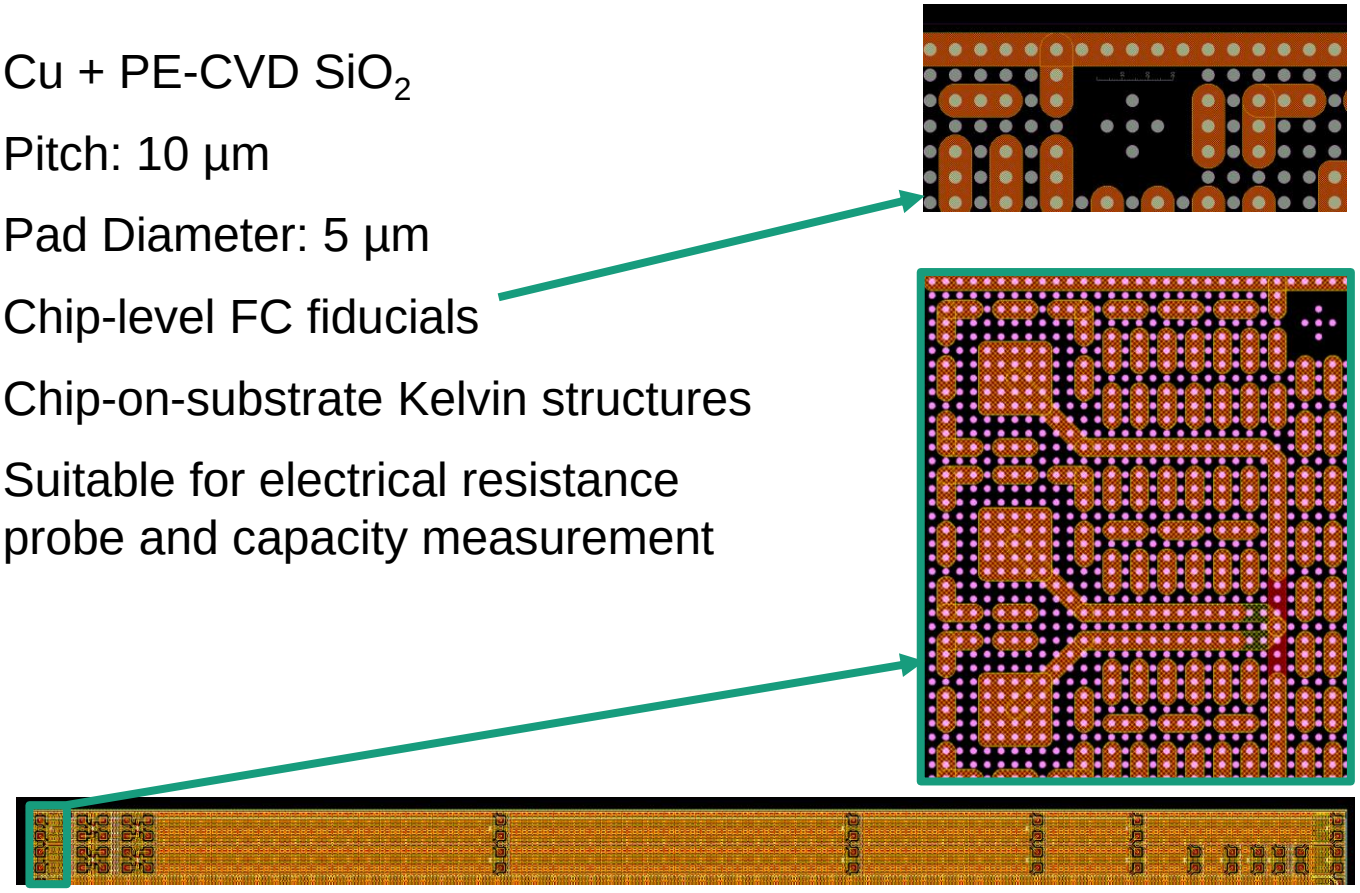


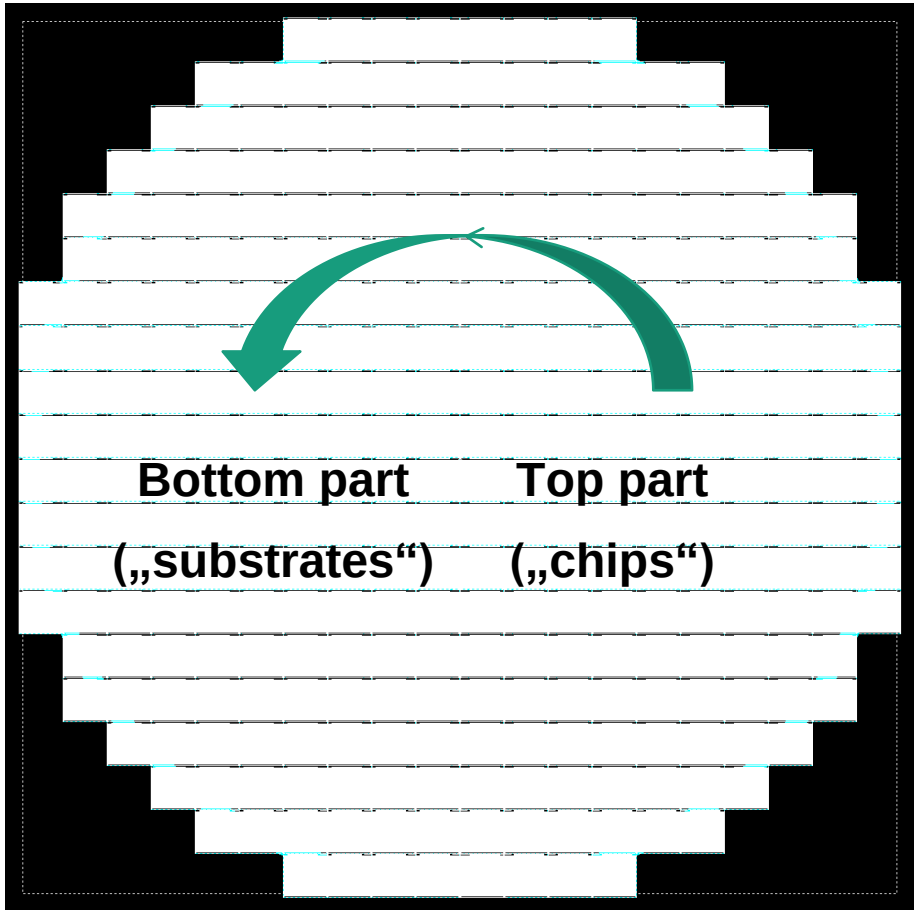




C2C Hybrid Test Chip Design

- Cu + PE-CVD SiO_2
- Pitch: 10 µm
- Pad Diameter: 5 µm
- Chip-level FC fiducials
- Chip-on-substrate Kelvin structures
- Suitable for electrical resistance probe and capacity measurement





Summary

- **Proof of concept** for first phase hydrophilic SiO2-SiO2 bonding
- **Evaluation** of wafer cleaning, activation and bonding using Atomic Force Microscopy (AFM), Scanning Acoustic Microscopy (SAM) and contact angle testing
- **Key findings**
  - sub-nanometer surface roughness
  - active surface up to 96 hours
  - consistent bond area of over 85%
- **Die handling tool** with wafer process compatibility for particle prevention and sample ramp up
- Next Steps:
  - Addressing limitations: **particle contamination** and **reliability of sub-nm measurements**
  - CMP and concept extension to PE-CVD oxide and Cu+PE-CVD oxide

THANK YOU

Fraunhofer IZM

Technische Universität Berlin