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Radiation tolerance of Depleted CMOS (D-CMOS) sensors

G. Casse

Abstract:

The non-ionising energy lost by energetic radiation to the structure of semiconductor sensors damages the crystal and consequently modifies the electrical characteristics of the devices.
All the parameters that are relevant to the performance of the sensors are changed: the current, the full depletion voltage, the response to ionising particles (signal), the inter-electrode resistance and capacitance (in segmented detectors). These changes are degrading the performance of the sensors and lead to their failure after significant fluences of impinging particles. The design of the sensors can be engineered to increase the failure fluence. Most of the radiation hardening was performed with hybrid segmented silicon sensors. Can this results be applied to deep depleted CMOS detectors?

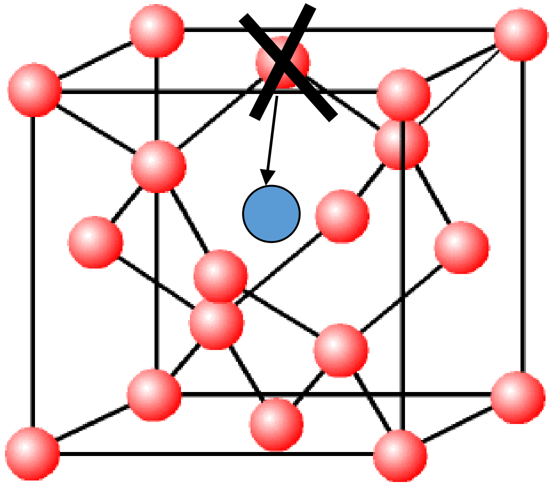
OUTLINE:

- What defines radiation tolerance
    - Radiation damage in silicon
    - Effects on detector performances
- Mitigation of sensor’s degradation
- D-CMOS: can they be designed radiation-hard?

Radiation with protons/neutrons

Surface damage: ion trapping in SiO_2, leading to charge on $Si\text{-}SiO_2$ interface. Sensor design must be robust against this (not discussed here).

Bulk damage: displacement of Si atoms within the crystal leaves vacancies and interstitials (defects).



- Energy needed to displace atom from lattice=15eV
- Damage energy dependent

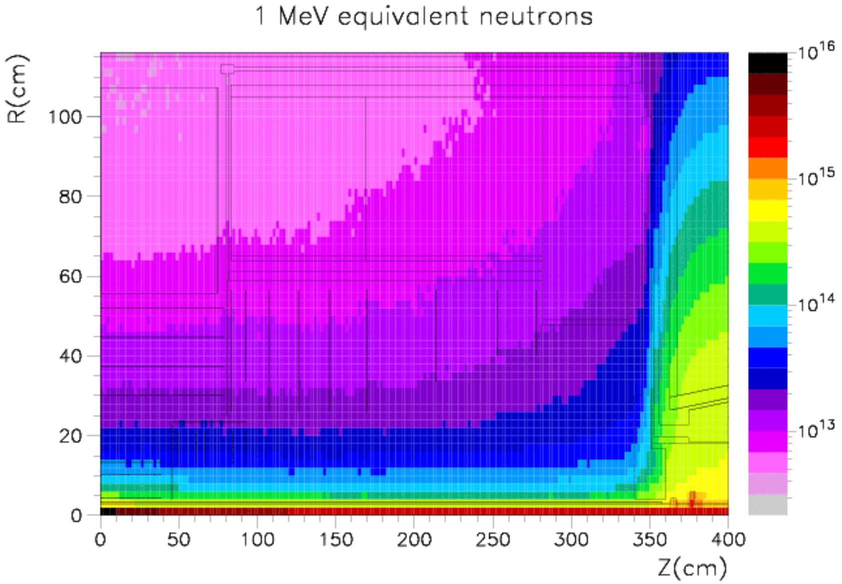
< 2 keV	⇒	isolated point defect
2-12 keV	⇒	defect cluster
>12 keV	⇒	many defect clusters

- This damage is called:

  Non-Ionizing Energy Loss (NIEL)

  – Results scaled to 1MeV neutrons

  (e.g. ATLAS ID up to ~$2\times10^{14}\ n_{eq}cm^{-2}yr^{-1}$)
- Electrons and photons don't make defects!



What radiation levels?

$e^+e^-\ 10^{12}\ n_{eq}\ cm^{-2}$

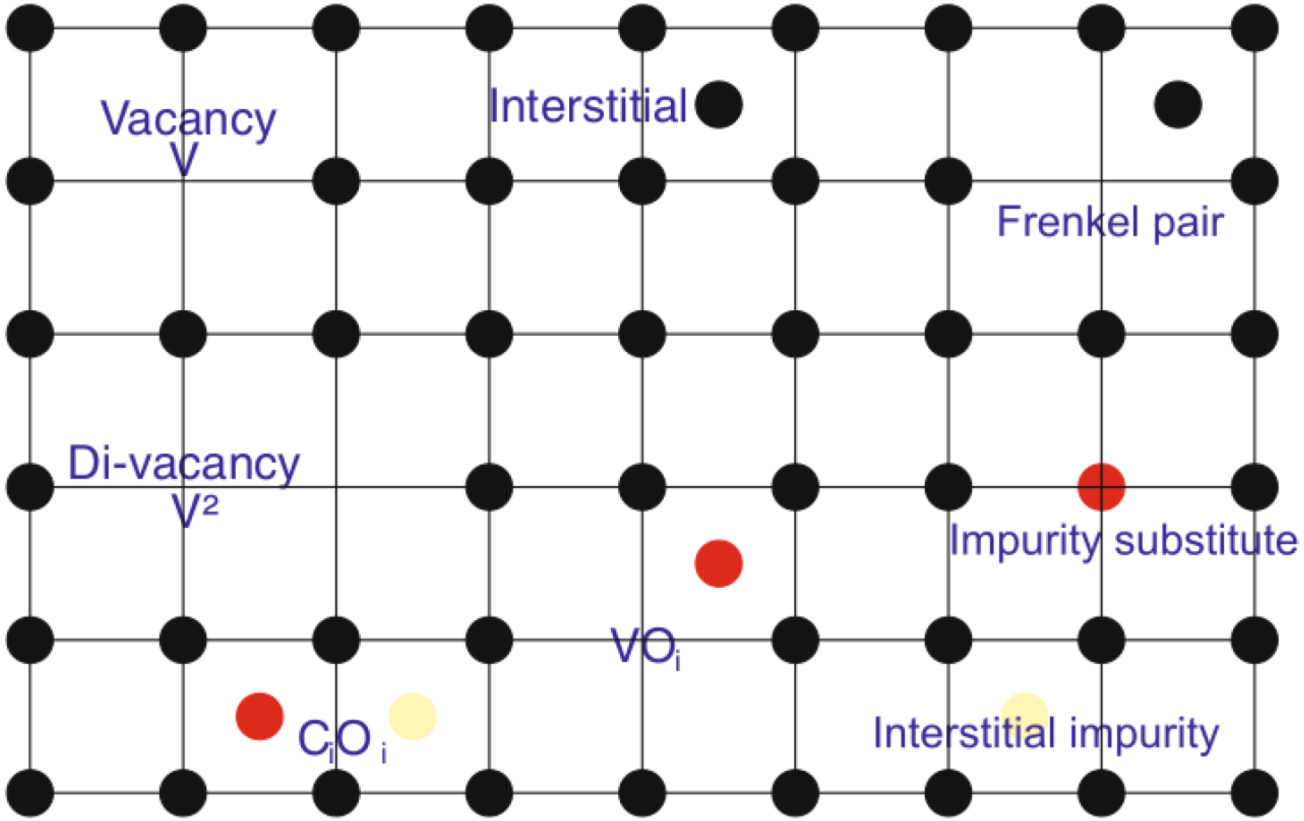
LHC $2\times10^{15}\ n_{eq}\ cm^{-2}$

HL-LHC $3\times10^{16}\ n_{eq}\ cm^{-2}$

FCC $7\times10^{17}\ n_{eq}\ cm^{-2}$

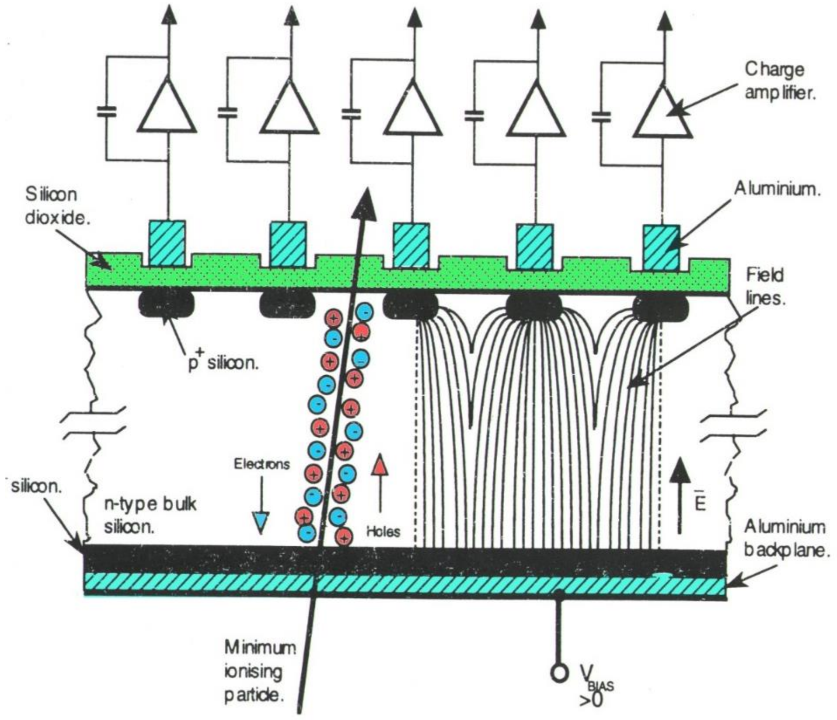
Microscopic view…

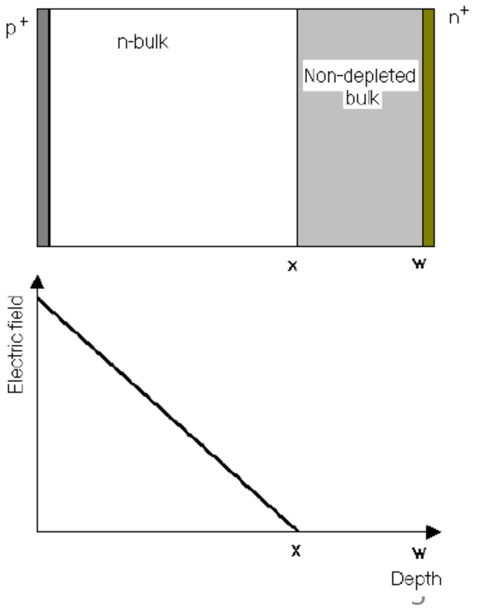
The damaged lattice ‘zoo’



J. Zhang

A fully depleted (array or matrix) silicon diode is a particle detector





Many diodes: p-strips in n-bulk

Positive (reverse-bias) voltage applied via conductive back-plane.

Depletes the detector and provides E-field for charge collection.

Deposited charge moves to nearest strip.

Typical signal

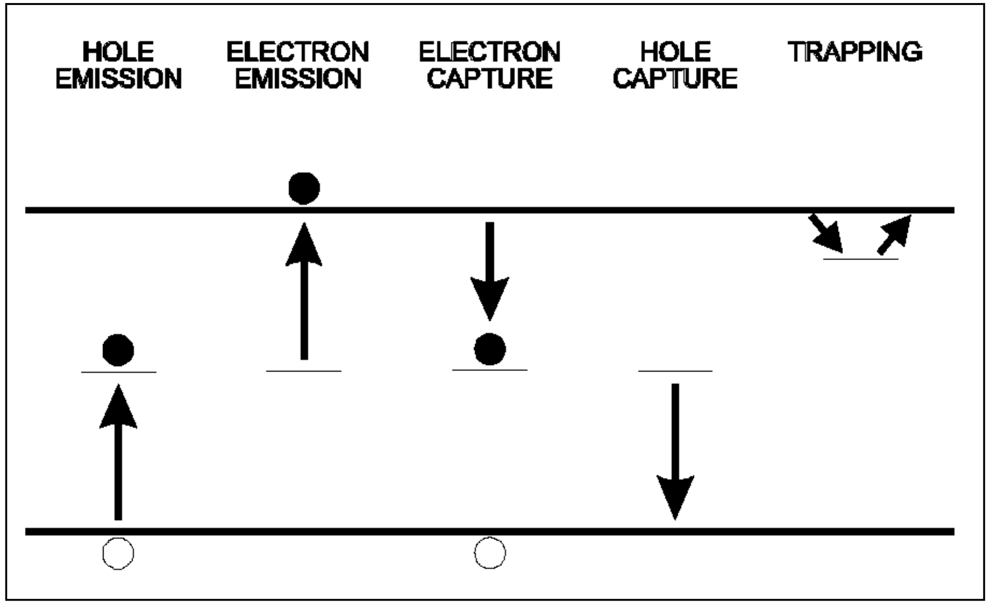
- 8900 e/h pairs/100 µm
- typical size of the charge cloud ~10 µm

Here: signal readout via Al strip, capacitively coupled to p-strip (SiO_2 in between).

(prevents large currents flowing through amplifier, but reduces collected charge.)

Effects of Radiation damage to silicon detectors

Defects in the lattice leave extra energy levels in band-gap.



These can:
- donate electron/holes
- capture electron/holes (trapping)
- increase leakage current (two-step transitions valence to conduction band)
- act as recombination centres

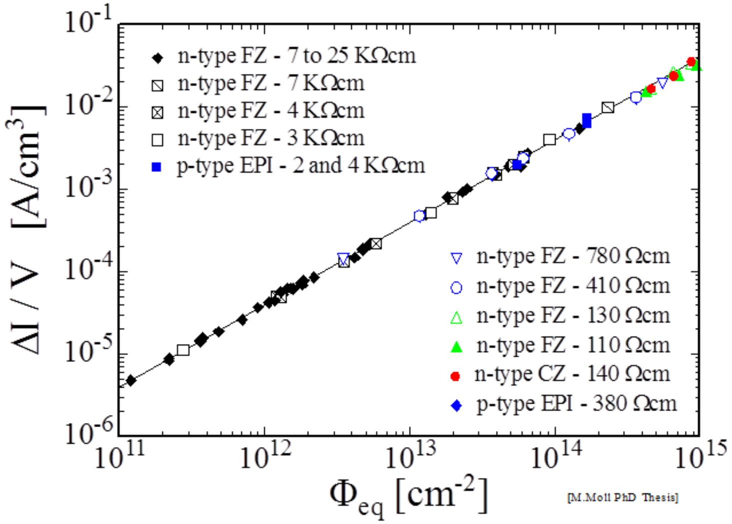
Damaging effects on Silicon detectors:
- increased leakage currents
- type-inversion (change of effective doping type)
- reduced charge collection efficiency and charge carrier mobility

Detailed behaviour depends on many factors (e.g. other impurities present)

Change of leakage current and depletion voltage

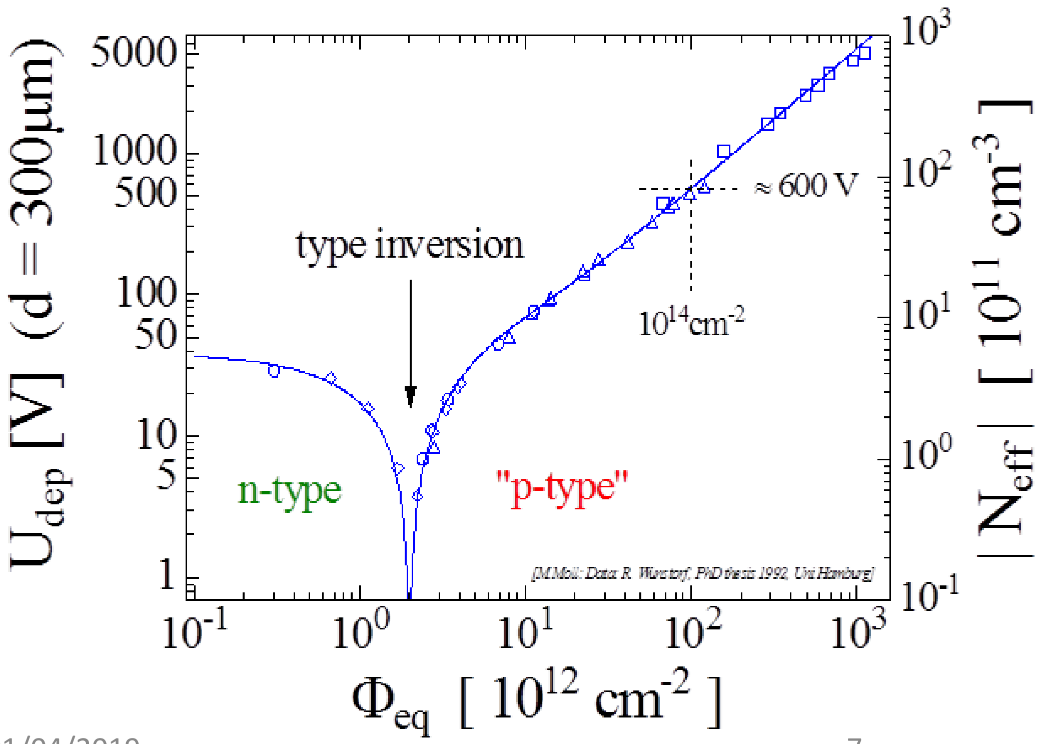
- The leakage current of a sensor, at constant temperature, increases with NIEL
- The damage parameter doesn't depends on Silicon resistivity, bulk type, fabrication technology, ...

$$\alpha = \frac{\Delta I}{V \cdot \Phi_{eq}}$$



M. Moll

Before inversion, in p-in-n sensors, the junction is on the segmented side. After inversion the junction moves to the back side.

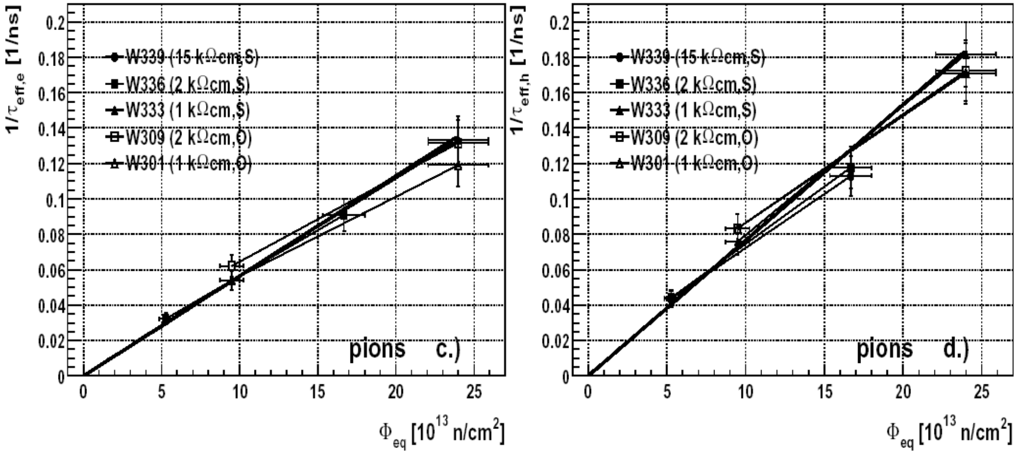


Change of charge collection efficiency

- The irradiation introduces defects which act as trapping center for the charge generated by an ionizing particle
- This reduce the overall signal thus affecting the detector efficiency

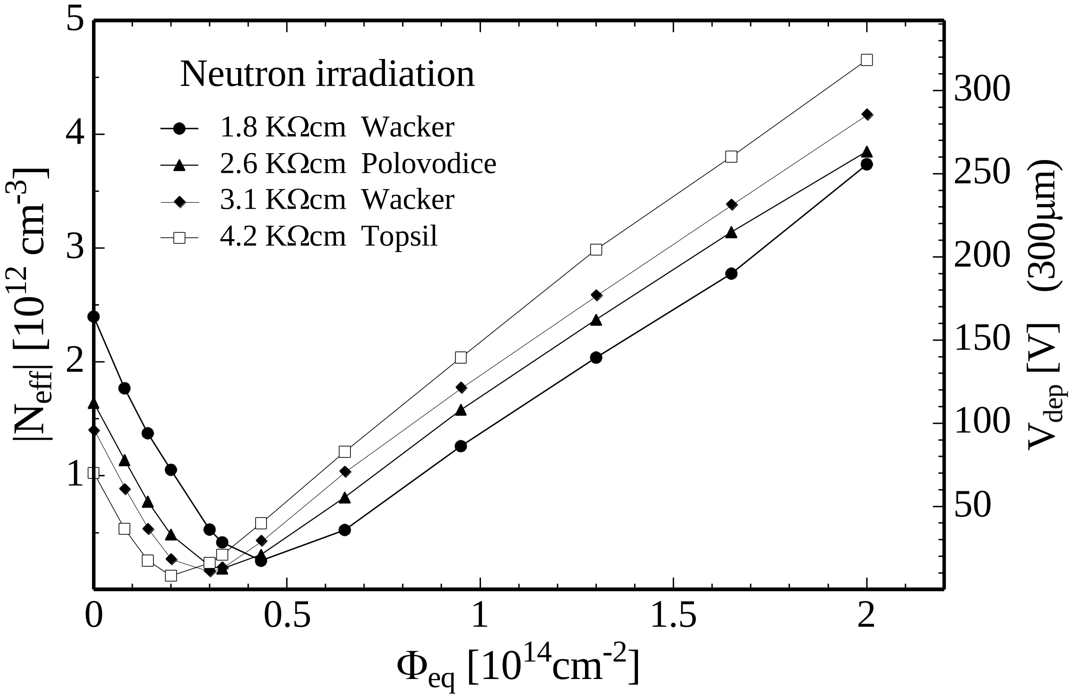
$$Q_{e,h}(t) = Q_{0_{e,h}} \exp\left(-\frac{1}{\tau_{eff\ e,h}} \cdot t \right) \qquad \frac{1}{\tau_{eff,e,h}} = \beta_{e,h}(T,t)\,\Phi_{eq}$$

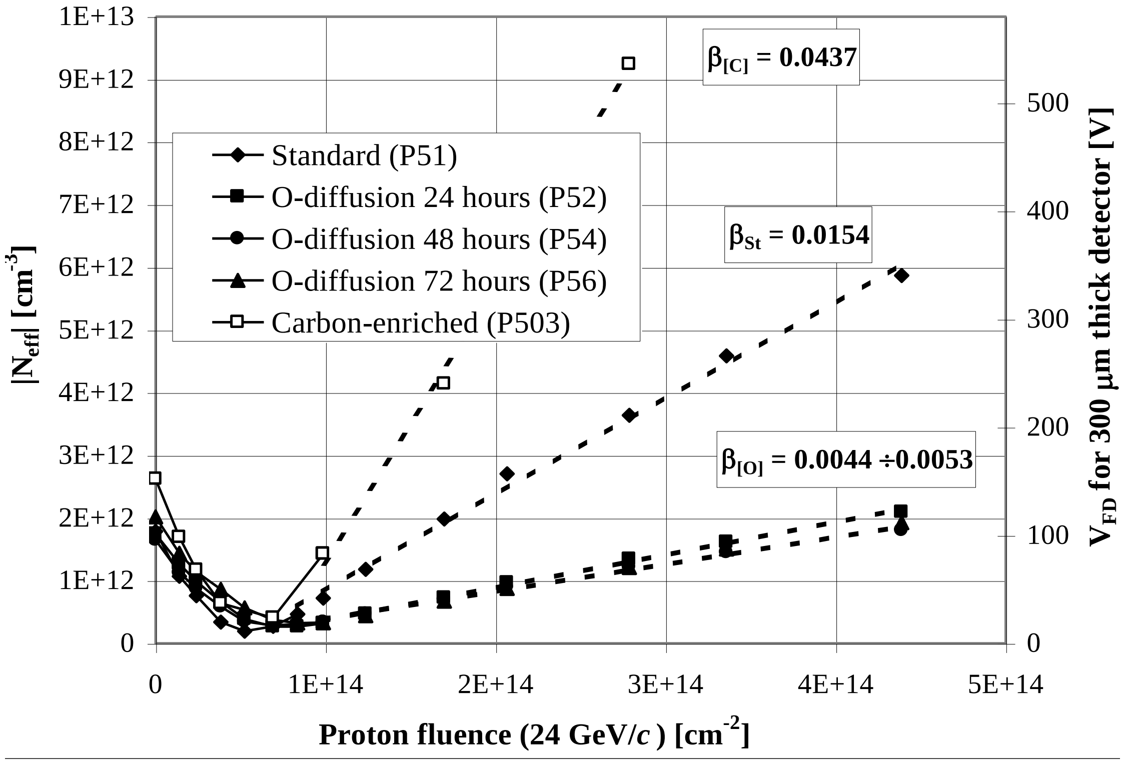
- When the effective trapping time becames of the order of the electron/hole drift time (5-20ns) the charge integrated at the electrodes by the front-end electronics is reduced



Radiation tolerance prediction: "old" method

What metric do we use for assessing the radiatione tolerance of a given sensor?



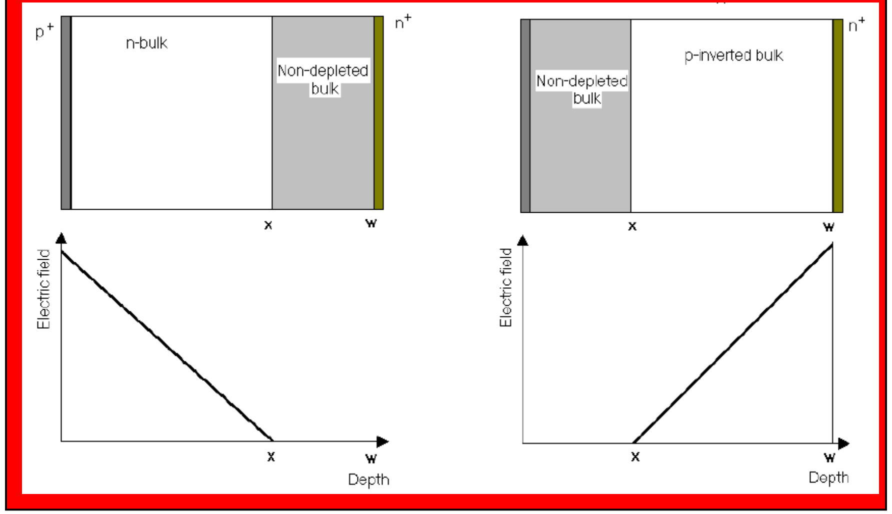


"Good" operation of sensors was based on the ability to provide a bias voltage corresponding to 120-130% of the full depletion voltage. But the VFD would be well over 10000V at HL-LHC doses ....

Under-depleted detectors

p-strips in n-bulk detector (p-in-n)

before irradiation after irradiation

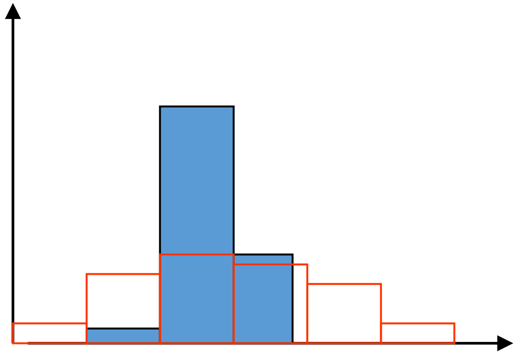


Undepleted region acts like an ohmic resistor.

- no effective conduction
- no/weak field to collect charge to the nearest strip (relying on diffusion)

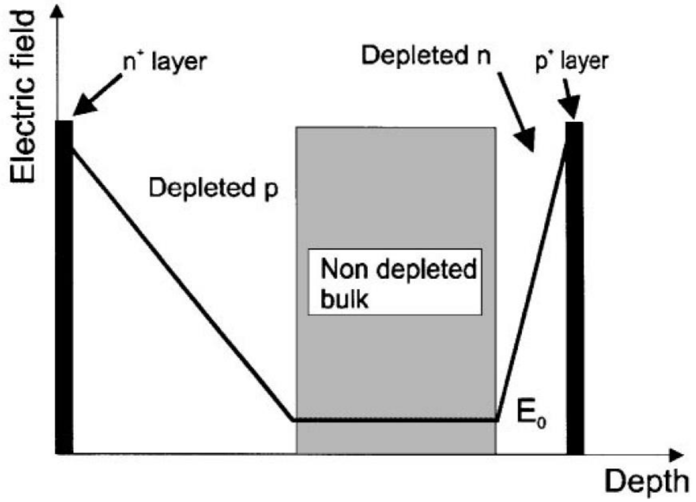
If detector is partially depleted:

- near the strip side
  - ⇒ only charge in depleted region contributes
  - ⇒ smaller signal, same spatial resolution
- near the backplane
  - ⇒ carriers travel towards strips, but don’t reach it
  - ⇒ signal spread over many strips
  - ⇒ poor spatial resolution



N-side read-out better for irradiated devices. Can we estimate the effect of charge trapping on the signal?

Schematic changes of Electric field after irradiation



There is electric field throughout the detector, undepleted bulk is not a correct statement after significant irradiation.

Effect of trapping on the Charge Collection Efficiency (CCE)

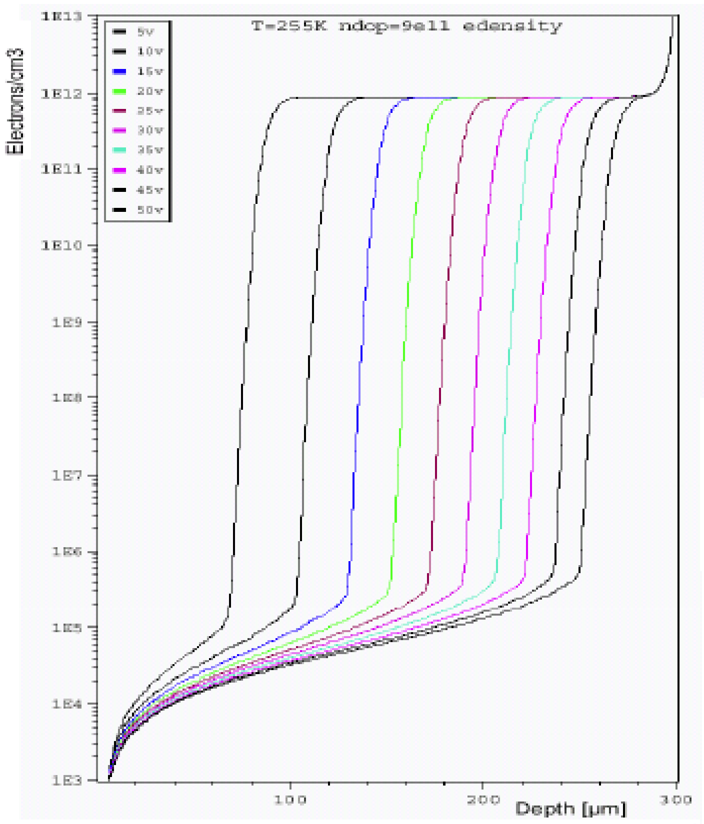
$$Q_{tc} \cong Q_0 \exp(-t_c/\tau_{tr}),\ 1/\tau_{tr} = \beta\Phi.$$

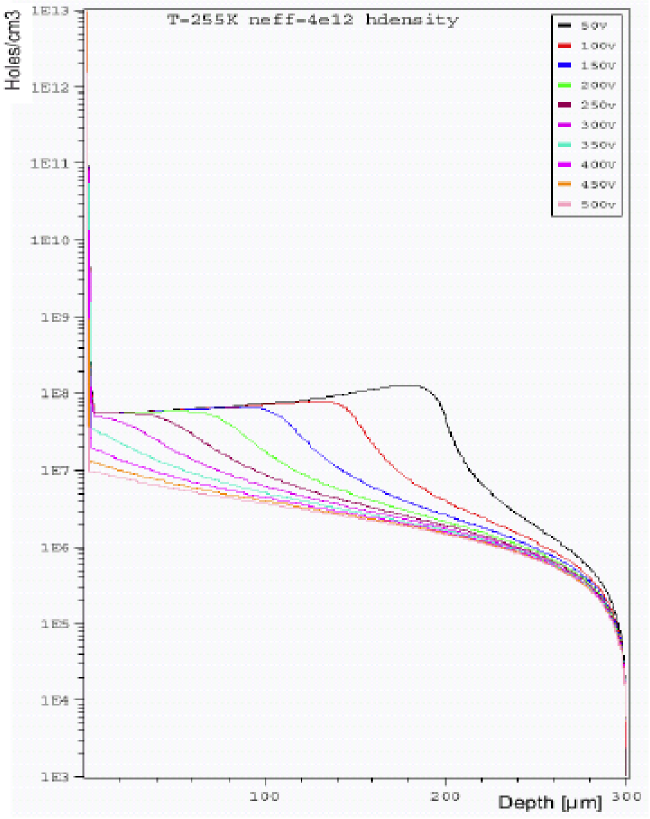
Collecting electrons provide a sensitive advantage with respect to holes due to a much shorter t_c. P-type detectors are the most natural solution for *e* collection on the segmented side.

N-side read out to keep lower t_c

The simplified approached of VFD does not hold for high radiation levels

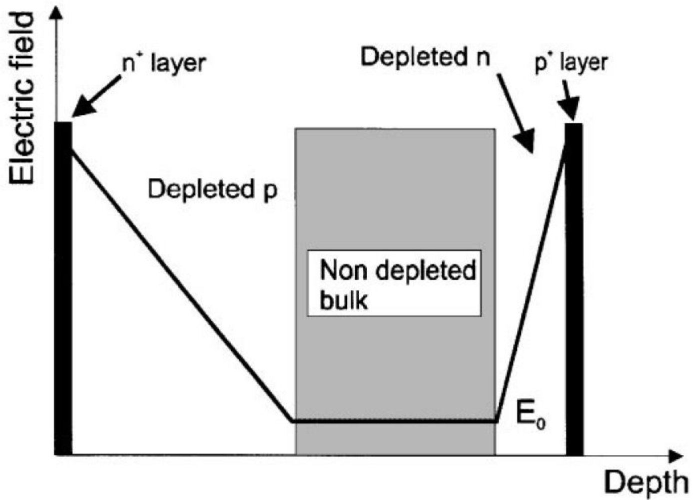
Majority carrier concentration at different bias voltages. Unirradiated sensors





After 2E14 n_{eq} cm^{-2}

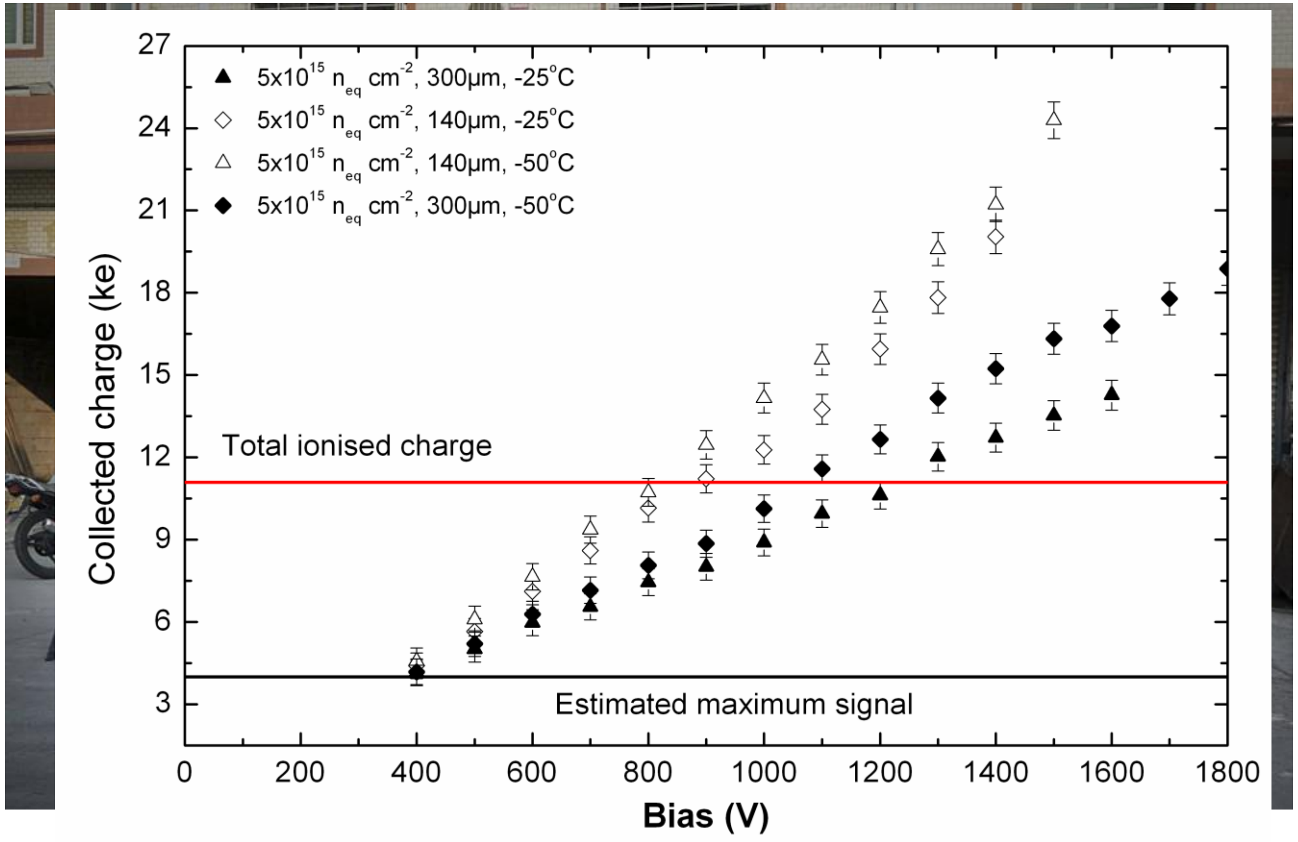
There is electric field throughout the detector, undepleted bulk is not a correct statement after significant irradiation.



G. Casse et al. / Nuclear Instruments and Methods in Physics Research A 512 (2003) 60–70

RD50 Charge multiplication

Some times, things go better than planned, a good day out fishing ....

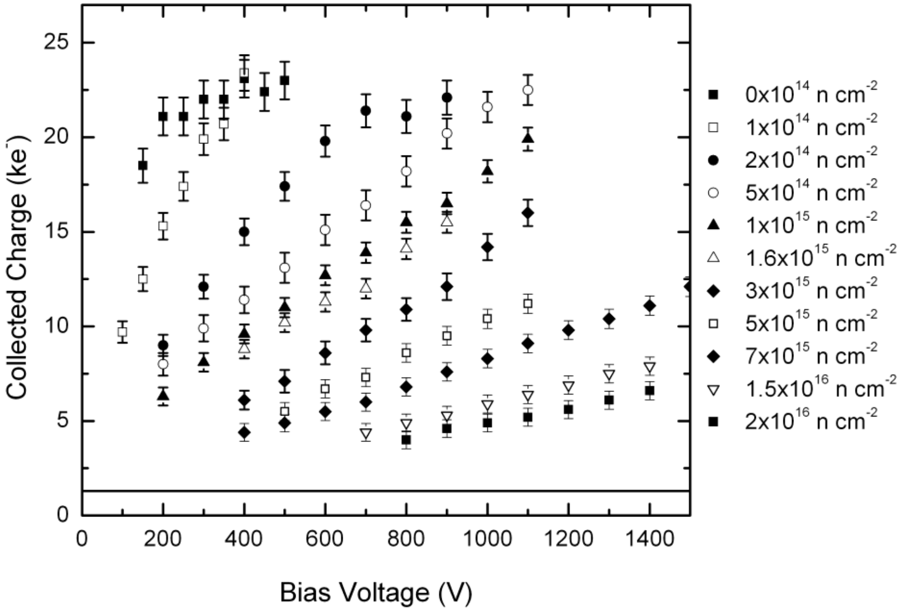


G. Casse, A. Affolder, P.P. Allport, H. Brown, I. McLeod, M. Wormald "Evidence of enhanced signal response at high bias voltages in planar silicon detectors irradiated up to 2.2x10^{16} n$_{eq}$ cm^{-2} ", NIMA Vol. 636 (2011).

Or more charge than you expect after irradiation ....

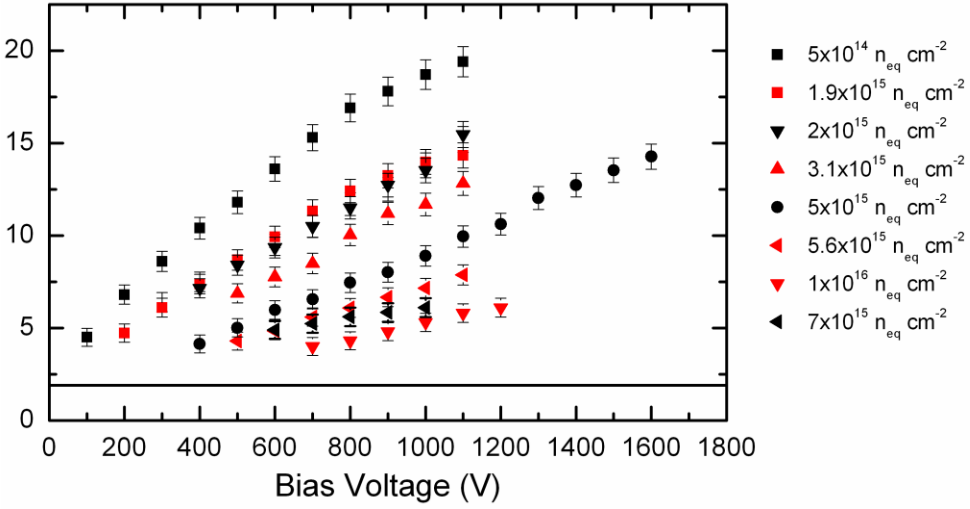
Results with proton irradiated 300 μm n-in-p Micron sensors (up to 1x10^{16} n$_{eq}$ cm^{-2})

Irradiated with reactor neutrons

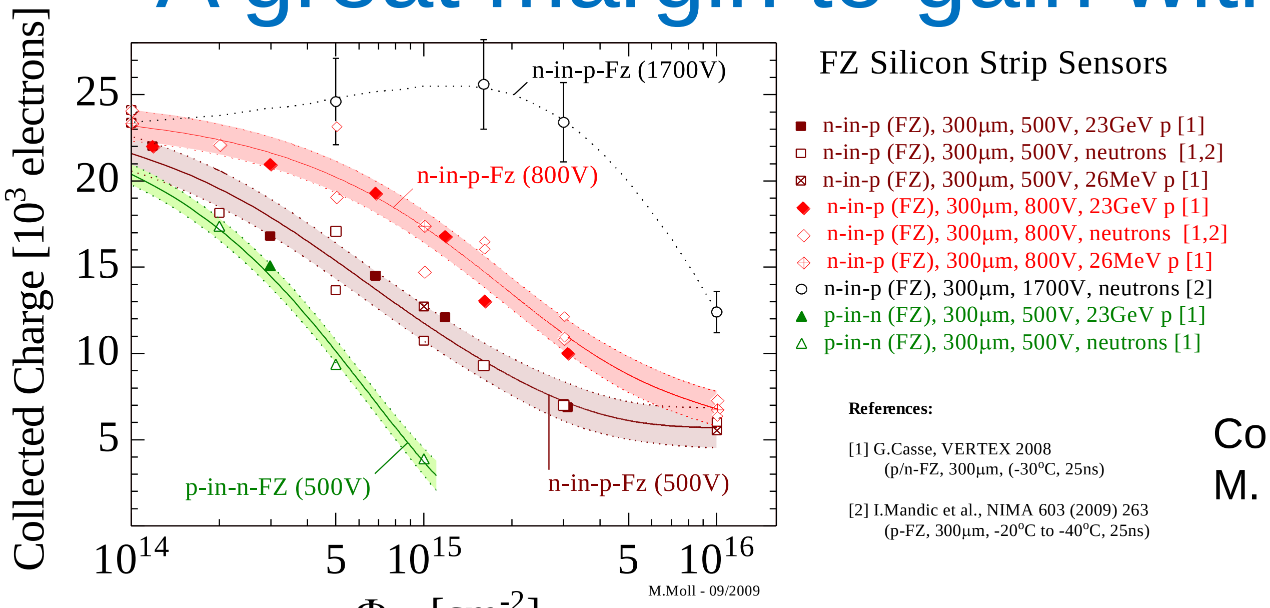


RED: irradiated with 24GeV/c protons

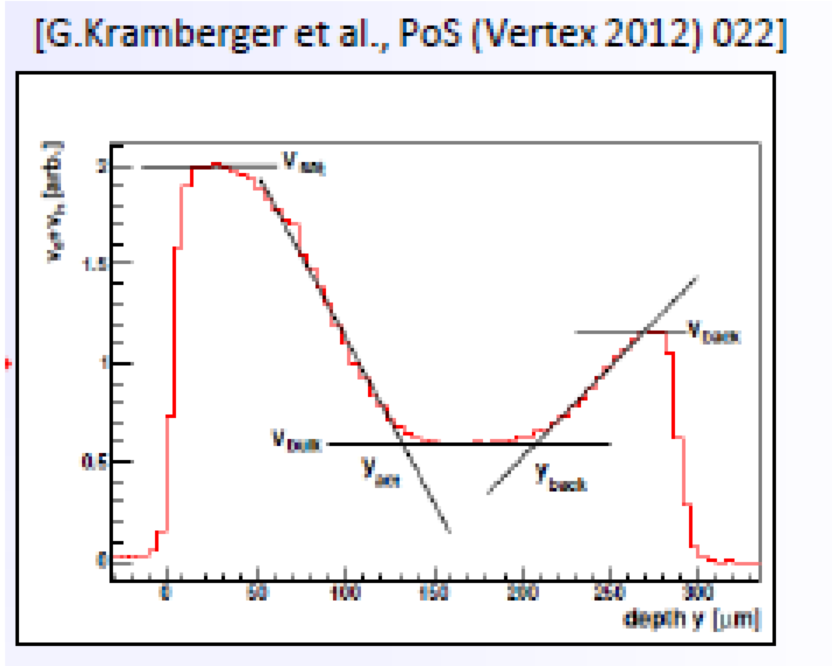
Other: 26MeV protons



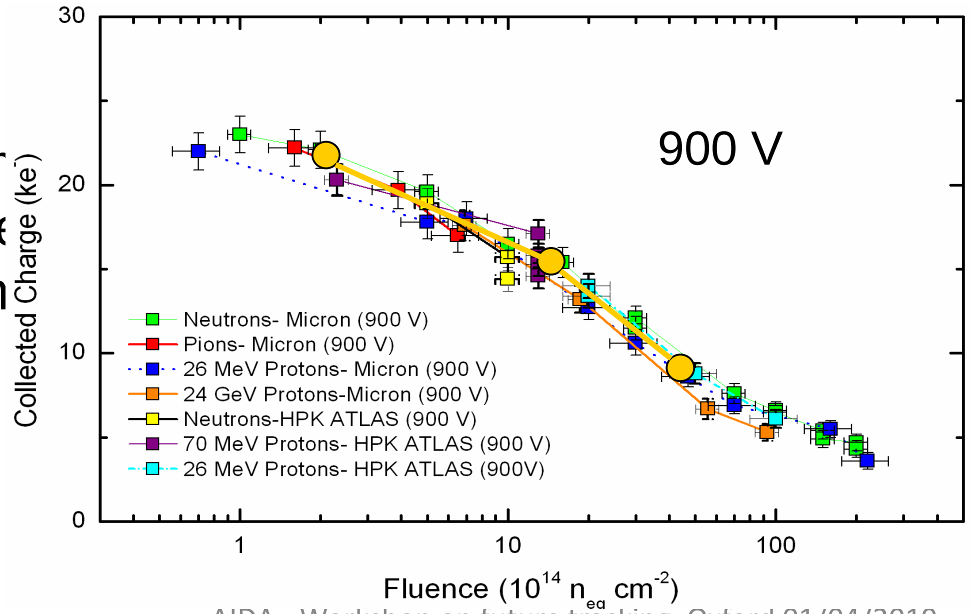
A great margin to gain with extremely high voltage



Compiled by
M. Moll

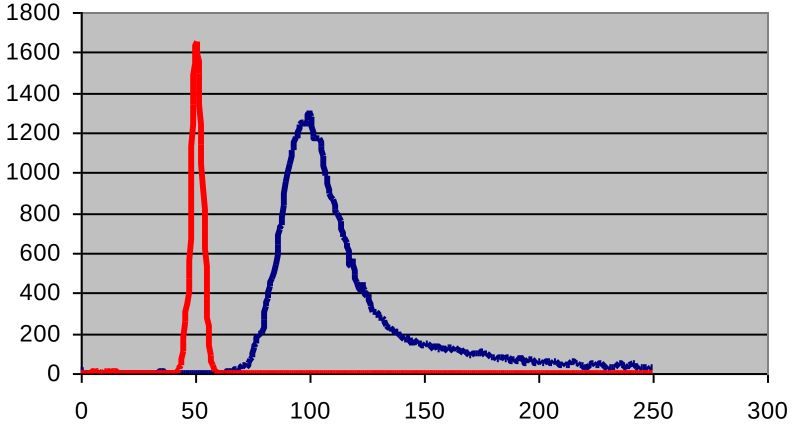

[G.Kramberger et al., PoS (Vertex 2012) 022]

..but good agreement ar
measurements from diffe
groups and sensors fron
different manufacturers



… and at the end of the day a good metric is S/N

We have learned that a signal exceeding 4000 e$^-$ can be extracted from planar sensors irradiated to 2E16 n_{eq} cm^{-2}, if we make this enough we achieve phenomenally high radiation tolerance.
Lets say, with S/N > 5 (ENC < 800).
Typically, highly segmented hybrid sensors exhibit ENC ranging from 300 to 1500 e$^-$.



Mitigation of sensor degradation

One essentially needs:

- Very high Electric field (voltage)
- Low noise

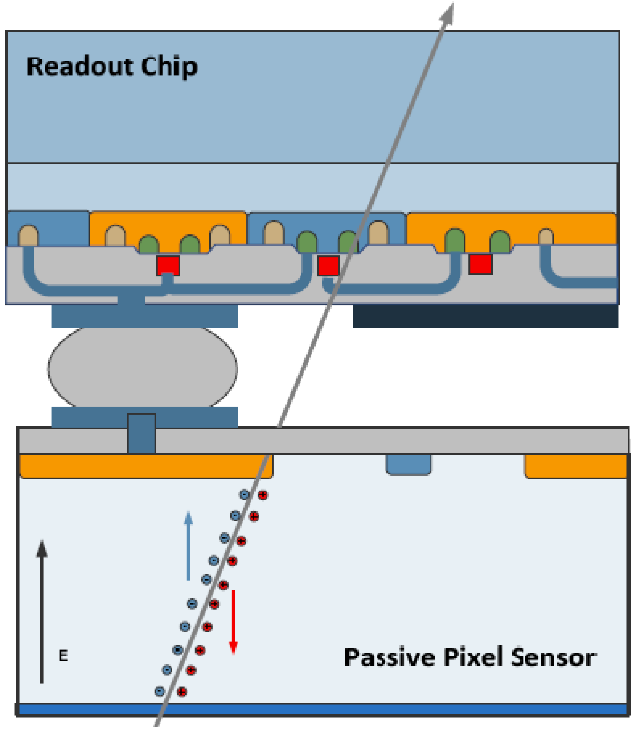
Parameters: Sensor geometry, operation conditions (cooling)

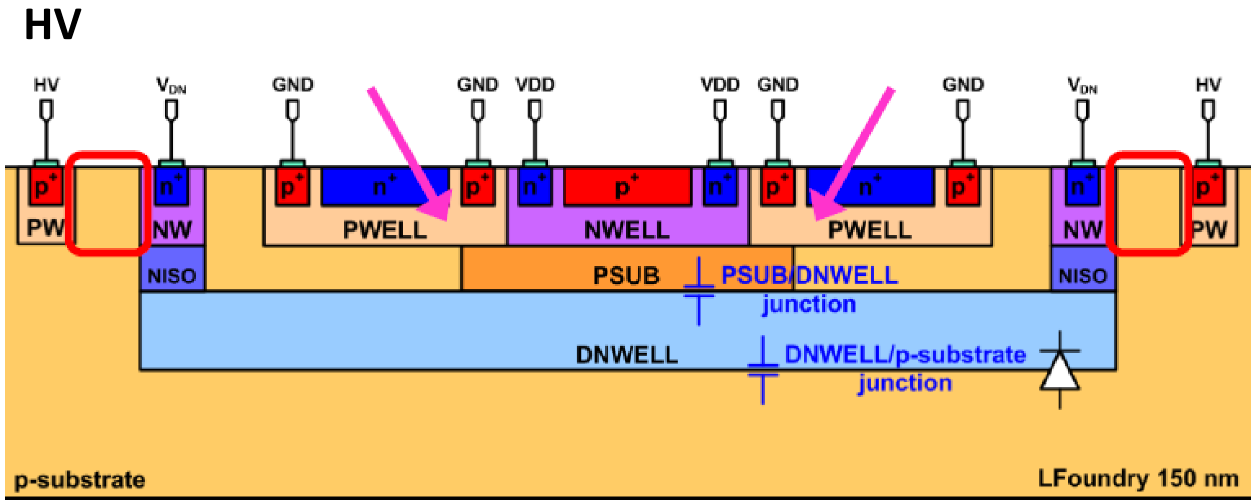
Parameters: Sensor geometry, operation conditions (cooling), electronics

At intermediate radiation damage one can play other tricks:

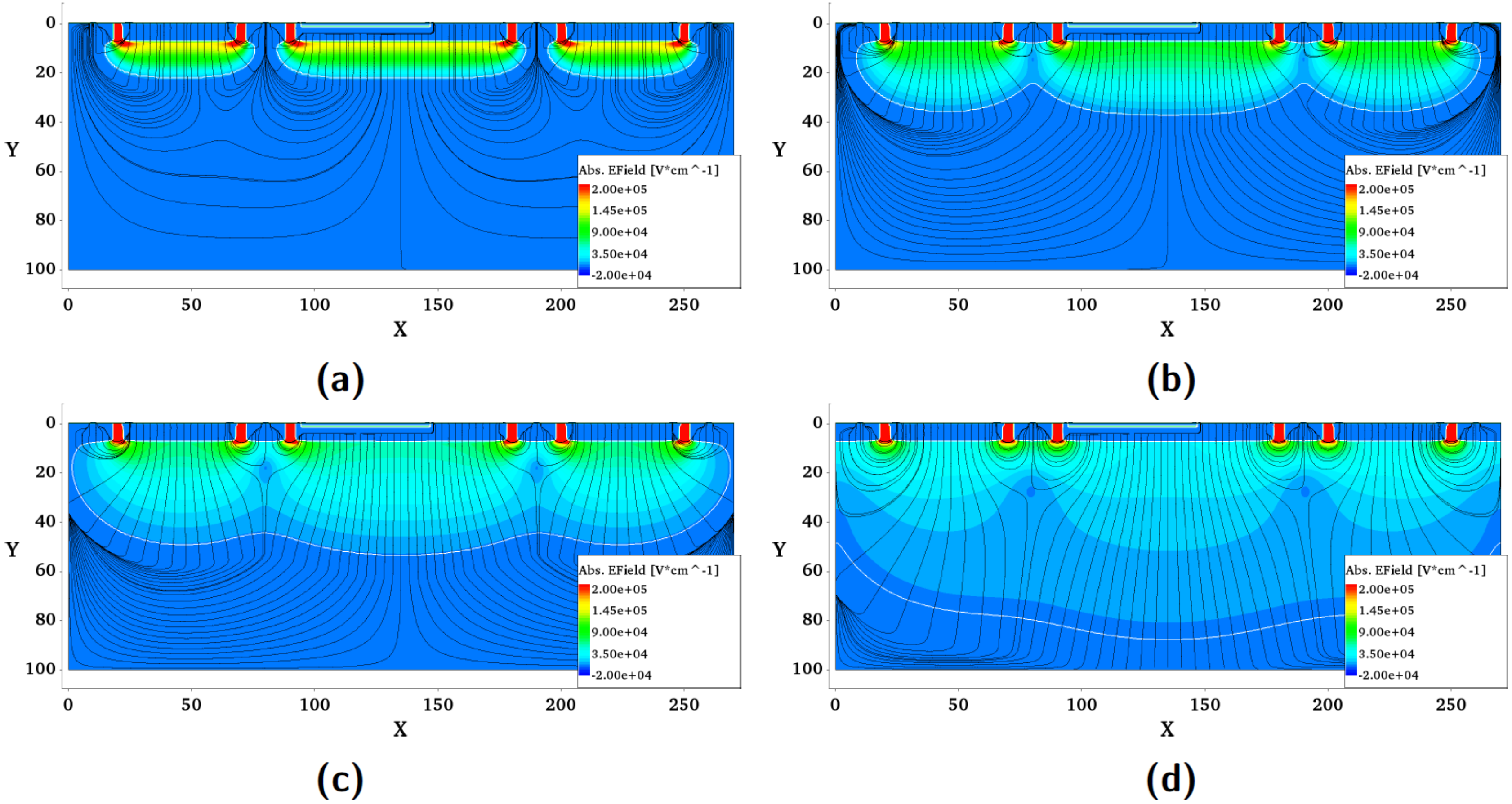
Choice of bulk resistivity
Choice of bulk type (impurity content)

Applying High Voltage to D-CMOS





Applying High Voltage to D-CMOS: Top biasing



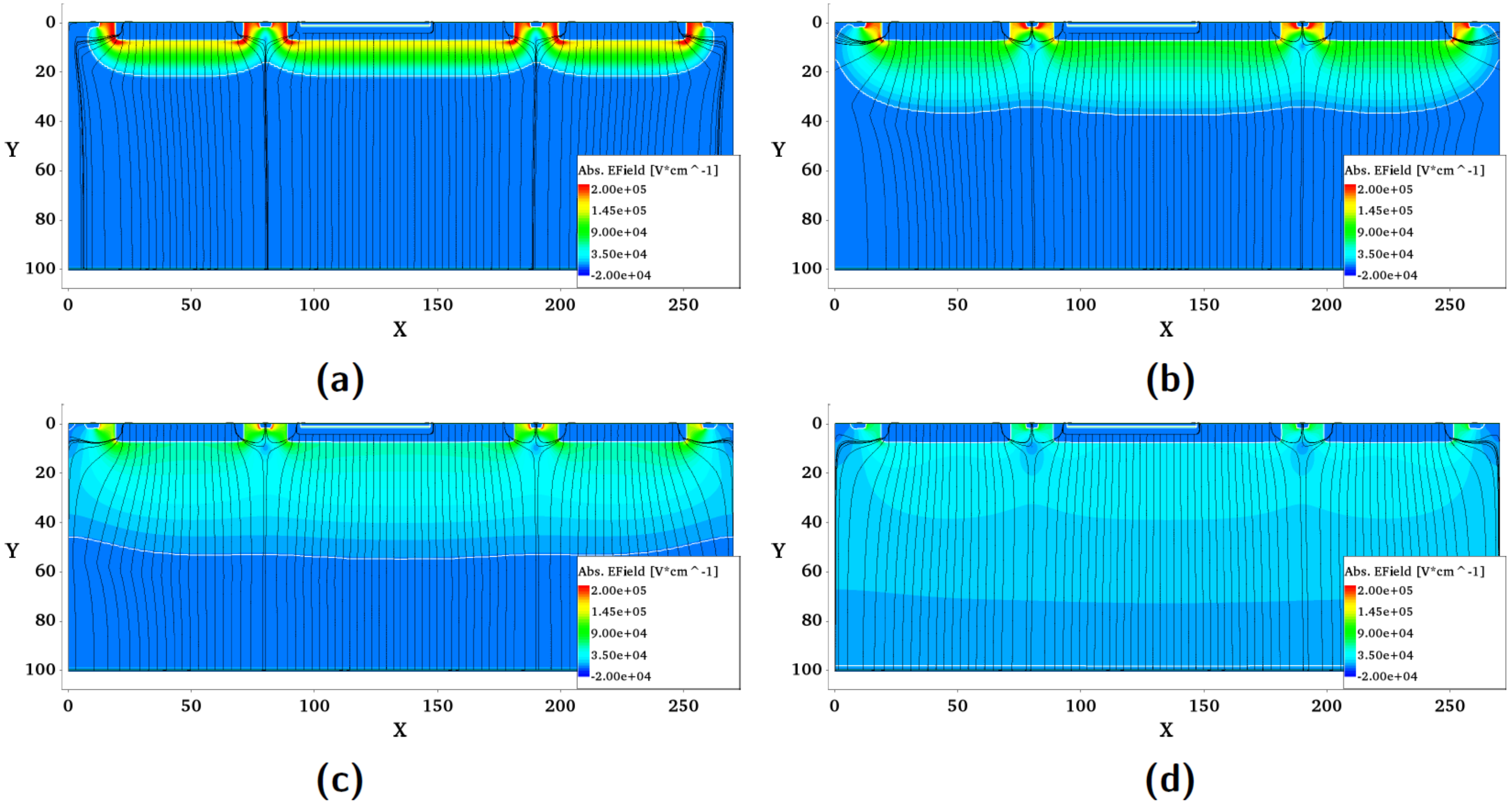
(a) (b)

(c) (d)

Figure 5.8: Absolute electric field strength of H35DEMO for resistivities 20 (a), 80 (b), 200 (c) and 1000 Ωcm (d), biased from the top at −120 V for the standard layout.

From Lingxin Meng PhD thesis.

Applying High Voltage to D-CMOS: Backside biasing

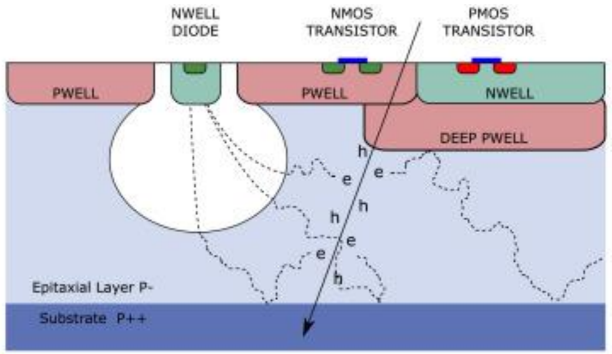


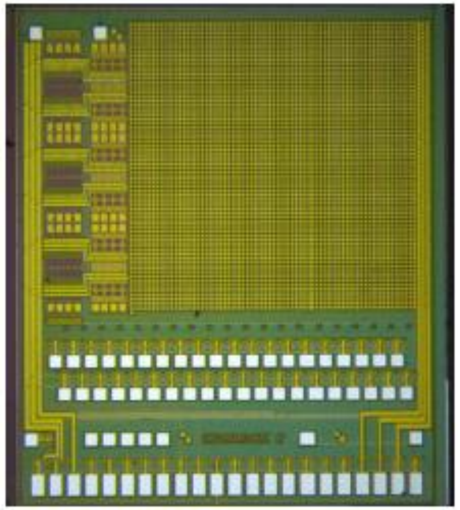
From Lingxin Meng PhD thesis.

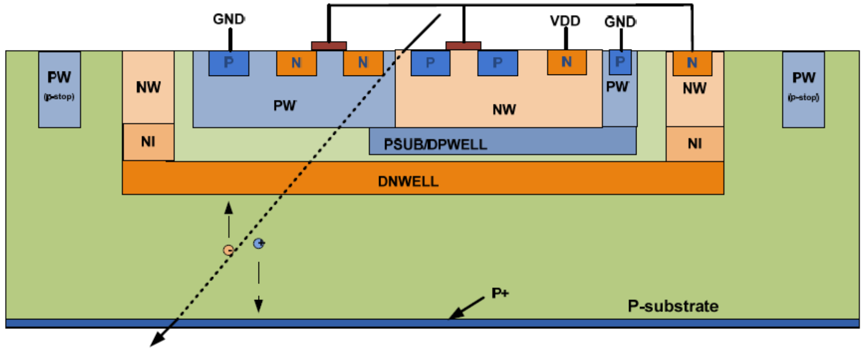
Figure 5.10: Absolute electric field strength of H35DEMO for resistivities 20 (a), 80 (b), 200 (c) and 1000 Ωcm (d), biased from the back at −120 V for the standard layout with back side process.

It is possible, with careful design, to apply HV to D-CMOS devices

How do D-CMOS compare to hybrid detectors for noise?







ALPIDE ~< 10 e^- noise
ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade, M. Mager et al., NIM A Volume 824, 11 July 2016, Pages 434-438

Typically, with monolithic HV-CMOS, can achieve a < 60 e^- equivalent noise charge.

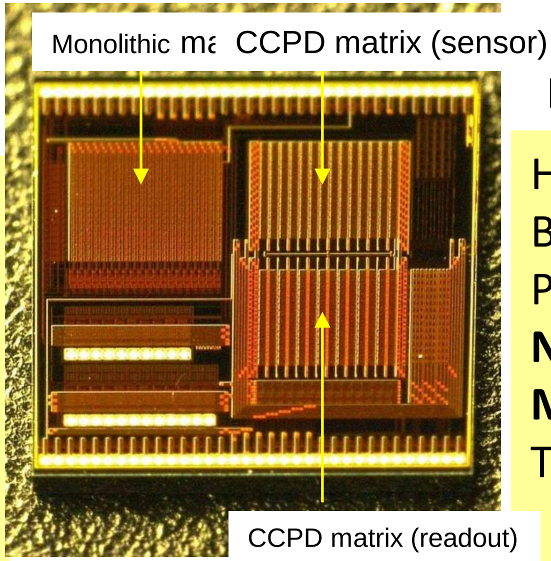
How do D-CMOS compare to hybrid detectors for noise?

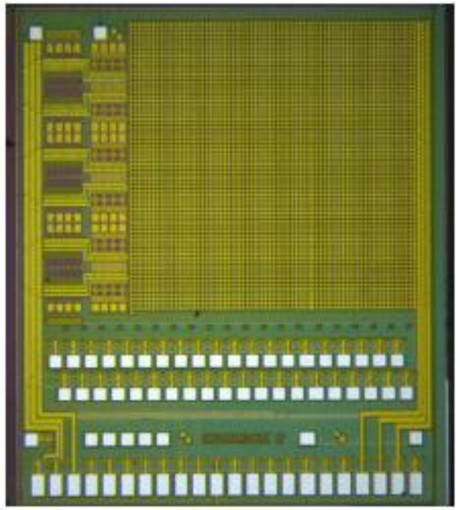
Capacitive coupled hybrid detector

CCPD1 - **capacitive coupled pixel detector**
Pixel size 55x55µm
Noise 70e
Time resolution <100ns
MIP SNR 25

CCPD2 (CAPPIX) - **capacitive coupled pixel detector**
Pixel size 50x50µm
Noise 30-40e
Time resolution <300ns
MIP SNR 45-60

Irradiations of test pixels
60MRad – MIP SNR 22 at 10C (CCPD1)
$10^{15}n_{eq}$ MIP SNR 50 at 10C (CCPD2)
Technology 350nm HV – substrate 20 Ωcm uniform





Monolithic detector - frame readout

HVPixel – **CMOS in-pixel electronics with hit detection**
Binary RO
Pixel size 55x55µm
Noise 60e
MIP seed pixel signal 1800 e
Time resolution <100ns

HVPixelM chip - frame mode readout
Pixel size 21x21µm
4 PMOS pixel electronics
128 on-chip ADCs
Noise: 21e (lab) - 44e (test beam)
MIP signal - cluster: 2000e/seed: 1200e
Test beam: **Detection efficiency >98%**
- **Seed Pixel SNR ~ 27**
- Cluster signal/seed pixel noise ~ 47
- **Spatial resolution ~ 3 µm**

A few results with D-CMOS

Other relevant metrics!

Non irradiated sensor for mu3e.

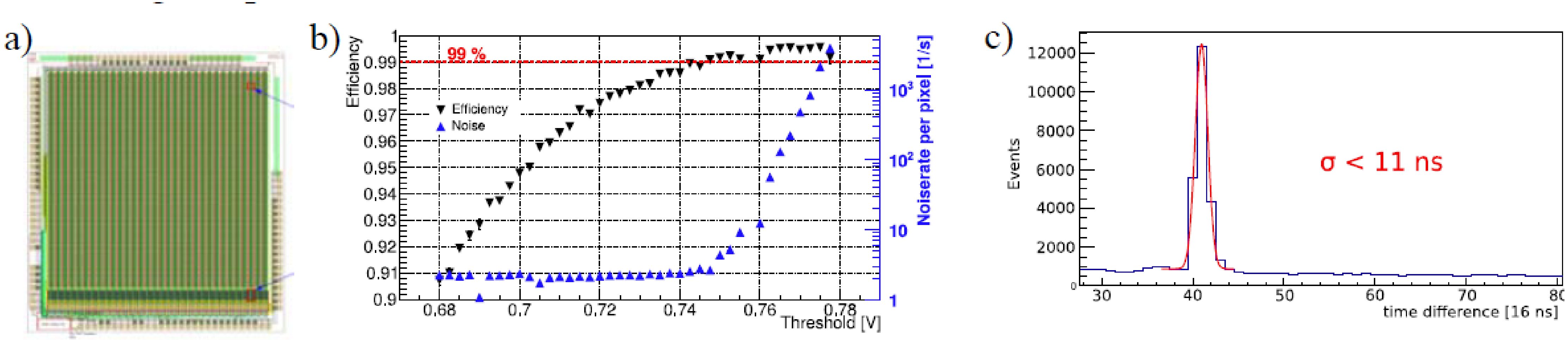


Figure 10 Layout of a) the MuPix7 chip and its measured performance b) hit detection efficiency and c) time stamping resolution (from [12]).

Radiation hardening of D-CMOS

M. Benoit et al., Characterization Results of a HVCMOS Sensor for ATLAS, NIMA

Max irradiation 5e15 n_{eq} cm^{-2}.

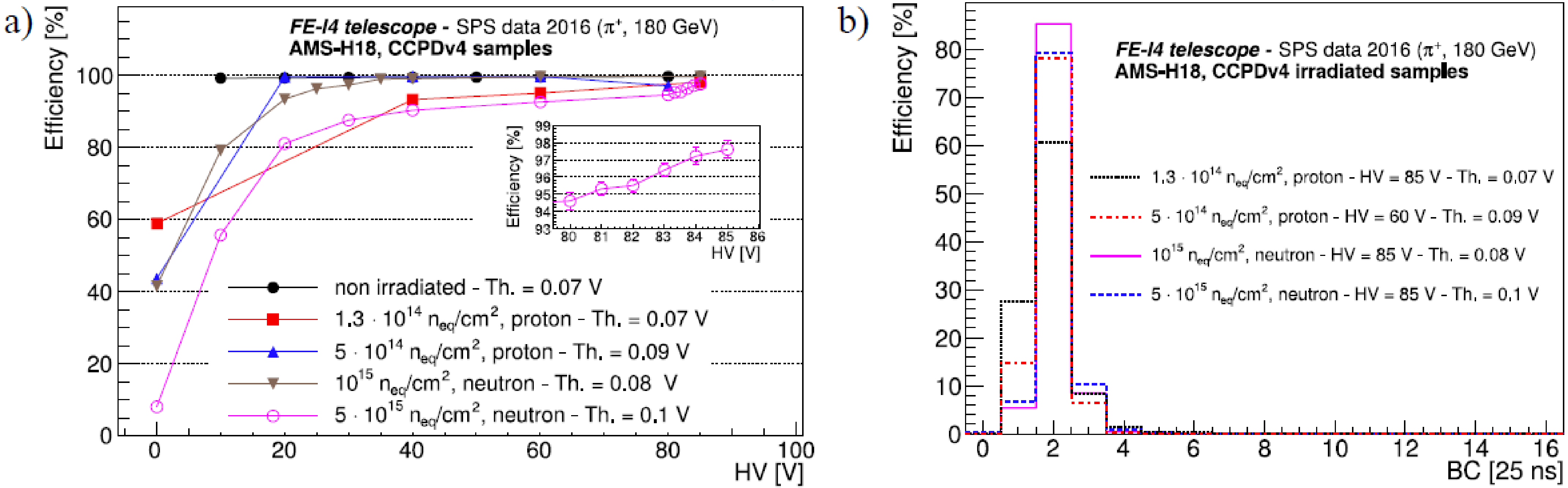
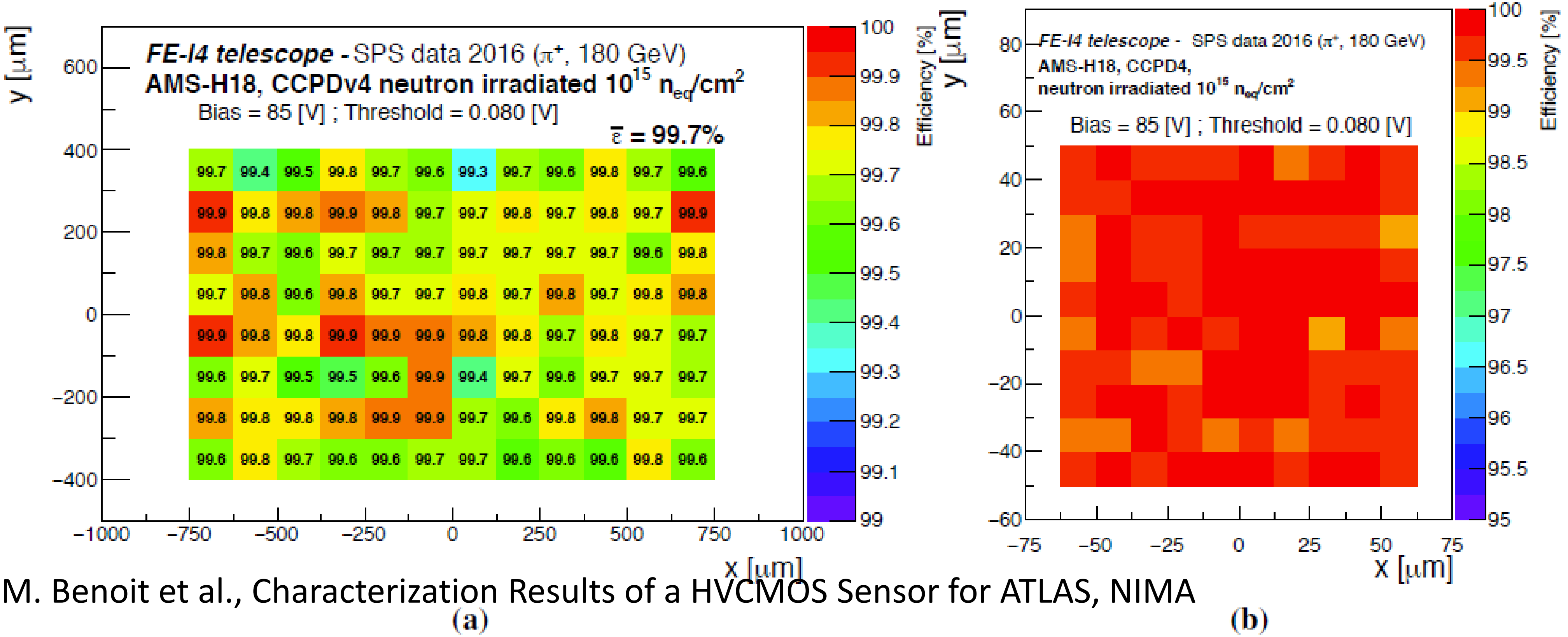


Figure 11 The measurement results of CCPDv4 devices a) track detection efficiency for different neutron dose, threshold and bias b) time stamping resolution (from [14])

M. Benoit et al., Test beam measurement of ams H35 HV-CMOS capacitively coupled , JINST 13 (2018) no.12, P12009

Radiation hardening of D-CMOS



99.7	99.4	99.5	99.8	99.7	99.6	99.3	99.7	99.6	99.8	99.7	99.6
99.9	99.8	99.8	99.9	99.8	99.7	99.7	99.8	99.7	99.8	99.7	99.9
99.8	99.7	99.6	99.7	99.7	99.7	99.7	99.7	99.7	99.7	99.6	99.8
99.7	99.8	99.6	99.8	99.7	99.7	99.8	99.7	99.8	99.7	99.8	99.8
99.9	99.8	99.8	99.9	99.9	99.9	99.8	99.8	99.7	99.8	99.7	99.7
99.6	99.7	99.5	99.5	99.6	99.9	99.4	99.7	99.6	99.7	99.7	99.7
99.8	99.8	99.8	99.8	99.9	99.9	99.7	99.6	99.8	99.8	99.7	99.7
99.6	99.8	99.7	99.6	99.6	99.7	99.7	99.6	99.6	99.6	99.8	99.6

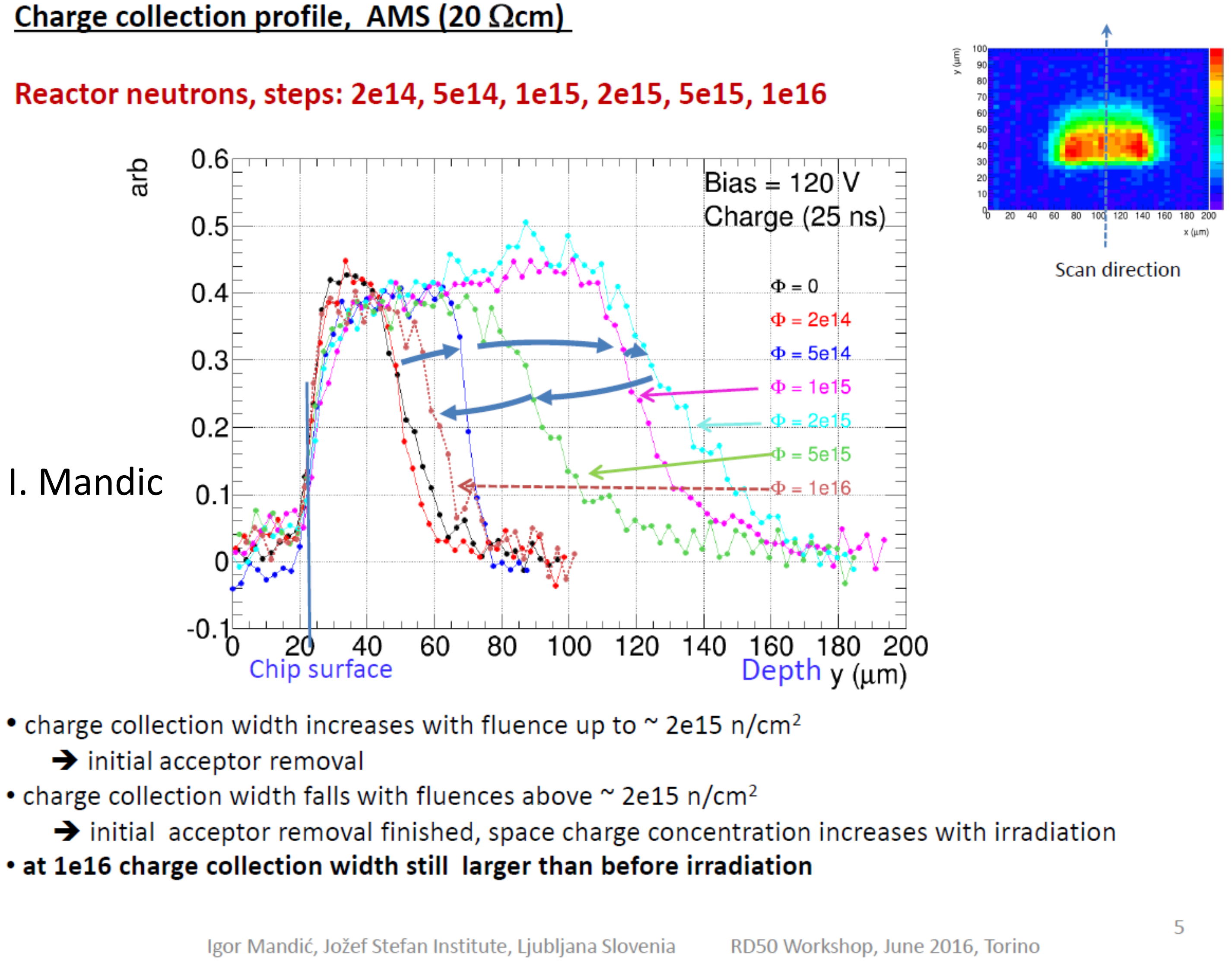
M. Benoit et al., Characterization Results of a HVCMOS Sensor for ATLAS, NIMA

(a) (b)

Figure 5. a) Hit efficiency map for CCPDv4 neutron-irradiated with 1×10^{15} n_{eq}/cm^2; the colour scale is only ranging from 99% to 100%. b) Sub-pixel hit efficiency map overlaid from all central pixels. No significant efficiency loss is visible in any region of the pixel. The threshold of 80 mV is assumed to be equivalent to 690 e^- according to [11].

M. Benoit et al., Test beam measurement of ams H35 HV-CMOS capacitively coupled , JINST 13 (2018) no.12, P12009

Radiation hardening of D-CMOS



Charge collection profile, AMS (20 Ωcm)

Reactor neutrons, steps: 2e14, 5e14, 1e15, 2e15, 5e15, 1e16

Scan direction

I. Mandic

- charge collection width increases with fluence up to ~ 2e15 n/cm^2
  - ➔ initial acceptor removal
- charge collection width falls with fluences above ~ 2e15 n/cm^2
  - ➔ initial acceptor removal finished, space charge concentration increases with irradiation
- **at 1e16 charge collection width still larger than before irradiation**

5

Igor Mandić, Jožef Stefan Institute, Ljubljana Slovenia RD50 Workshop, June 2016, Torino

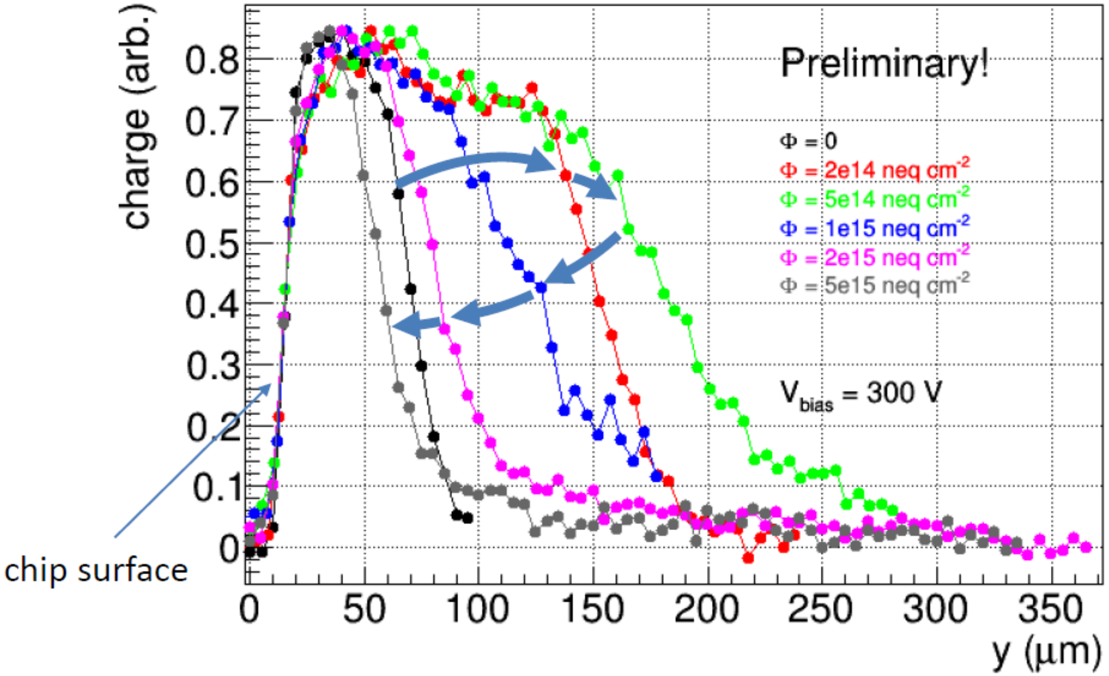
Some consequence of the relatively low resistivity of CMOS wafer substrates. It can impact on sensor performance at low/intermediate irradiation levels.

Radiation hardening of D-CMOS

Charge collection profile, Xfab (100 Ωcm)

Reactor neutrons, fluence steps: 2e14, 5e14, 1e15, 2e15, 5e15

I. Mandic



Some consequence of the relatively low resistivity of CMOS wafer substrates. It can impact on sensor performance at low/intermediate irradiation levels.

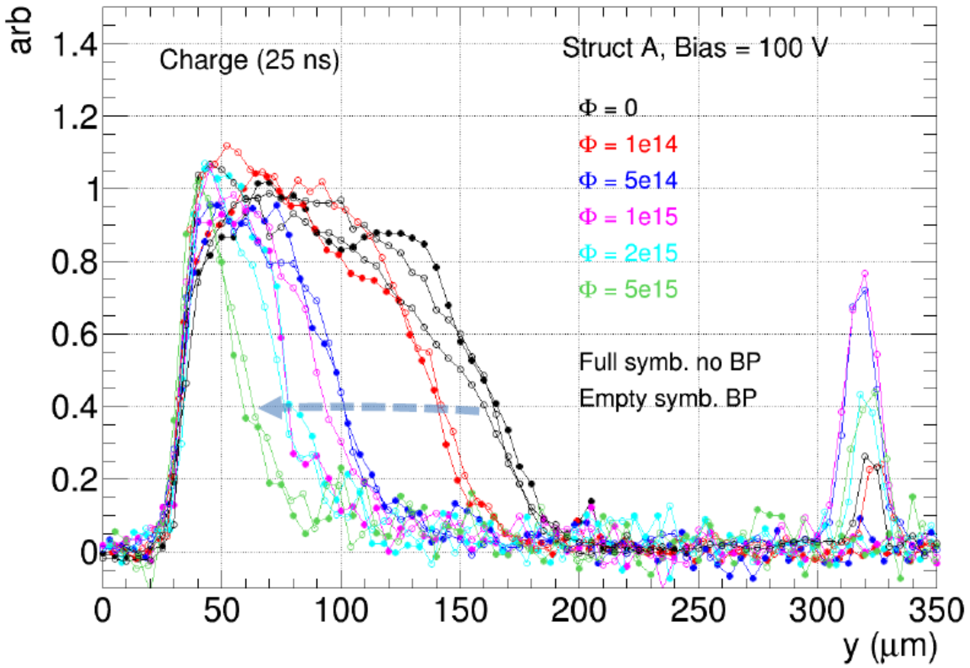
- large increase of charge collection region at lower fluence than AMS
- at 5e15 charge collection region narrower than before irradiation, but still 40 µm at 300 V

Radiation hardening of D-CMOS

Charge collection profile, LFoundry (2000 Ωcm)

Reactor neutrons, fluence steps: 1e14, 5e14, 1e15, 2e15, 5e15

I. Mandic

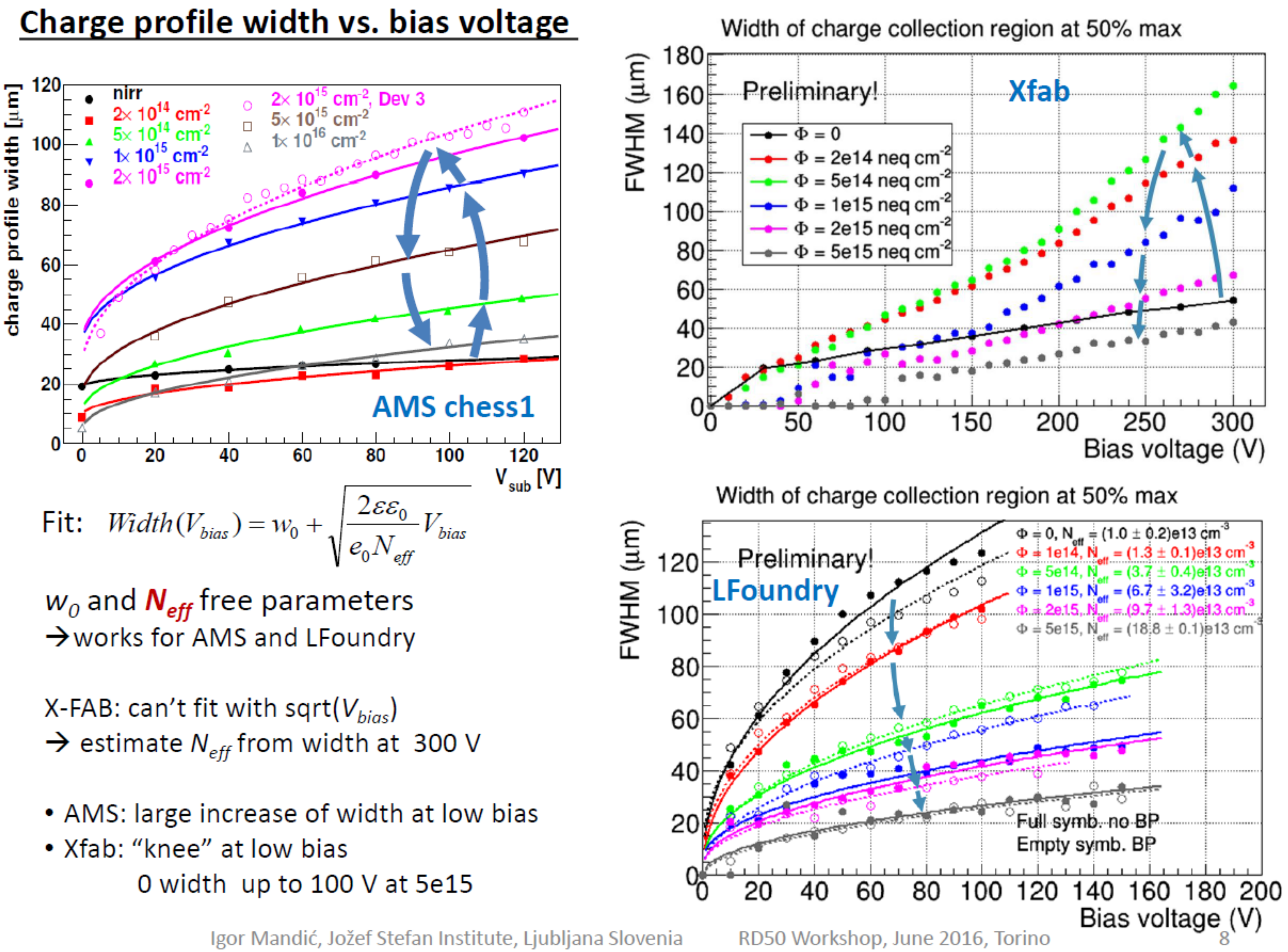


- no increase of charge collection width after irradiation seen
- no significant difference between samples with and without back plane (BP)

Some consequence of the relatively low resistivity of CMOS wafer substrates. It can impact on sensor performance at low/intermediate irradiation levels.

Radiation hardening of D-CMOS

I. Mandic



Charge profile width vs. bias voltage

Fit: $Width(V_{bias}) = w_0 + \sqrt{\frac{2\varepsilon\varepsilon_0}{e_0 N_{eff}} V_{bias}}$

w_0 and N_{eff} free parameters

→works for AMS and LFoundry

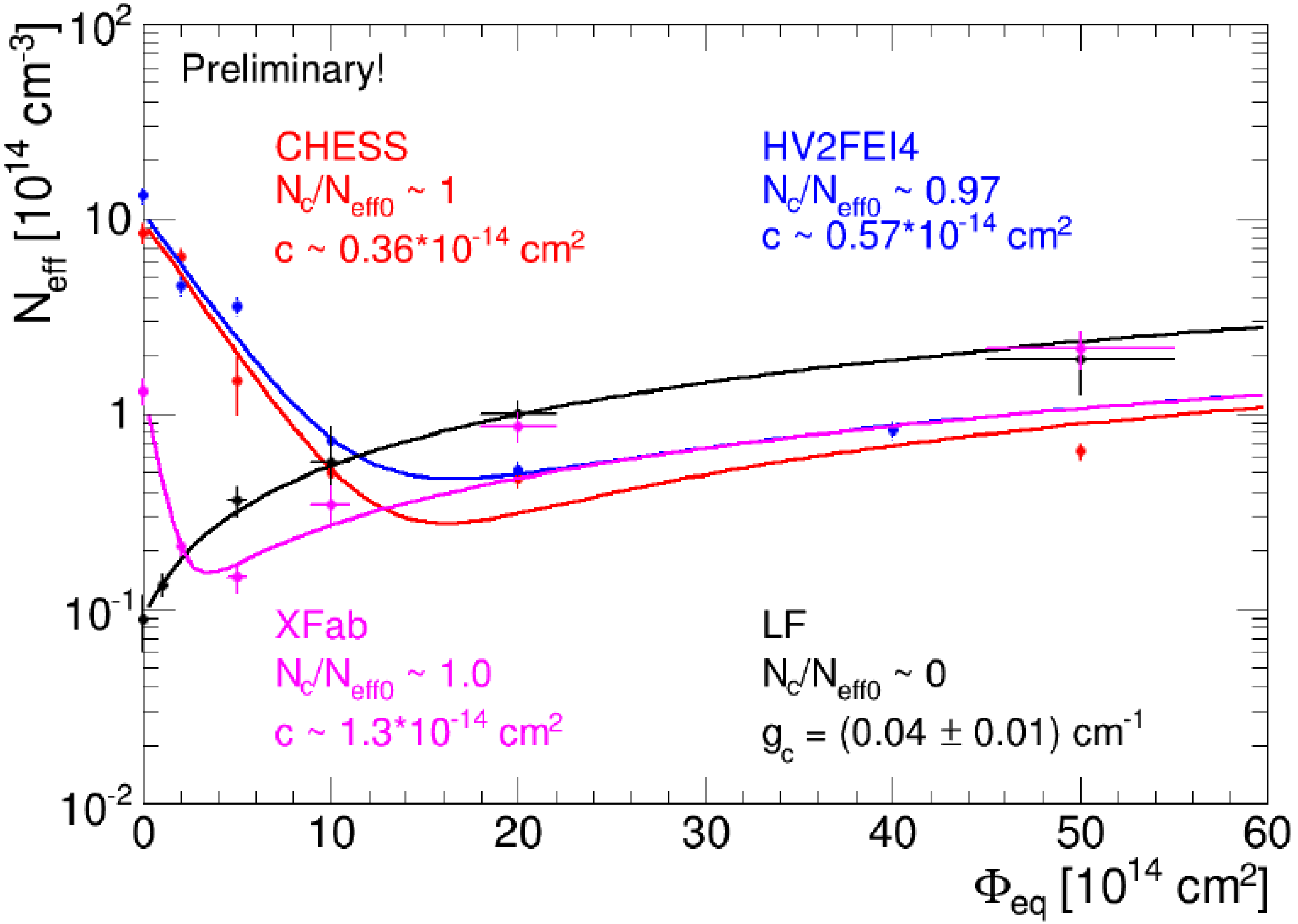
X-FAB: can't fit with sqrt(V_{bias})

→ estimate N_{eff} from width at 300 V

- AMS: large increase of width at low bias
- Xfab: "knee" at low bias
  0 width up to 100 V at 5e15

Igor Mandić, Jožef Stefan Institute, Ljubljana Slovenia RD50 Workshop, June 2016, Torino 8

Radiation hardening of D-CMOS



AMS

(CHESS and HV2FEI4)

from:

G. Kramberger et al.,

2016 *JINST11 P04007*

SUMMARY

- D-CMOS can be designed, with careful crafting of their geometry, with the ability of sustaining significantly high bias voltage, especially with the backplane bias option.
- D-CMOS can show ENC smaller than 50 e^-, retaining therefore good S/N also after high hadron radiation fluences.
- Results are accumulating showing the tolerance of these devices, e.g. high hit efficiency after large fluences.
- The full potential of these sensors is not yet exploited, subtle design modifications are still possible to improve tolerance.
- In essence, D-CMOS are a valid option for tracking and vertexing in hadron machines