Precision vertexing and tracking for Linear Colliders

AIDA-2020 Topical Workshop on Future of Tracking

April 2nd, 2019

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Outline

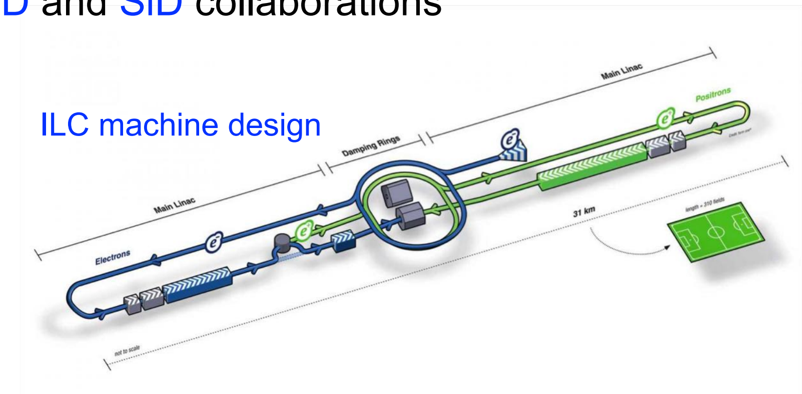
- Linear colliders and detectors
- Sensor and readout technologies for vertex/tracker
- Simulation framework
- Detector integration
- Conclusions

Disclaimer: incomplete selection of examples!
Many developments not mentioned here were discussed in previous talks at this workshop.

Linear e+e- colliders

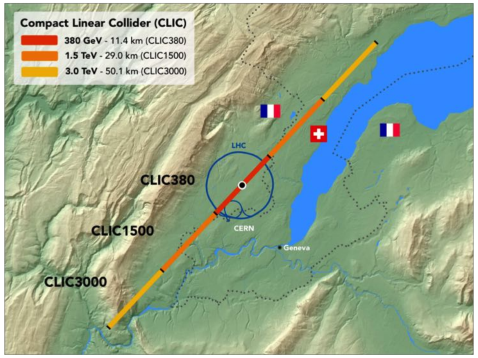
- ILC (International LInear Collider):
- $\sqrt{s}$ from 250 GeV to 500 GeV
  (superconducting RF cavities with 32 MV/m)
- Precision Higgs and top physics
- Detector and physics studies within the ILD and SiD collaborations

ILC machine design

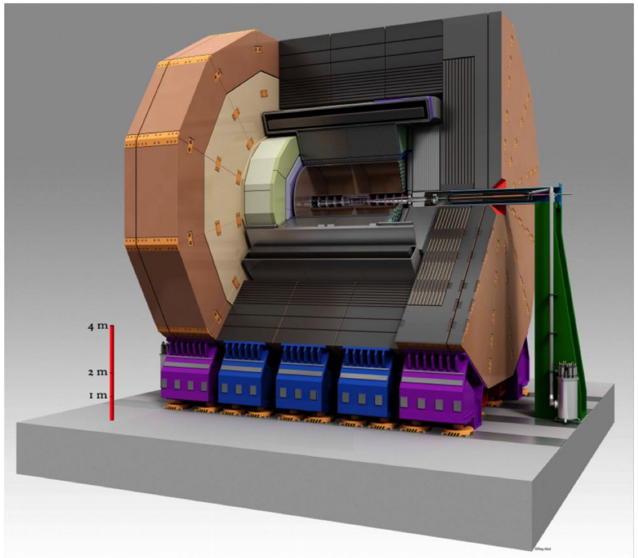


- CLIC (Compact LInear Collider):
  $\sqrt{s}$ from 380 GeV up to 3 TeV
  (two-beam acceleration with ~100 MV/m)
- Precision and top physics, BSM
- Detector and physics studies within the CLICdp collaboration

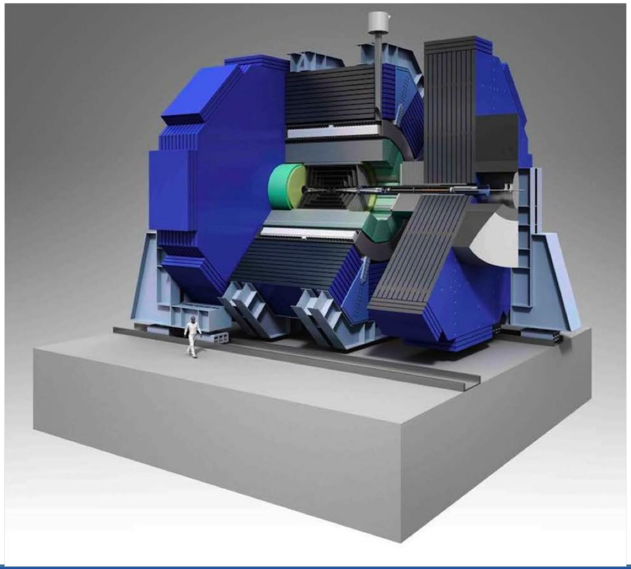
Staged CLIC implementation near CERN



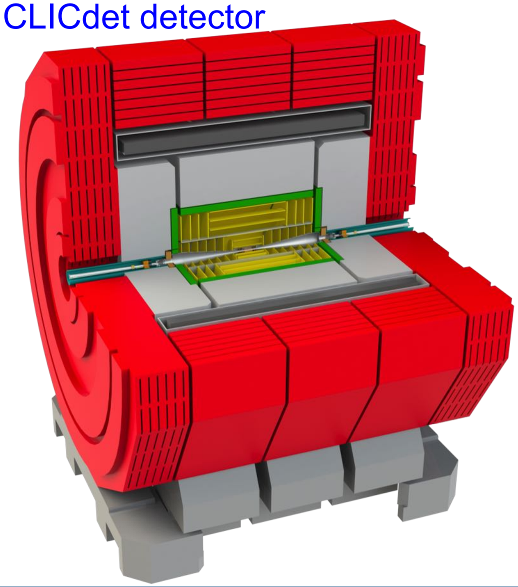
ILD detector



SiD detector



CLICdet detector



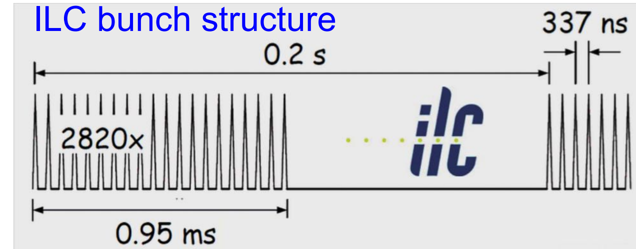
Experimental conditions

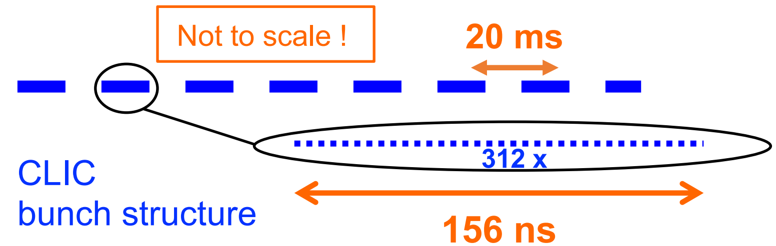
- ILC+CLIC operate with bunch trains, 5-50 Hz repetition rate

→ Low duty cycle

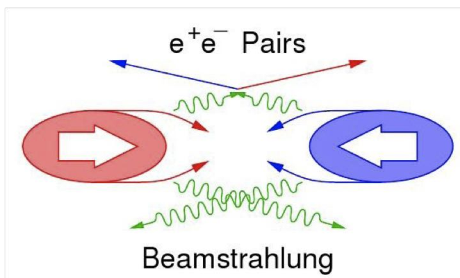
→ Trigger-less readout between trains

→ Allows for power-pulsed operation of detector, to reduce average power consumption

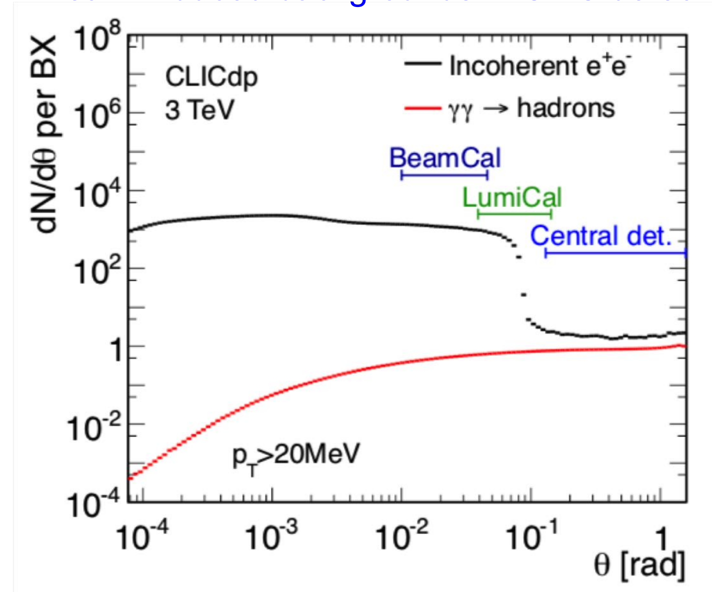




Very small bunches at LC:
40 nm (x) x 1 nm (y) x 44 μm (z)
(CLIC at 3 TeV)



Beam-induced backgrounds in CLIC detector



- High E-fields lead to Beamstrahlung

→ High rates of beam-induced background particles, overlaid to *O*(1) physics event per train

- At CLIC: all backgrounds within 156 ns trains,

→ up to 6 GHz/cm^2 instantaneous rate in inner detector at 3 TeV CLIC

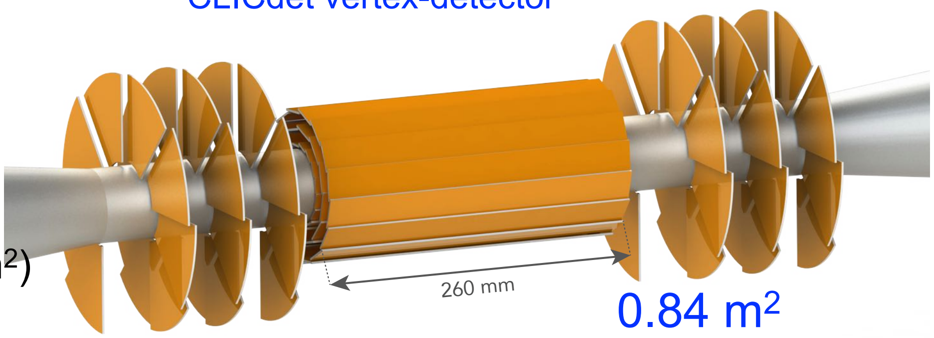
→ Drives detector design (layout, granularity, timing)

Vertex- and tracking detector requirements

Vertex detector:

- efficient tagging of heavy quarks through precise determination of displaced vertices:
  → good single point resolution: σ_{SP}~3 μm
    → small pixels ≲ 25x25 μm²
  → low material budget: ≲ 0.2% X_0 / layer
    → low-power ASICs + RT air cooling (~50 mW/cm²)

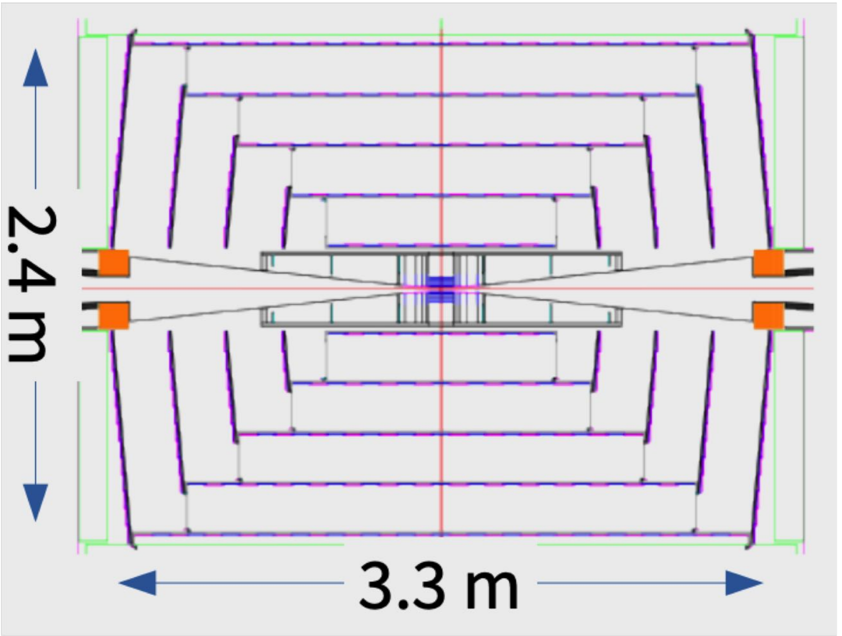
CLICdet vertex-detector



Tracker:

- Good momentum resolution: $\sigma(p_T) / p_T^2 \sim 2 \times 10^{-5}$ GeV^{-1}
  → 7 μm single-point resolution (~25-50 μm Rφ pitch)
  → many layers, large outer radius
  → ~1-2% X0 per layer
    → low-mass supports + services

SiD Tracker

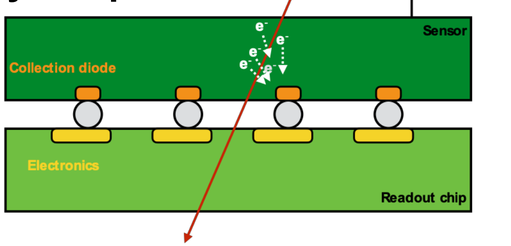


Both:

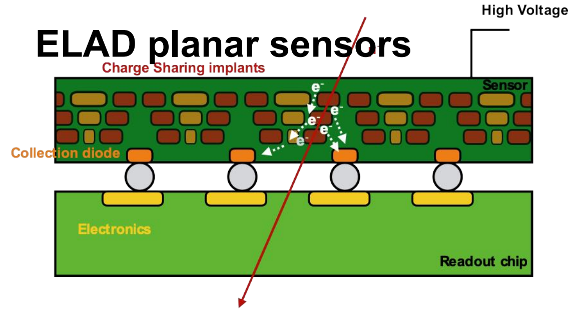
- 20-200 ms gaps between bunch trains
  → trigger-less readout, pulsed powering
- few % max. occupancy from beam backgrounds
  → sets inner radius and limits cell sizes
  → time stamping with ~5 ns accuracy for CLIC
  → depleted sensors (high resistivity / high voltage)
  (>=300 ns for ILC)
- moderate radiation exposure (~10⁴ below LHC!):
  - NIEL: < 10^{11} n_{eq}/cm²/y
  - TID: < 1 kGy / year

Sensor and readout R&D

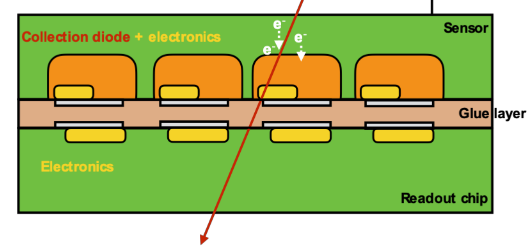
Hybrid planar sensors



ELAD planar sensors



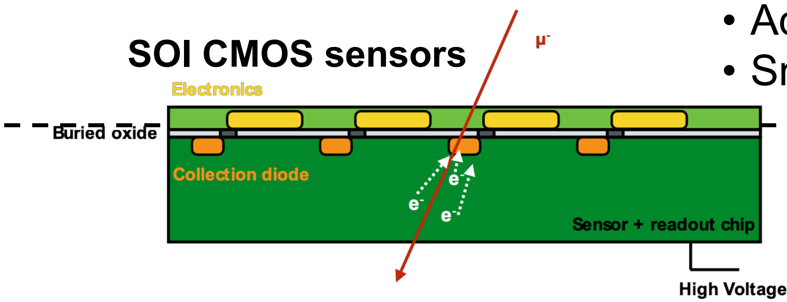
CCPD sensors



Hybrid detectors:

- Factorise r/o and sensor R&D
- Smallest feature-size ASICs
- Advanced sensor concepts
- Small pixels, highest performance → for CLIC inner layers

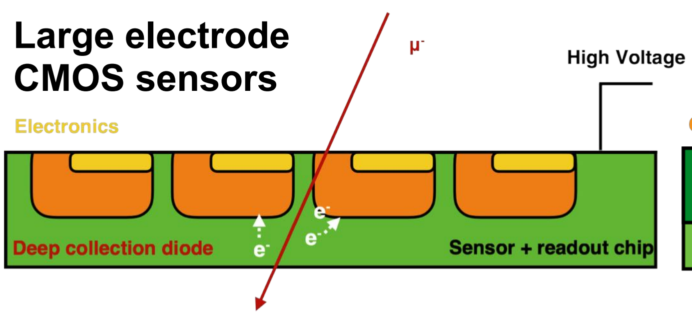
SOI CMOS sensors



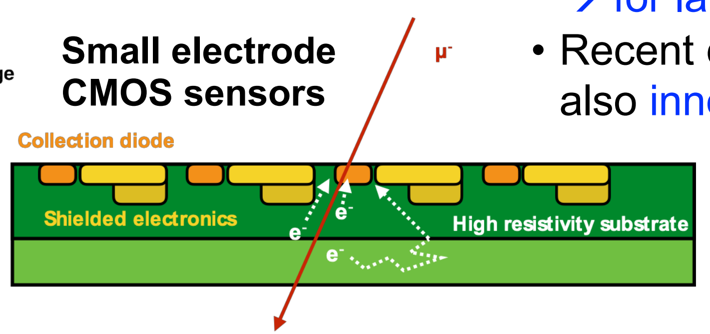
Monolithic CMOS sensors:

- Lowest material budget
- Medium feature-size
- Simplified construction
  → for large-area trackers
- Recent developments target also inner layers

Large electrode CMOS sensors

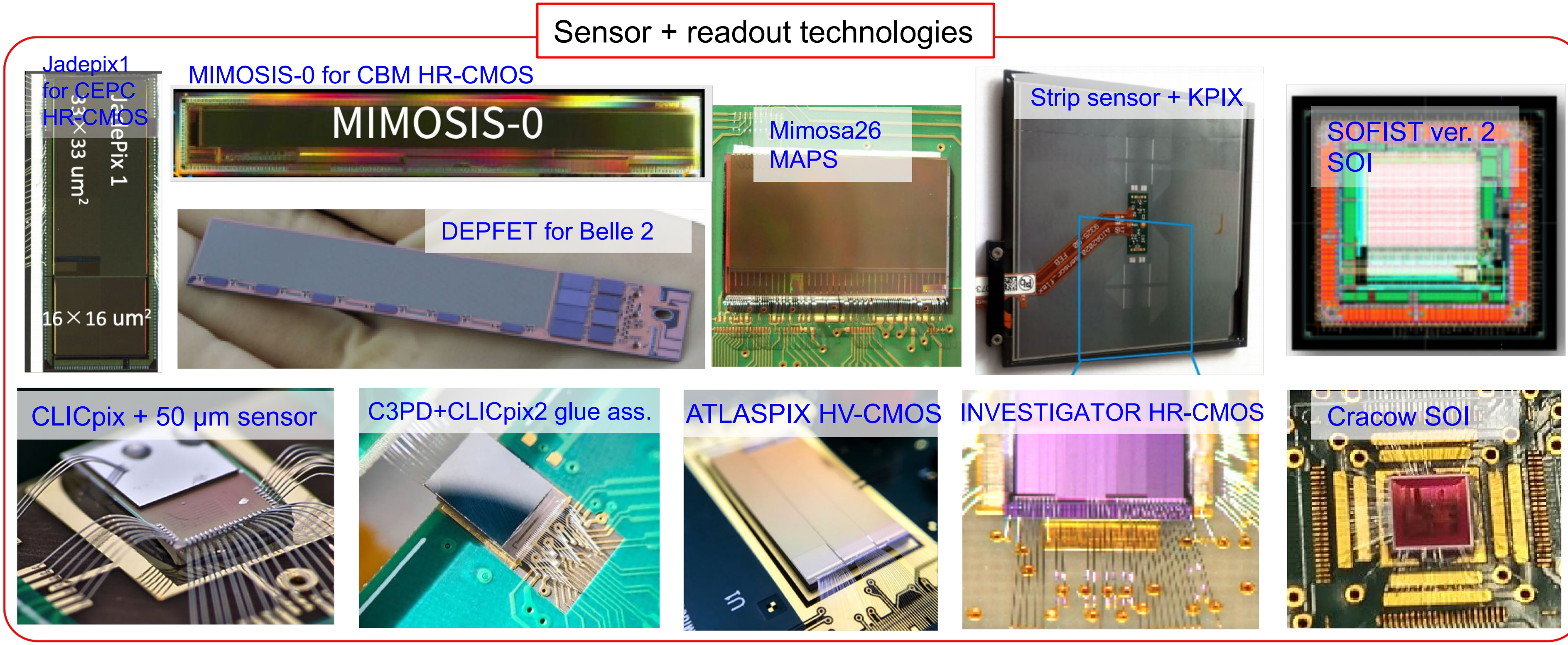


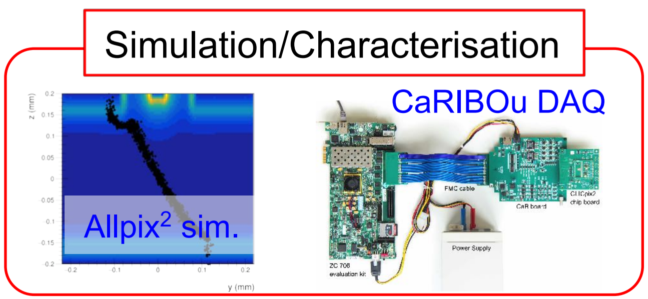
Small electrode CMOS sensors

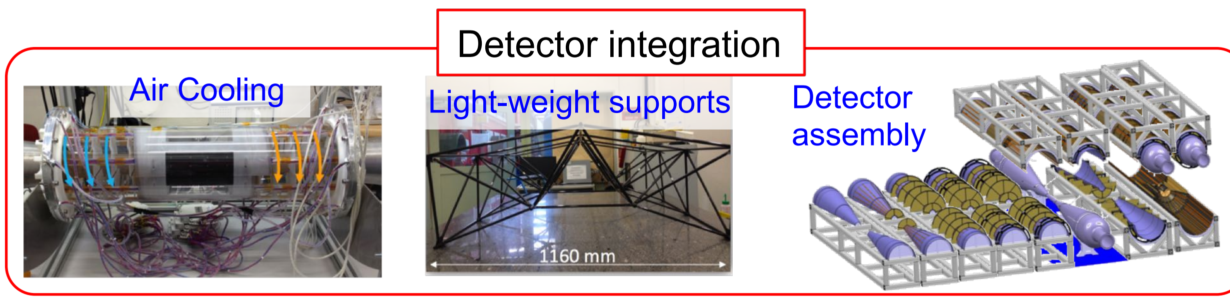


For ILC trackers: also strip detectors + Time Projection Chamber are considered

Silicon Detector R&D







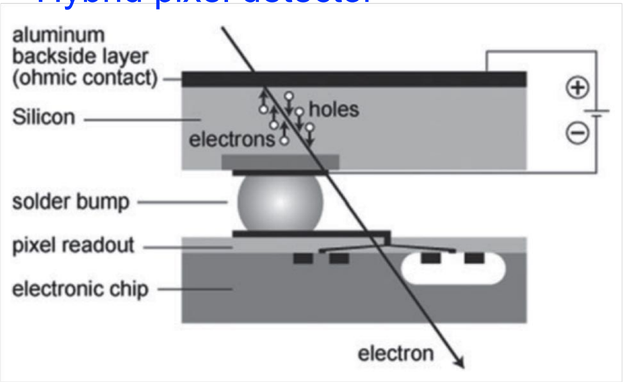
- Challenging requirements for LC lead to extensive detector R&D program
- Exploiting synergy and collaboration with other detector development projects, such as Belle II, STAR, CBM, ATLAS, ALICE, LHCb, Mu3e, CEPC, AIDA-2020, …

Thin hybrid planar pixel detectors

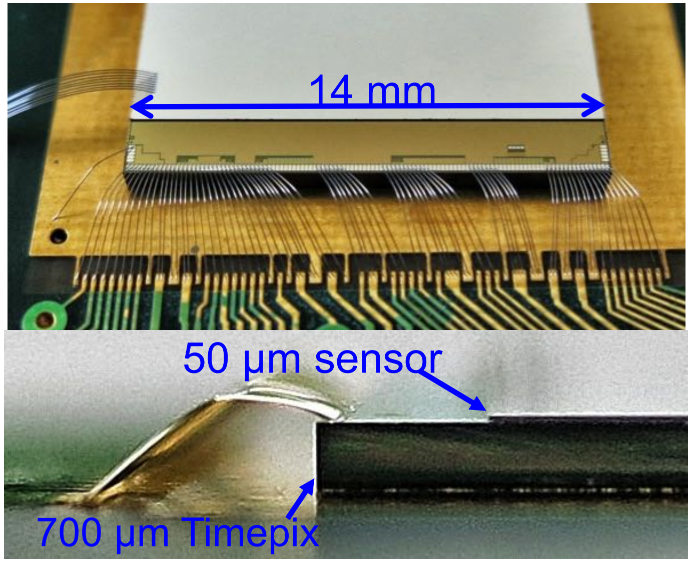
- Planar pixel sensors bump-bonded to r/o ASICs
- Considered for CLIC vertex detector

- Comprehensive thin-sensor studies with slim-edge and active-edge sensors (50-500 μm thickness) on Timepix (250 nm) and Timepix3 (130 nm) readout ASICs with 55 μm pitch

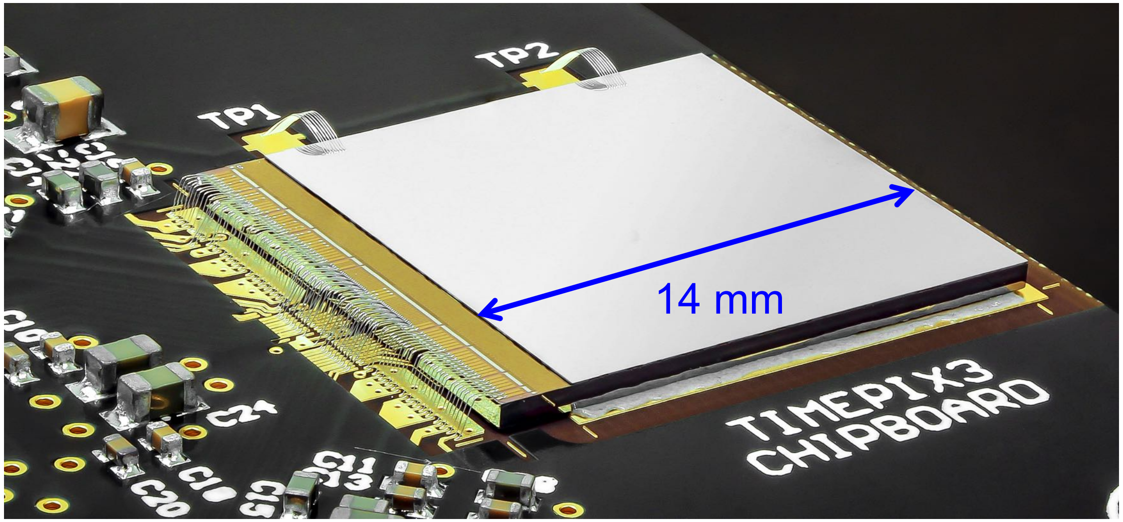
Hybrid pixel detector



Timepix with 50 μm active-edge sensor

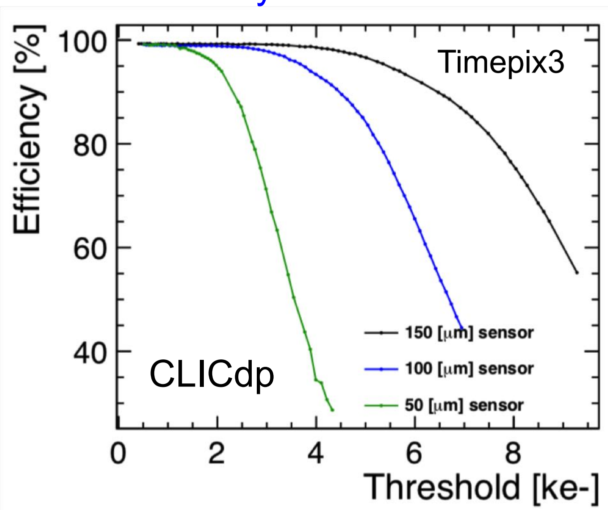


130nm Timepix3 with 50 μm active-edge sensor

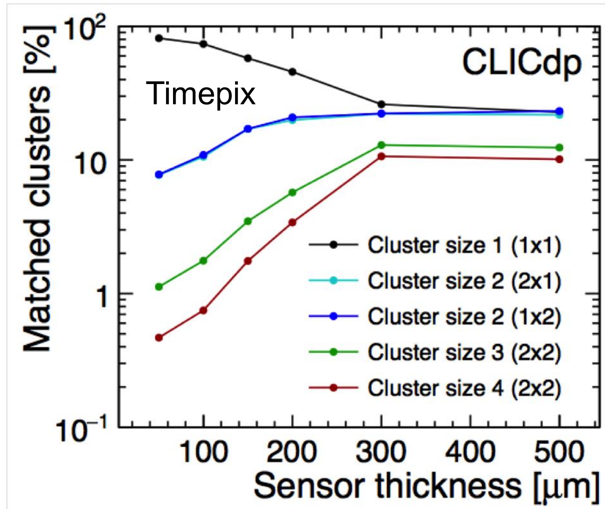


Timepix(3) + planar sensor test-beam results

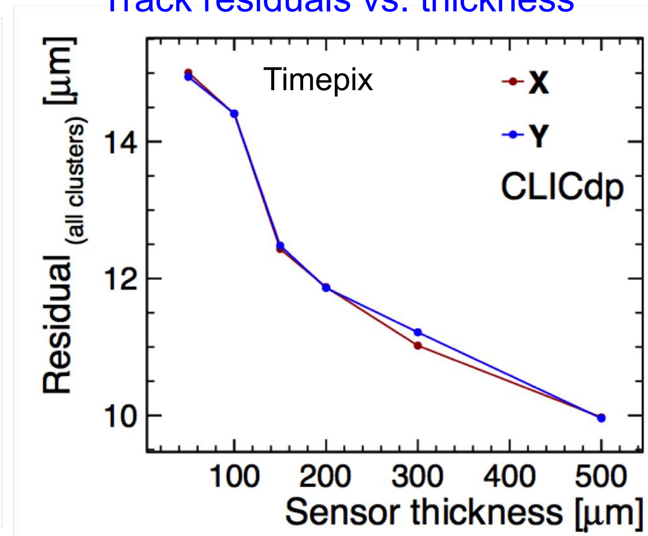
Efficiency vs. det. threshold



Cluster sizes vs. thickness

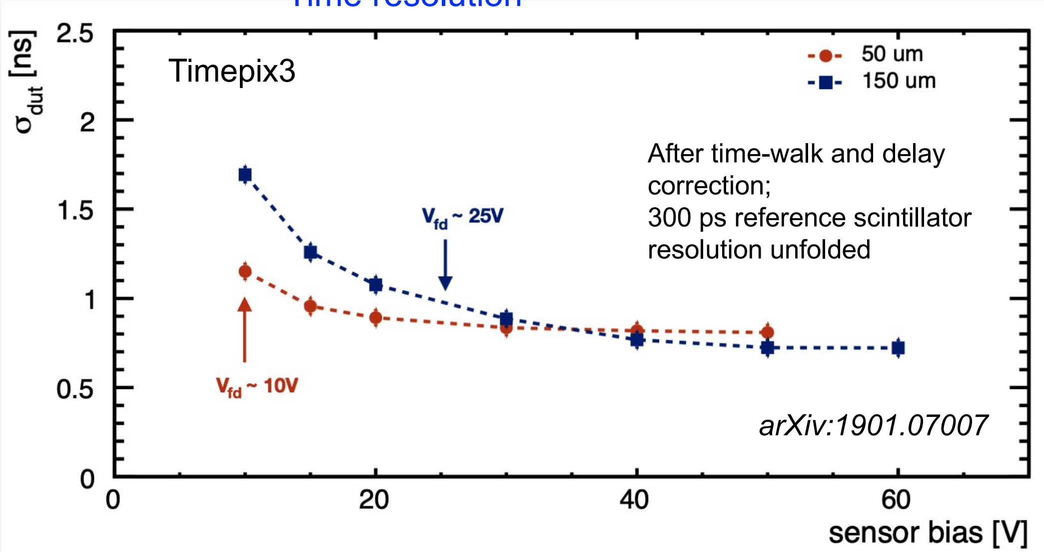


Track residuals vs. thickness



CLICdp-Note-2016-001
DISS. ETH NO. 24216

Time resolution

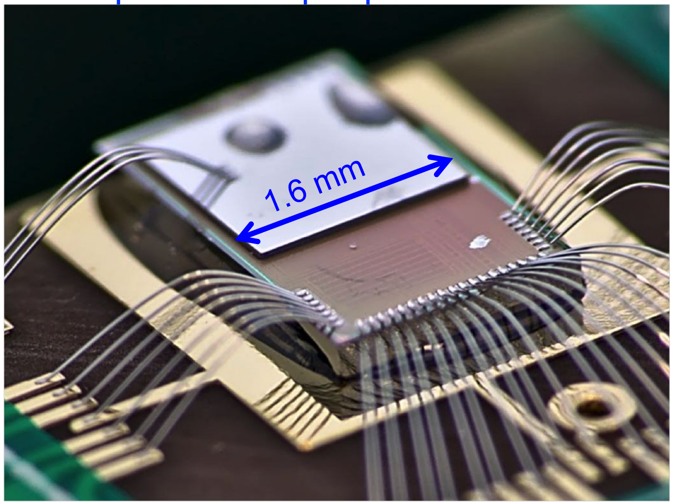


- ~100% efficiency down to 50 μm thickness (up to cut edge)
- Low fraction of 2-hit clusters limits achievable resolution
  → Not enough charge sharing in very thin sensors
- ~700 ps time resolution, better than required for CLIC

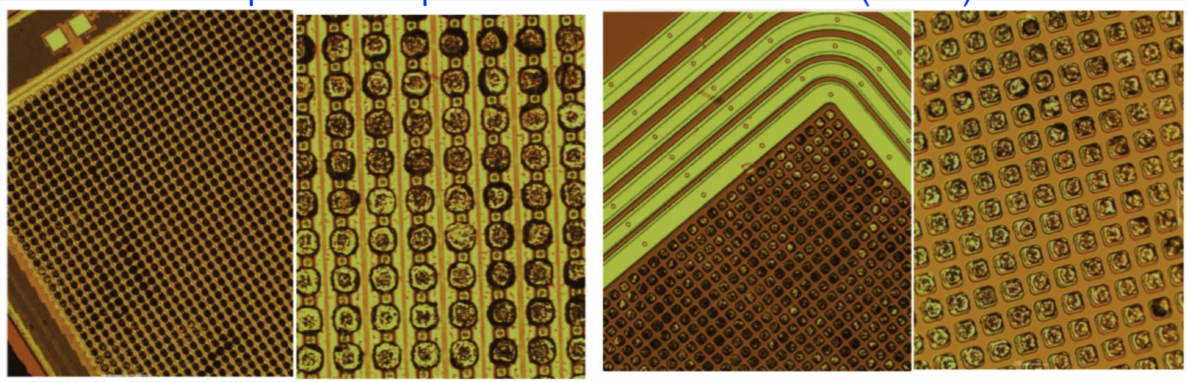
Fine-pitch hybrid detectors for CLIC

- CLICpix/CLICpix2 r/o ASICs with in-pixel time (10 ns binning) and energy (4-5 bit) measurement
- 25x25 μm^2 pitch
- Implemented in 65 nm CMOS process
- Single-chip bump-bonding with 50-200 μm thin sensors
  → challenging; process optimization ongoing

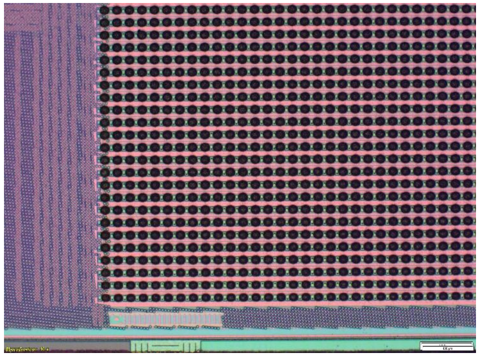
CLICpix with 50 μm planar sensor



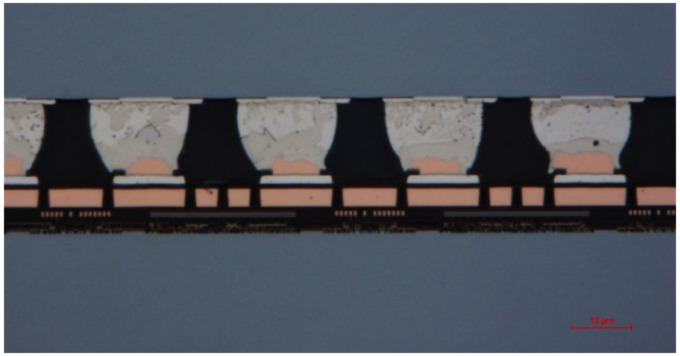
Indium bumps on CLICpix ASIC and Micron sensor (SLAC)



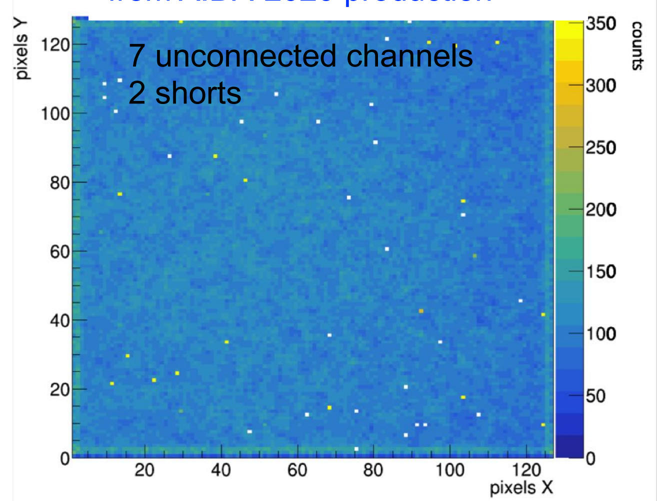
SnAg bumps on CLICpix2 (IZM)



Advacam sensor on CLICpix2 (IZM)

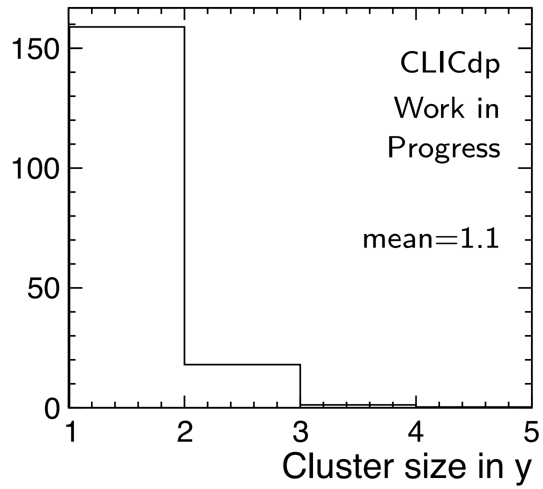


Sr-90 hit map for CLICpix2 + FBK 130 μm active-edge sensor from AIDA-2020 production

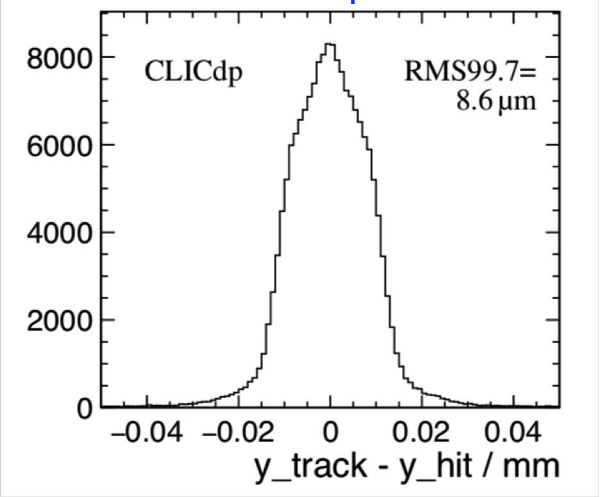


CLICpix + planar sensor test-beam results

Cluster size 50 µm sensor

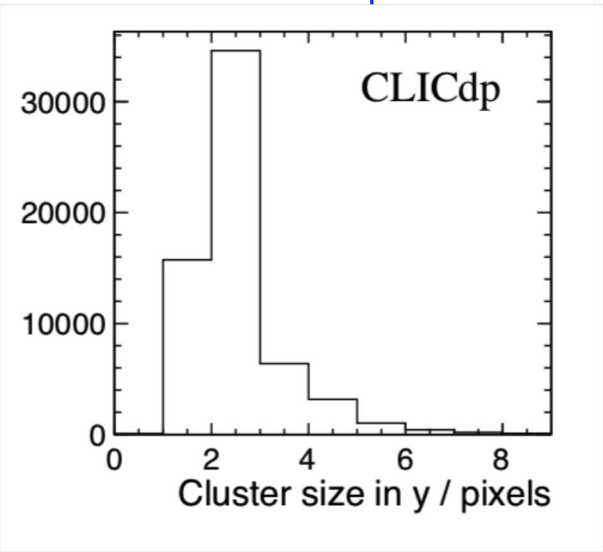


Residuals 50 µm sensor

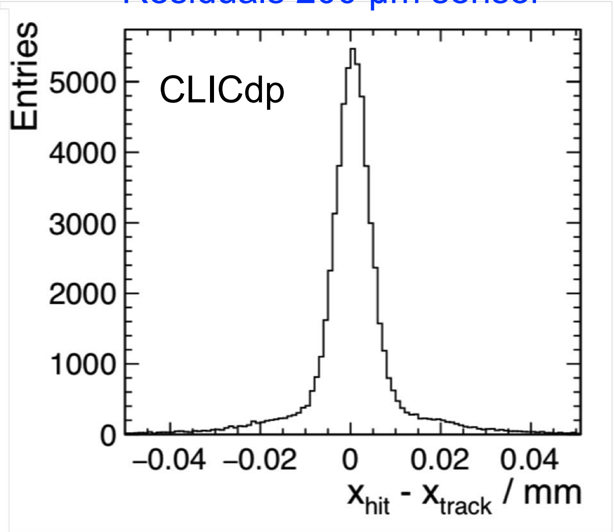


For 50 µm sensor thickness:
Mostly single-pixel cluster
→ No charge interpolation
→ Resolution limited by pixel pitch

Cluster size 200 µm sensor



Residuals 200 µm sensor



For 200 µm sensor thickness:
Mostly two-pixel cluster
→ Charge interpolation
→ Resolution close to target value of 3 µm
→ But too thick for material-budget target 0.2%X0/layer

JINST 12 (2017) C06006

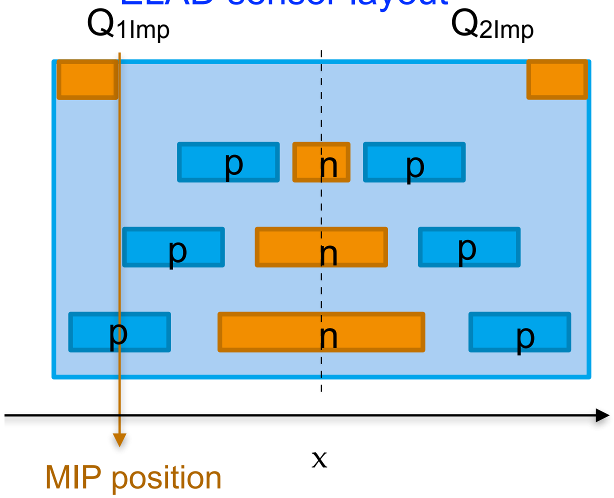
Enhanced Lateral Drift sensors

- Position resolution in very thin sensors so far limited to ~pixel pitch / $\sqrt{12}$ (almost no charge sharing)

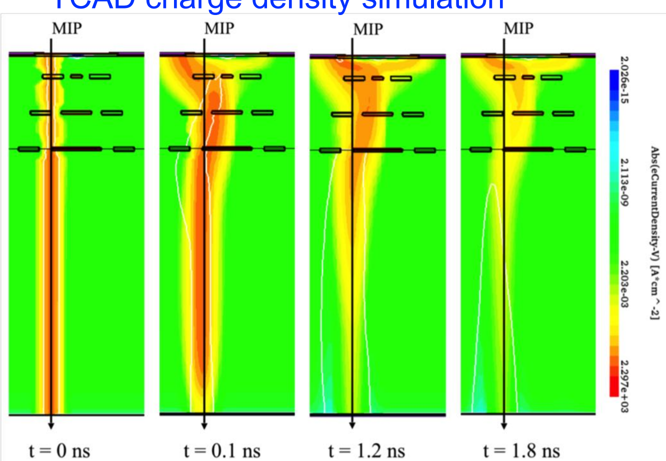
→ **E**nhanced **LA**teral **D**rift sensors (ELAD) Patent DE102015116270B4

- Deep implantations to alter the electric field
  → lateral spread of charges during drift, cluster size ~2
  → improved resolution for same pitch
- Challenges:
  - Complex production process, adds cost
  - Have to avoid low-field regions (recombination)
- TCAD and MC simulations: Implantation process, Sensor performance for MIPs
  → expect significantly improved position resolution vs. standard sensor
- Plans for first demonstrator production: generic test structures, strips and test sensors with Timepix(3) footprint (55 µm pitch)

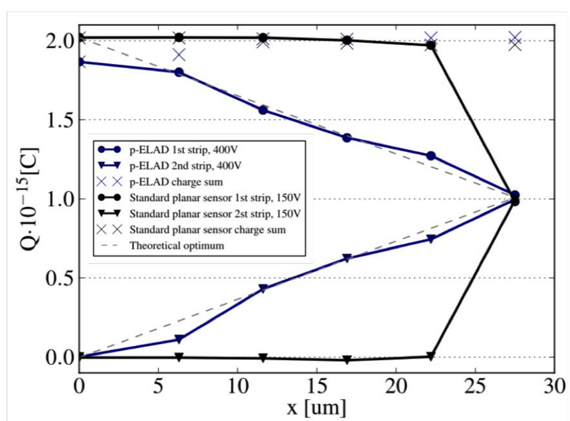
ELAD sensor layout



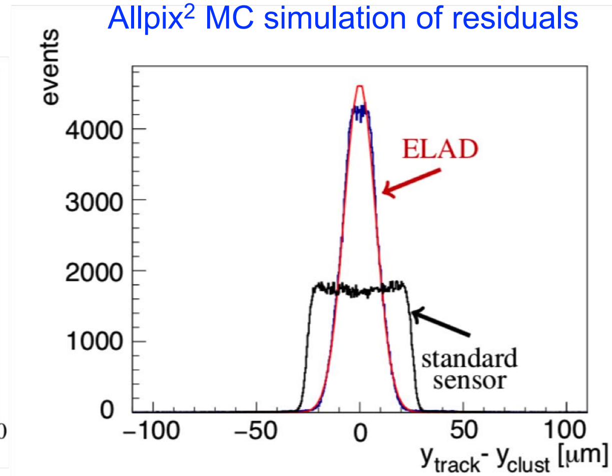
TCAD charge density simulation



Collected charge vs. MIP position



Allpix² MC simulation of residuals

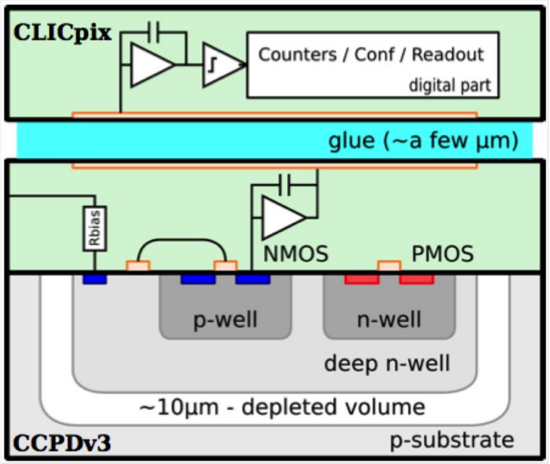


Capacitively coupled HV-CMOS sensors

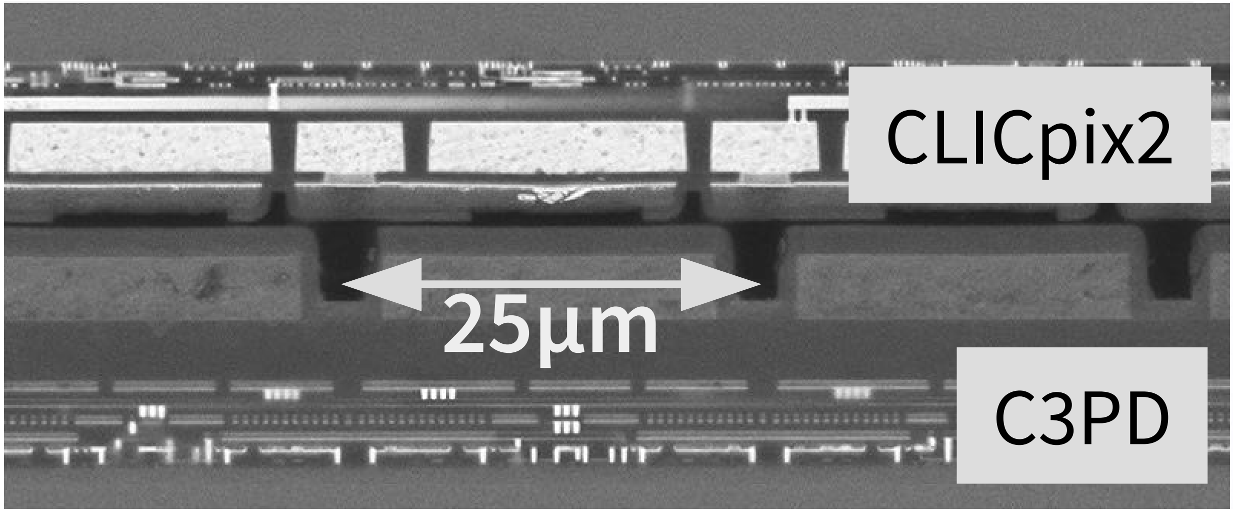
- Active sensors in 180 nm High-Voltage (HV) CMOS process, large fill factor: electronics in charge-collection well
- Amplification in sensor, capacitive coupling to r/o ASICs
  → thin glue layer replaces costly small-pitch bump bonds
- High-resistivity substrates (up to 1kΩcm) to increase depletion
- Considered for CLIC vertex detector

- Active sensors (CCPDv3, C3PD), 25x25 μm^2 pitch
- Glue assemblies with CLICpix/CLICpix2

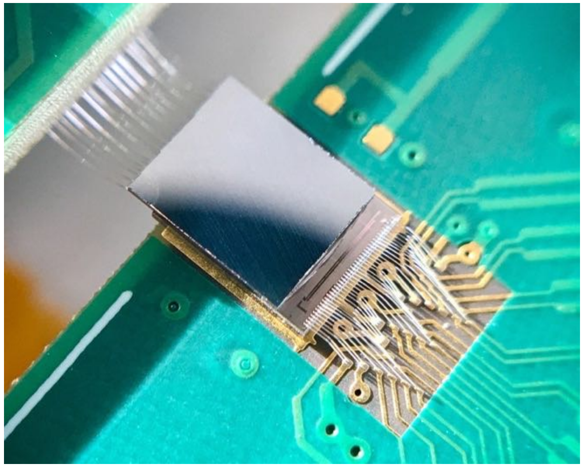
Capacitively Coupled Pixel Detector



Cross section through C3PD/CLICpix2 glue assembly



C3PD/CLICpix2 glue assembly



NIM A 823 (2016) 1-8;
JINST 12 P09012 (2017)

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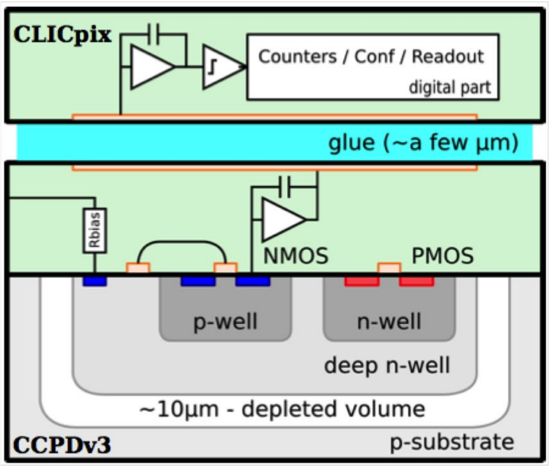
- Considered for vertex detector

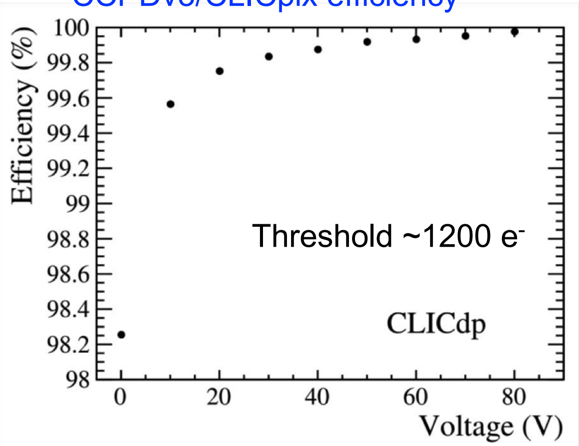
- Active sensors (CCPDv3, C3PD), 25x25 μm^2 pitch
- Glue assemblies with CLICpix/CLICpix2

- ~100% efficiency, σ_{SP}~6 μm, σ_t~7 ns
- Finite-element simulation of capacitive coupling
- Challenges: glue uniformity / alignment, calibration

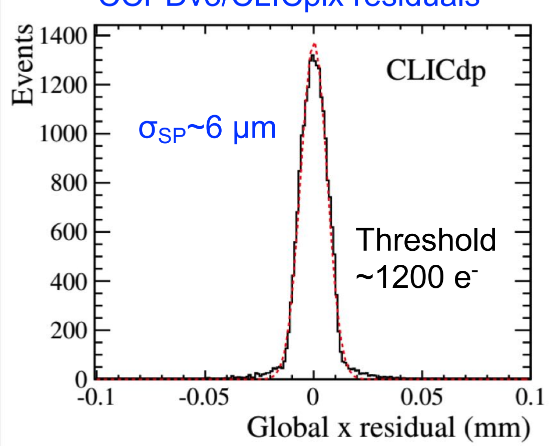
Capacitively Coupled Pixel Detector



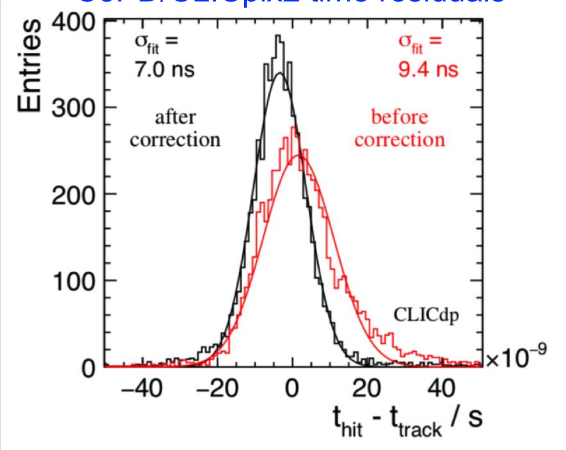
CCPDv3/CLICpix efficiency



CCPDv3/CLICpix residuals



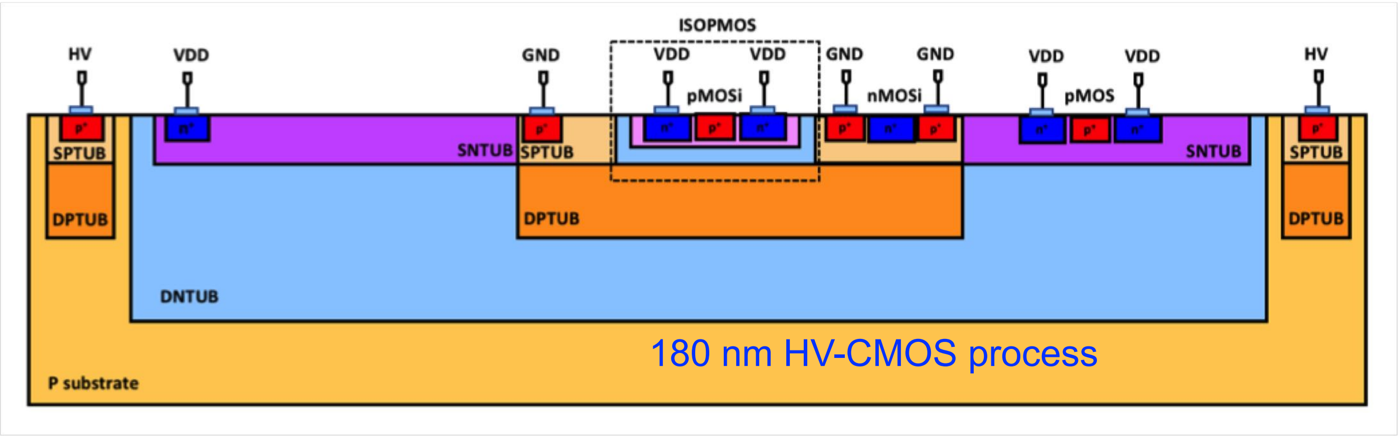
C3PD/CLICpix2 time residuals



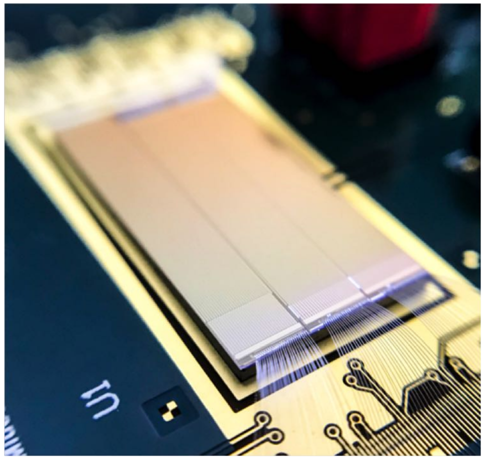
Monolithic HV-CMOS sensors

10.1016/j.nima.2018.06.060

- Active depleted HV-CMOS sensors with fully integrated readout
- Considered for CLIC tracker

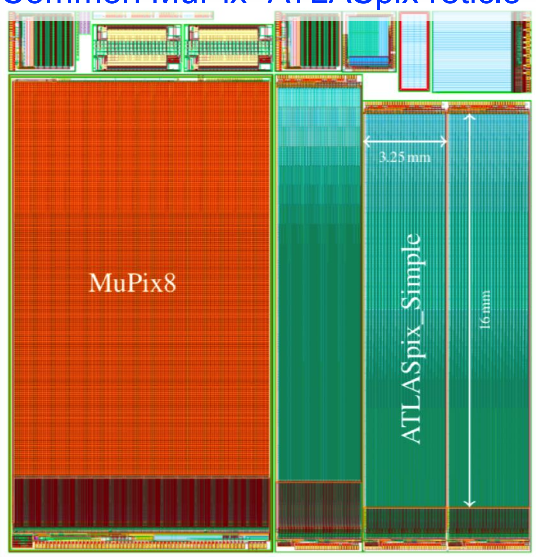


ATLASpix HV-CMOS sensor



- ATLASpix_Simple sensors in 180 nm HV-CMOS process:
  - Designed for ATLAS ITK upgrade
  - Targeting also CLIC tracker requirements
  - 130 x 40 μm^2 pitch
  - 25 x 400 pixels
  - Data-driven column-drain readout @ 1.6 Gb/s
  - 12.5 ns time bins
  - Beam tests in CLICdp Timepix3 telescope (1 ns reference timing)

Common MuPix+ATLASpix reticle



ATLASpix_Simple test-beam results

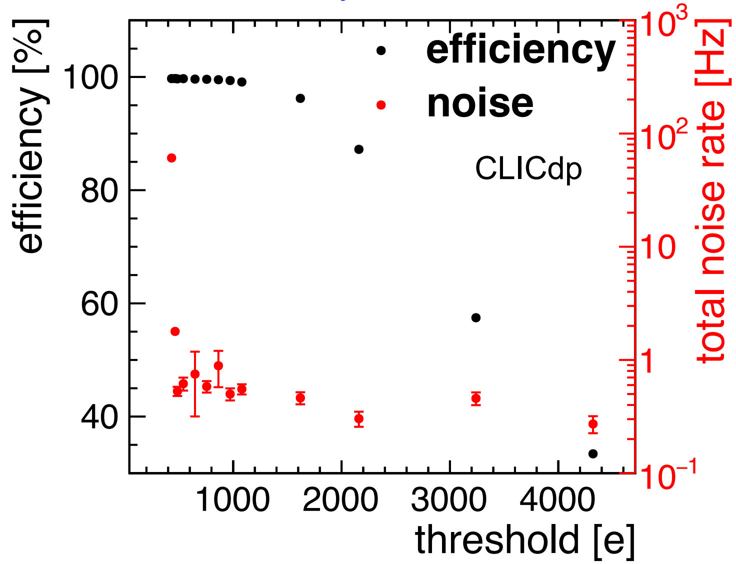
- 99.7% efficiency
- Time resolution: ~7 ns (RMS)
- Spatial resolution: σ_{SP}~12 µm (almost no charge sharing)
  → worse than required 7 µm

→ Plan for CLIC version with adapted footprint: ~200 x 25 µm² pitch

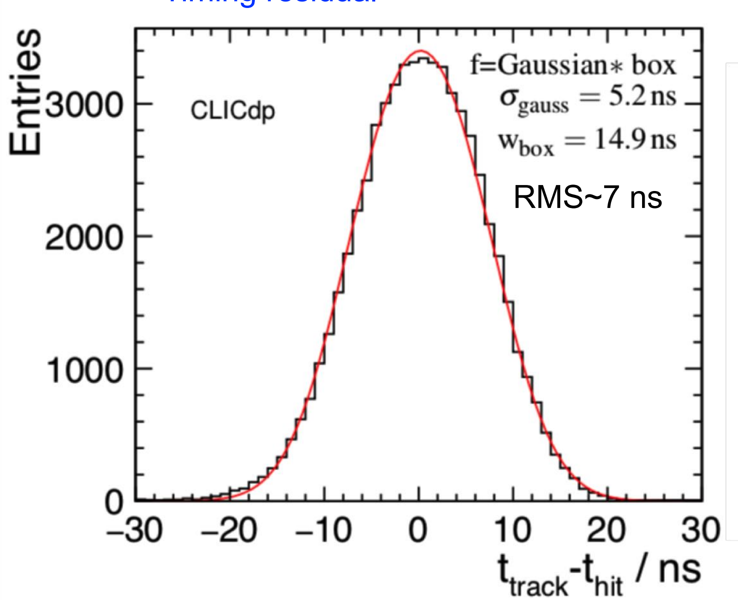
→ Plan for "generic" sensor matching test-beam telescope requirements

Also RD50 HV-CMOS developments in same process technology (Barcelona, Liverpool et al.)

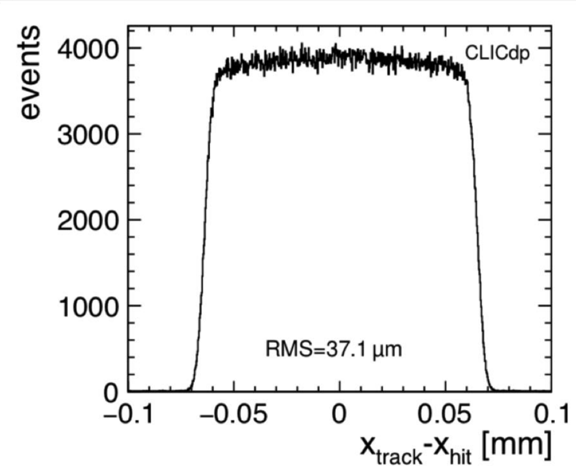
Efficiency



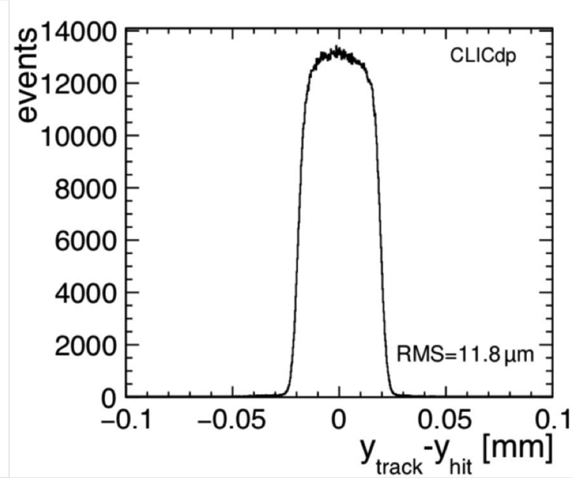
Timing residual



Residual in column direction



Residual in row direction

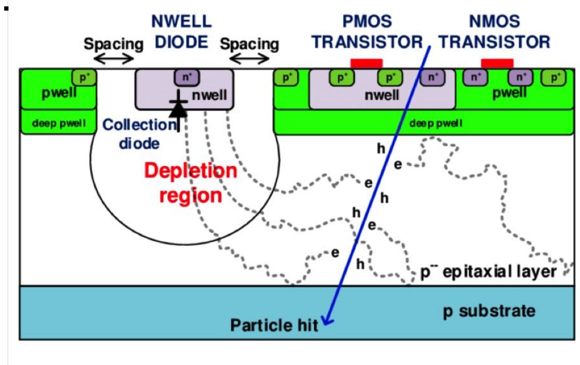


Reconstruction using: *https://gitlab.cern.ch/corryvreckan/corryvreckan*

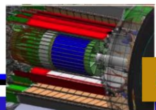
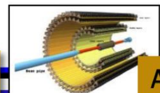
CMOS pixel sensors

"Mimosa-type" CMOS pixel sensor developments (IPHC Strasbourg):
- 350 nm / 180 nm imaging processes
- High-resistivity epitaxial layer, no high voltage, partial depletion
  → drift + diffusion contribute to signal

180 nm CMOS process



Evolving CPS

	ULTIMATE STAR-PXL	ALPIDE ALICE-ITS	MIMOSIS CBM-MVD	PSIRA proposal ILD-VXD
Data taking	2014-2016	>2021-2022	>2021	>2030
Technology	AMS-opto 0.35 μm	**0.18 μm**	0.18 μm	0.18 μm (conservative) < 0.18 μm ?
	4M	HR, V_{bias} ~-6V Deep P-well	HR, Deep P-well	?
Architecture	Rolling shutter + sparsification + binary output	**Asynchronous r.o. In pixel discri.**	Asynchronous r.o. In pixel discri.	Asynchronous r.o. (conservative)
Pitch (μm²) / Sp. Res.	20.7 x 20.7 / 3.7	27 x 29 / 5	22 x 33 / <5	~ 22 / ~ 4
Time resolution (μs)	~185	**5-10**	5	**1 – 4**
Data Flow		~10^6 part/cm²/s Peak data rate ~ 0.9 Gbits/s	peak hit rate @ 7 x 10^5 /mm²/s **>2 Gbits/s output (20 inside chip)**	~375 Gbits/s (instantaneous) ~1166Mbits / s (average)
Radiation	O(50 kRad)/year	2x10^{12} n_{eq}/cm² 300 kRad	3x10^{13} n_{eq}/cm²/yr & 3 MRad/yr	O(100 kRad)/year & O(1x10^{11} n_{eq}(1MeV)) /yr
Power (mW/cm²)	< 150 mW/cm²	**< 35 mW/cm²**	< 200 mW/cm²	~ 50-100 mW/cm² + Power Pulsing
Surface	2 layers, 400 sensors, 360x10^6 pixels 0.15 m²	7 layers, 25x10^3 sensors **> 10 m²**	4 stations Fixed target	3 double layers 10^3 sensors (4cm²) 10^9 pixels ~0.33 m²
Mat. Budget	~ 0.39 % X_0 (1st layer)	~ 0.3% X_0 / layer		~ 0.15-0.2 % X_0 / layer
Remarks	1st CPS in colliding exp.	(with CERN)	Vacuum operation Elastic buffer	Evolving requirements

4

A. Besson, LCWS 2018

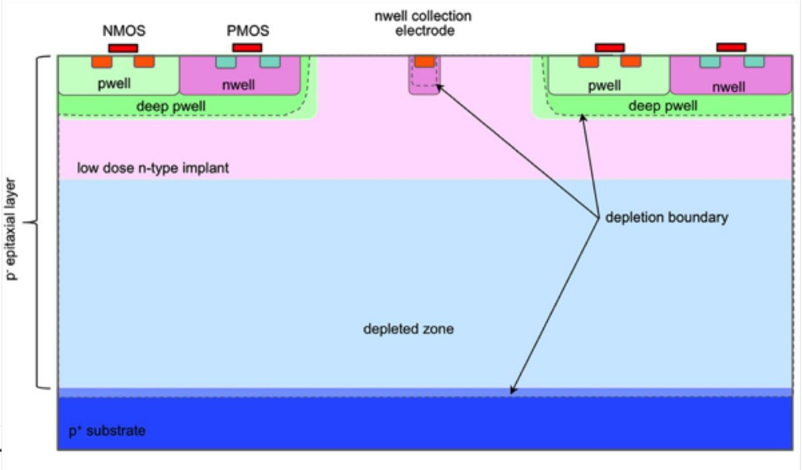
Developments feature:
- Low material budget
  ~50 μm Si
- Low power
  <200 mW/cm²
- Small pixels
  <5 μm resolution
- Moderate timing
  ~1-200 μs

- Targeting ILD VTX detector
- Various intermediate applications
  → talk by Jerome Baudot in this workshop

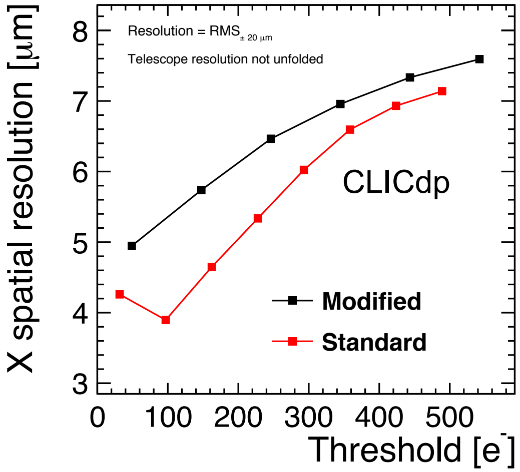
Monolithic HR-CMOS sensors

- Integrated CMOS sensors on High-Resistivity (HR) substrate
- Small collection electrode separated from electronics
  → small capacitance, high signal/noise
- Considered for ILC vertex, CLIC tracker
- Tests with Investigator analog test chip (external r/o) in 180 nm modified HR-CMOS imaging process (ALICE development), various test matrices
- For 28x28 μm^2:
  99.3% efficiency (<400 e^- thr.), σ_{SP}~4-5 μm, σ_t~6 ns

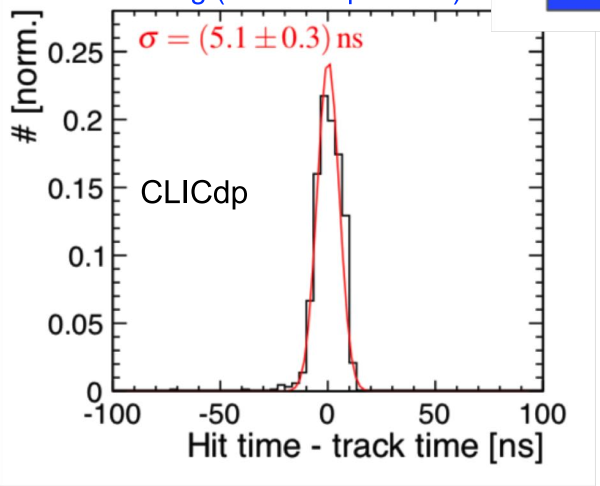
HR-CMOS process



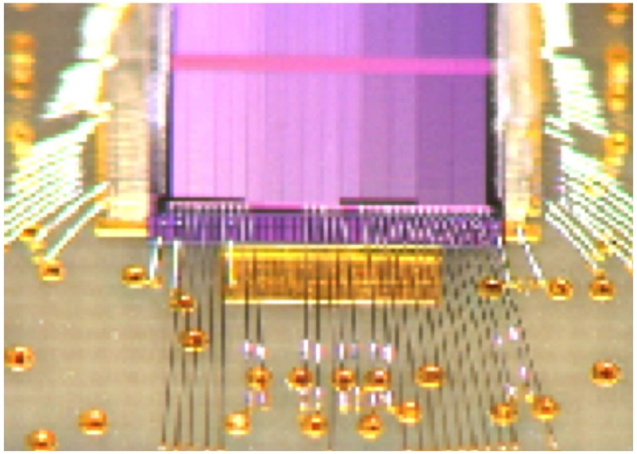
X resolution vs. threshold:



Timing (modified process)



INVESTIGATOR HR-CMOS test chip

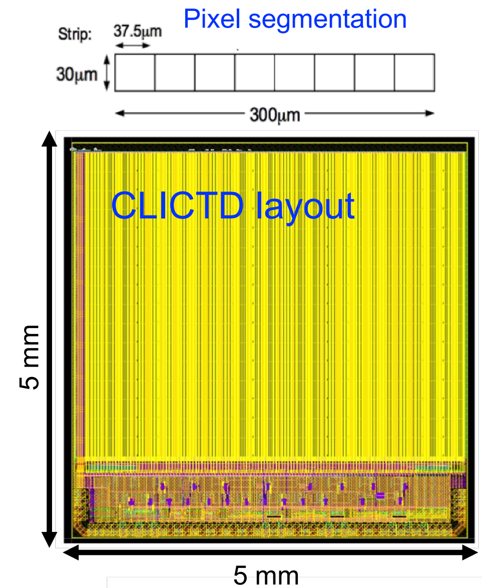


CLICdp-Pub-2018-004

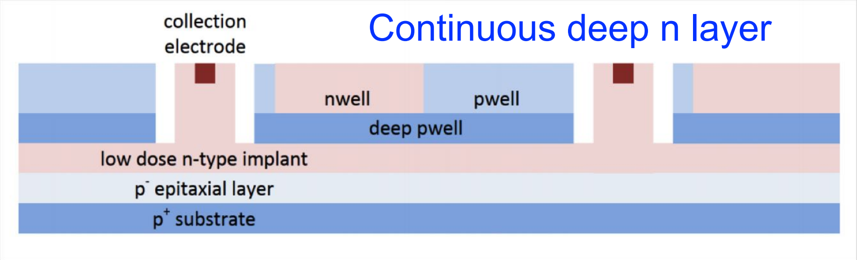
See also MALTA/Monopix developments (CERN, Bonn, et al.):
Combine precision with high rate / radiation hardness

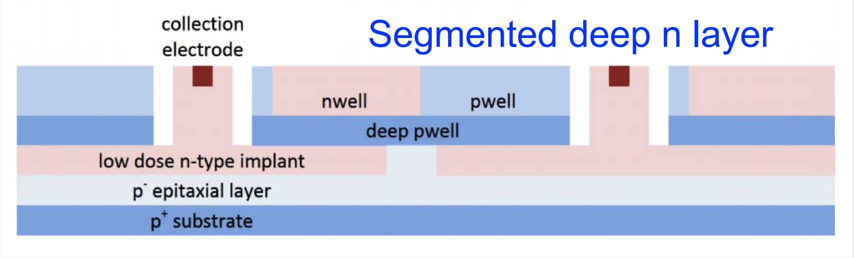
CLICTD monolithic HR-CMOS sensor

- Promising results obtained with Investigator test chip lead to design of fully integrated monolithic CLICTD sensor for CLIC tracker:
  - New concept of pixel segmentation in small collection diodes, to maintain fast charge collection while reducing digital logic: 30 x 300 μm^2 pixel size, 30 x 37.5 μm^2 diode size
  - TCAD geometry and process optimization
  - Process modification for radiation hardness (HL-LHC requirement) results in faster charge collection (CLIC requirement)
  - Time (8 bit, 10 ns bins) and charge (5 bit) measurement per pixel
  - Hit-pattern readout, power-pulsing features
- Chip submitted for production in 2 process variants (February 2019)

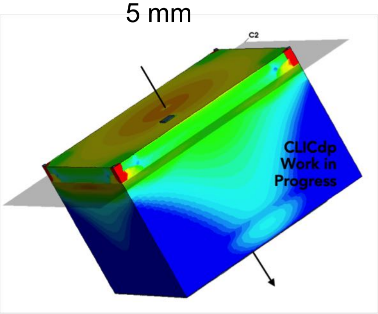


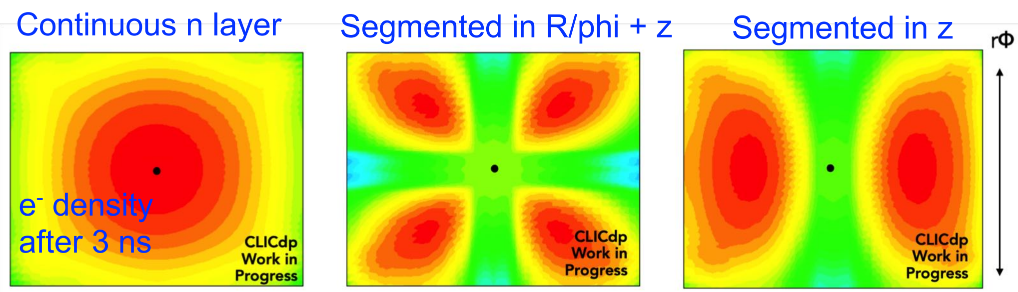
CLICdp-Conf-2018-008





TCAD optimisation:
Effect of sensor implant design on charge sharing

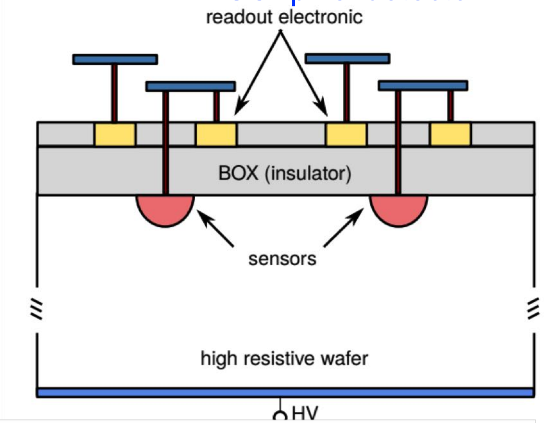




Monolithic SOI sensors

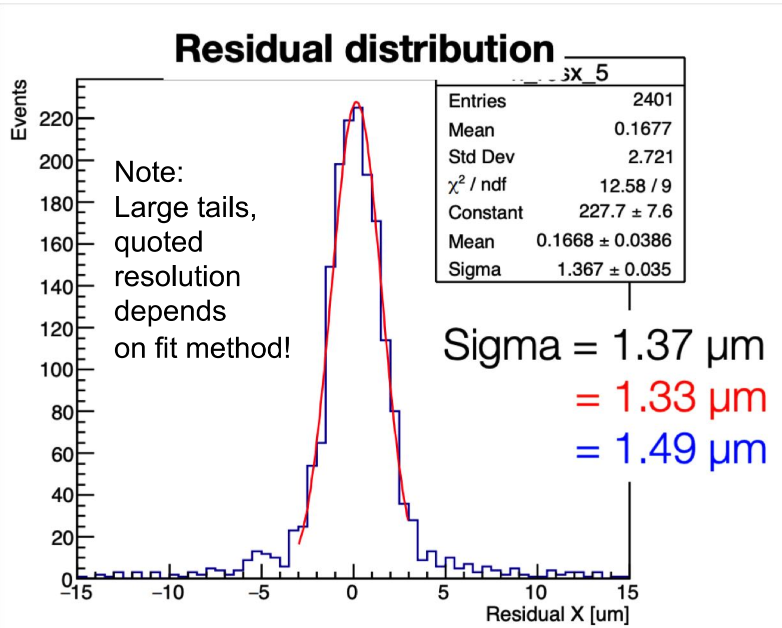
- Silicon-On-Insulator (SOI): r/o electronics on thin low-resistivity electronics wafer, separated from high-resistivity sensor wafer by buried insulation oxide layer
  → large signal, low noise
- Target both vertex and tracker requirements

SOI pixel detector

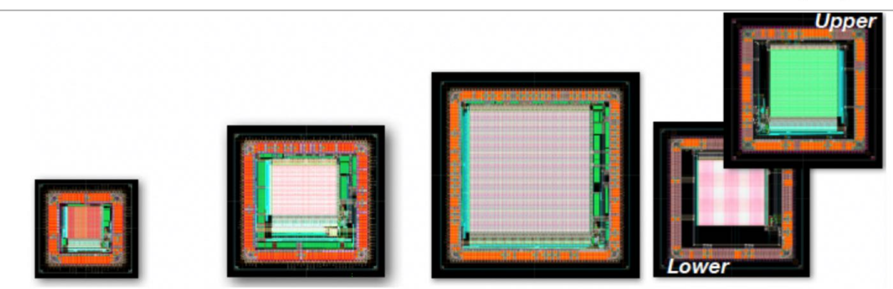


SOFIST: SOI sensor for Fine measurement Space and Time

- 200 nm Lapis SOI process, 20 x 20 – 30 x 30 μm^2 px size
- Spatial resolution ~1.3 μm (SOFIST 1, 200 μm depletion, only analog)
- Time resolution ~1.5 μs (SOFIST 2) → targets ILC detector



- 12 bit ADC, 500 μm (Full-depletion)
- 12 bit ADC, 200 μm (500 μm physic. thickn.)
- 8 bit ADC (On-chip), 500 μm

SOFIST	Ver.1	Ver.2	Ver.3	Ver.4 (3D)
				
Pixel circuit	Analog signal	Hit detection Timestamp	Full functionality	Full functionality 3D stacking
Chip size (mm)	2.9 × 2.9	4.45 × 4.45	6.0 × 6.0	4.45 × 4.45
Pixel size (μm)	20 × 20	25 × 25	30 × 30	20 × 20
Functions	Pre-amplifier Analog signal memory	Pre-amplifier Comparator Shift-register Analog signal memory (2hits) or Timestamp memory (2hits)		Pre-amplifier Comparator Shift-register Analog signal memory (3hits) Timestamp memory (3hits)

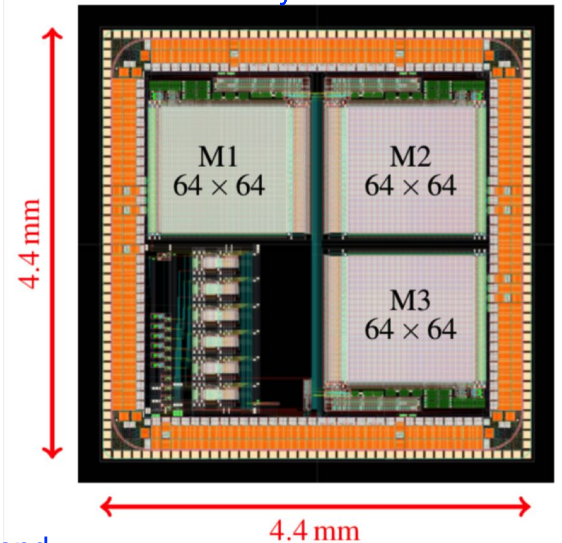
Shun Ono (KEK), PIXEL 2018

CLIPS monolithic SOI sensor

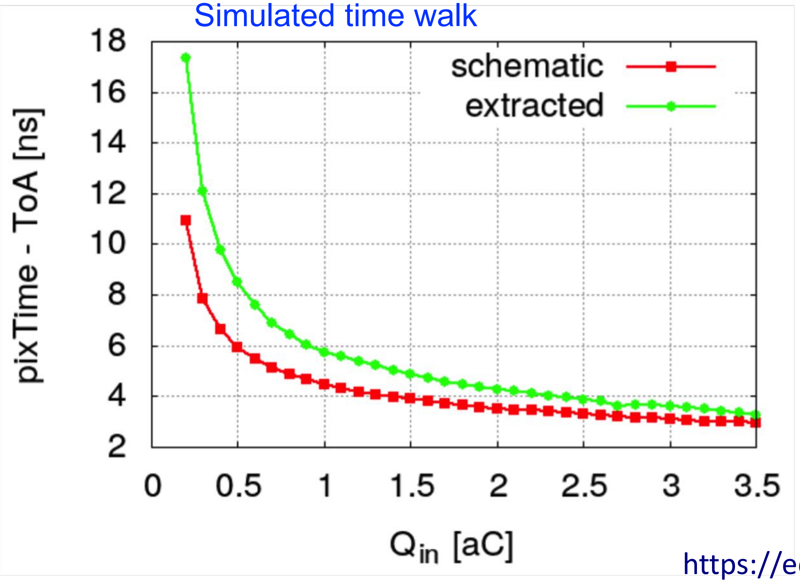
- CLIPS: New AGH SOI chip targeted to Linear Collider vertex detectors:
  - 3 test matrices with 64x64 pixels, 20x20 μm^2 pitch
  - Targets spatial resolution <3 μm, time resolution <10 ns
  - Analog charge and time information in storage capacitors in each pixel → no need for fast clock distribution into matrix
  - Snapshot analog readout between bunch trains with external ADC
  - On-chip trigger to reduce the data rate

  - Chips fabricated on 500 μm thick FZ-n wafers received
  - Thinning of selected wafers to 100 μm foreseen
  - Development of test system ongoing

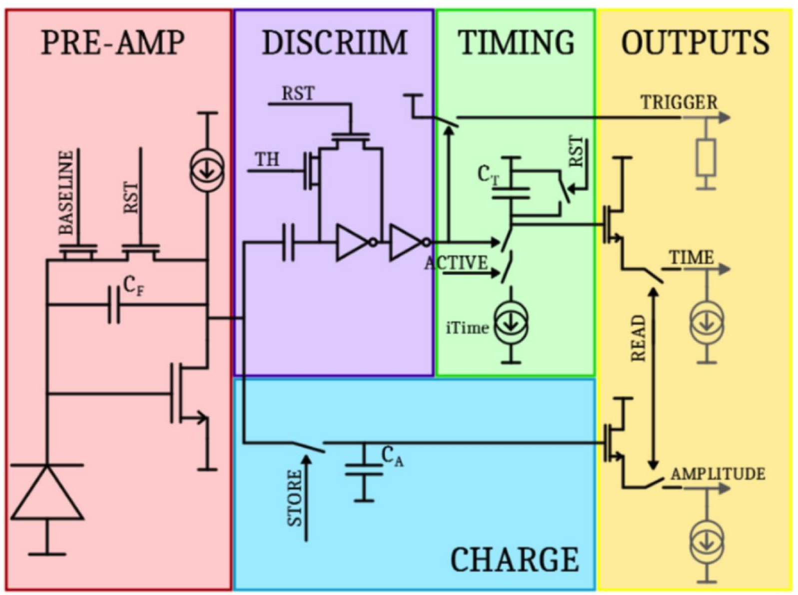
CLIPS layout



Simulated time walk



CLIPS frontend



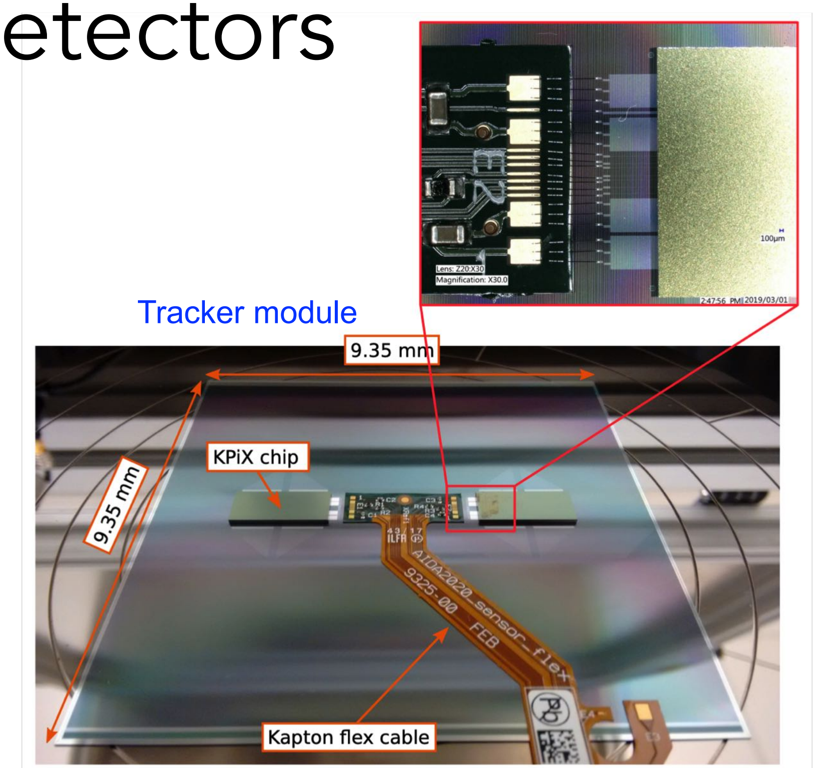
https://edms.cern.ch/document/2087018/1

Silicon strip detectors

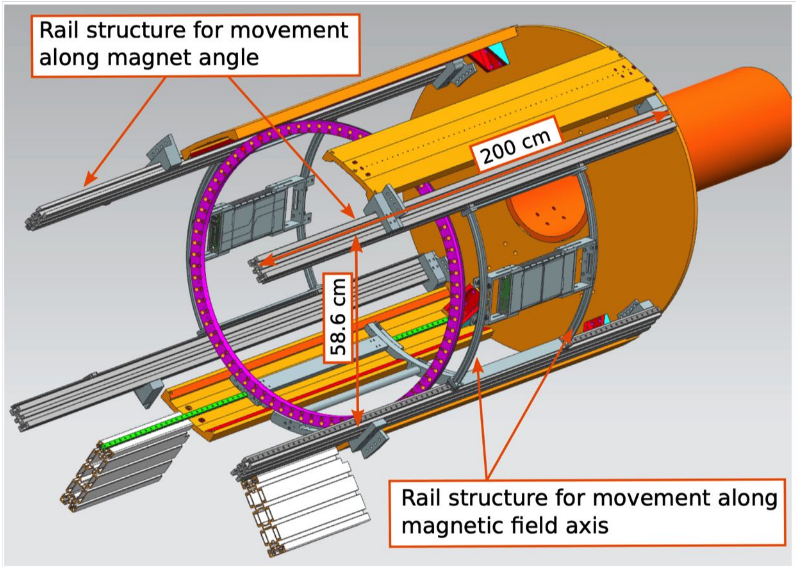
- ILD and SiD foresee strip-detector layers in tracker
- Strip tracker module prototypes for SiD produced:
  - Integrated pitch adapter (no separate hybrids)
  - 10 x 10 cm^2 Hamamatsu sensors, 320 µm thickness
  - 25 µm strip pitch, 50 µm r/o pitch, analog r/o (KPiX)

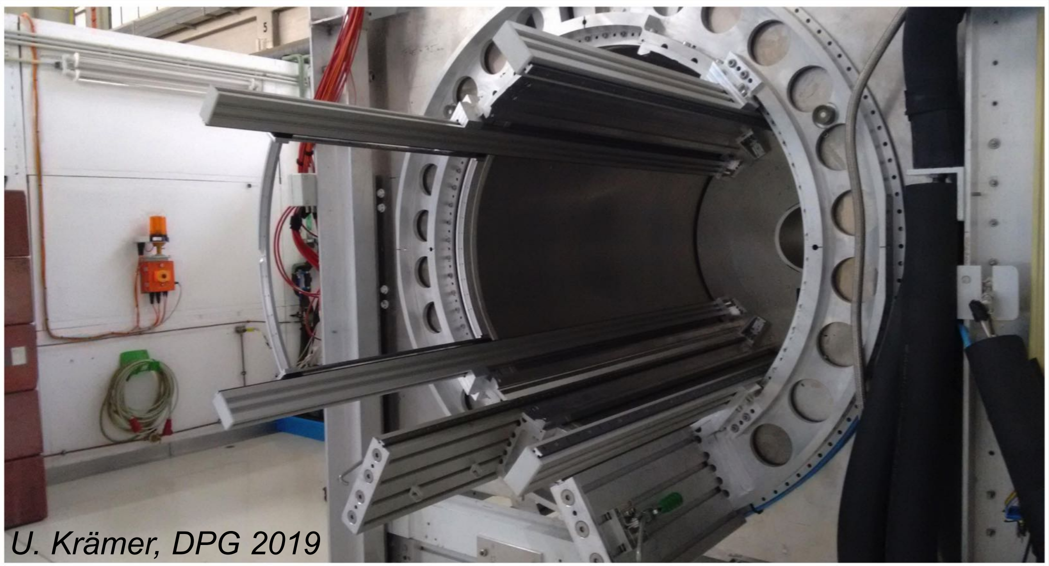
  →~7 µm single-point resolution in measurement plane
- First application: LYCORIS large-area telescope at DESY test beam

Tracker module



LYCORIS large-area telescope around TPC





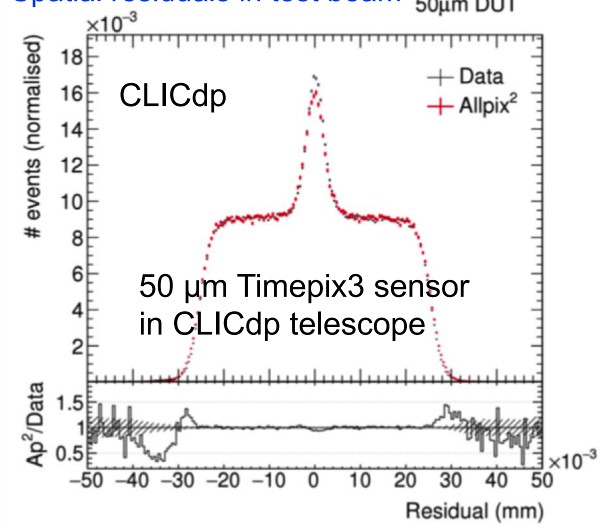
Allpix^2 simulation framework

- Complex sensors (ELAD, HR/HV-CMOS) require detailed simulations
- TCAD: device modeling, self-consistent charge propagation, slow
- Geant4: MC simulation of charge deposition and full detector setup, stochastic effects (Landau fluct.), no detailed device modeling, fast

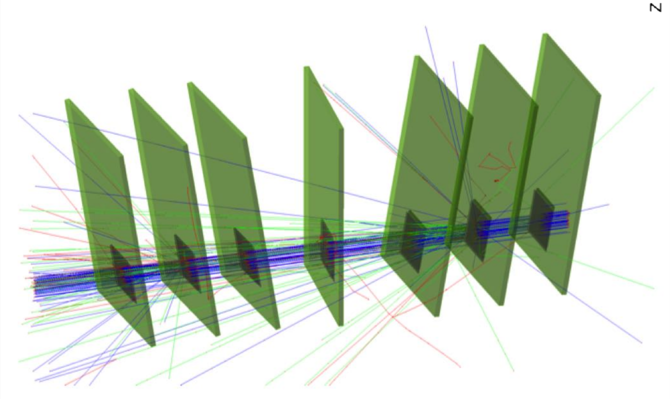
Allpix^2 simulation framework for tracking detectors

- Simulates full chain from incident radiation to digitized hits
- Combination of tools:
  - Full Geant4 simulation of charge deposition
  - Fast charge propagation using drift-diffusion model
  - Import electric fields from TCAD
- Validated with test-beam data (planar, HV-CMOS, HR-CMOS sensors)

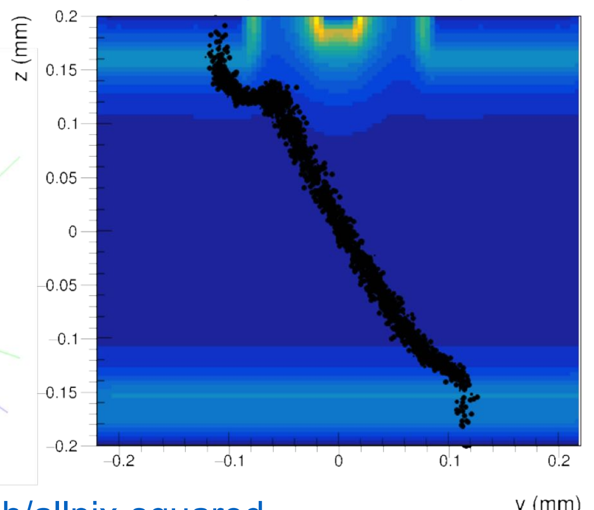
Spatial residuals in test beam



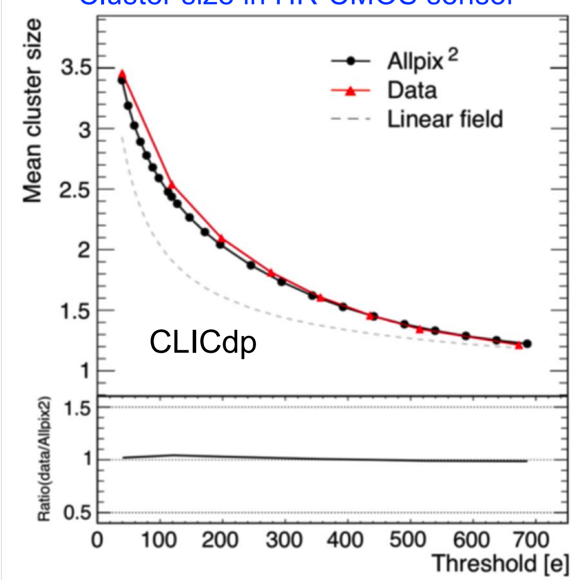
Beam telescope with tilted DUT



MIP in underdepleted HV-CMOS pixel sensor



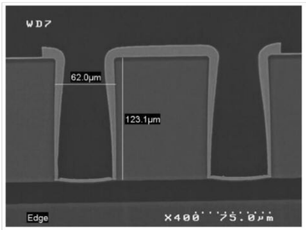
Cluster size in HR-CMOS sensor



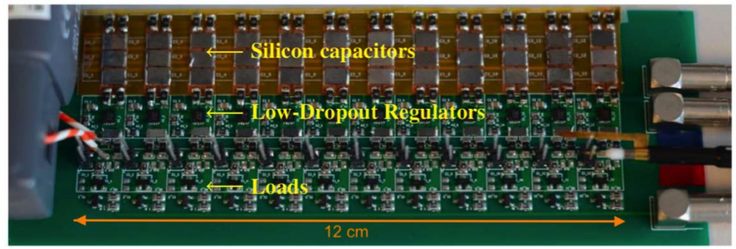
NIMA 901 (2018) 164   https://cern.ch/allpix-squared

Detector integration

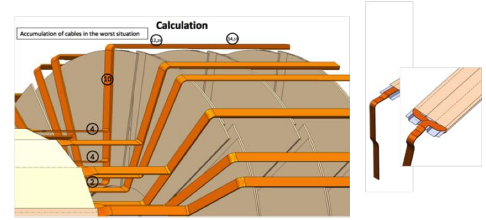
Through-Silicon Via



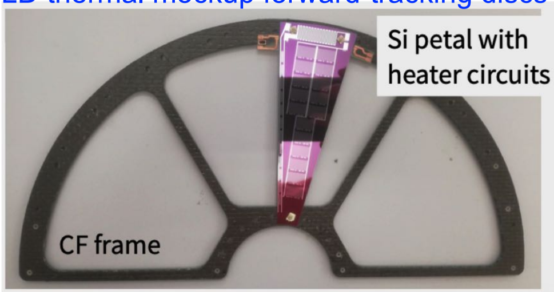
Power-pulsing mockup



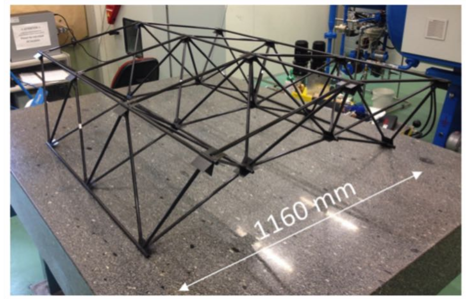
Vertex-detector services



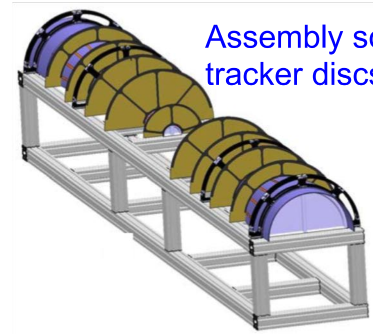
ILD thermal mockup forward-tracking discs



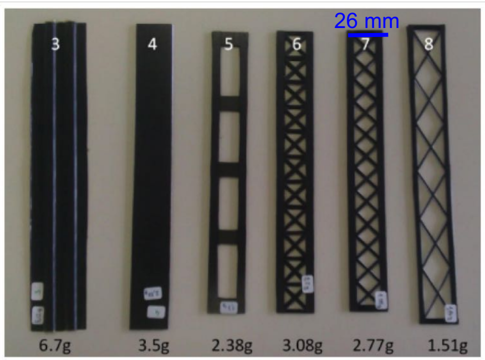
Outer barrel tracker support structure



Assembly scenario
tracker discs

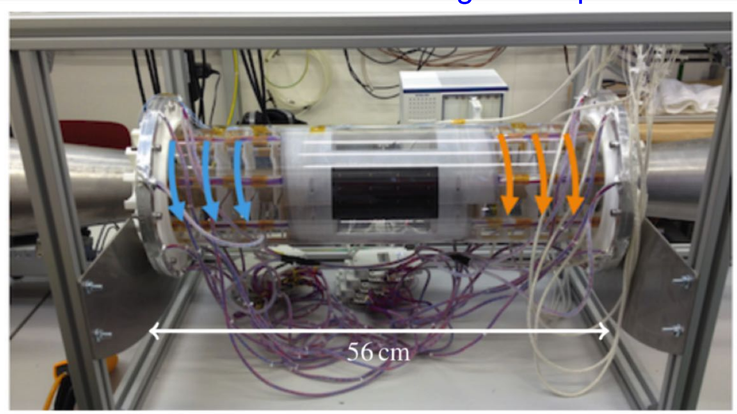


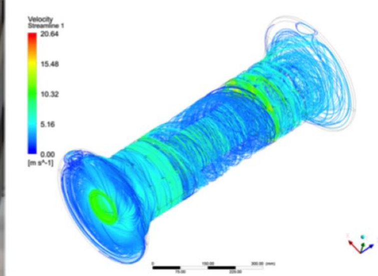
CFRP support prototypes



X/X0					
0,156 %	0,134 %	0,091 %	0,118 %	0,106 %	0,058 %

Air-flow cooling mockup and simulation





(b)

Calculations, simulations, prototyping → confirm feasibility of detector-integration concepts

Conclusions

- Stringent requirements for LC vertex and tracking detectors have inspired broad and integrated technology R&D program
- Various innovative sensor + readout technologies under study
- Moderate timing requirements for ILC allow for high-precision detectors based on established technologies
- Combination of requirements for CLIC vertex detector remains challenging
- Monolithic pixel detectors under development for large-area tracker and vertex
- Advanced simulation and analysis tools for detector performance optimization
- Detector integration studies confirm feasibility of proposed detector concepts

Thanks to everyone who provided material for this talk!

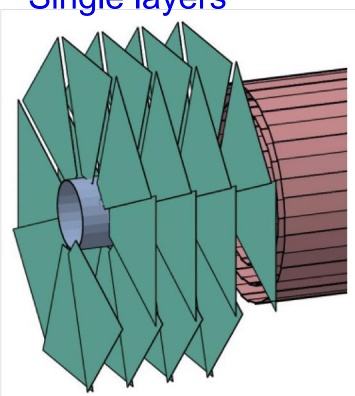
Additional Material

Flavor-tagging performance

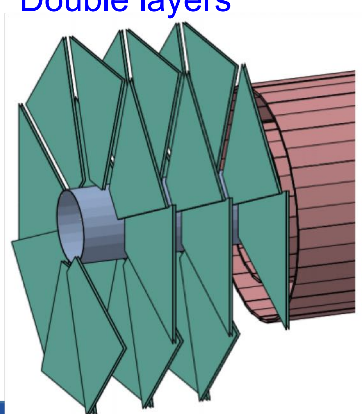
- Use b- and c-tagging performance as benchmark for detector designs
- Technically challenging full-simulation study (multivariate analysis)
- Results for geometries following engineering studies:
  - 3 double layers vs. 5 single layers
    → similar performance
  - Geometry with 2x more material in vertex layers
    → 5% - 35% degradation in performance

CLICdp-Note-2014-002
doi:10.1088/1748-0221/10/07/C07001

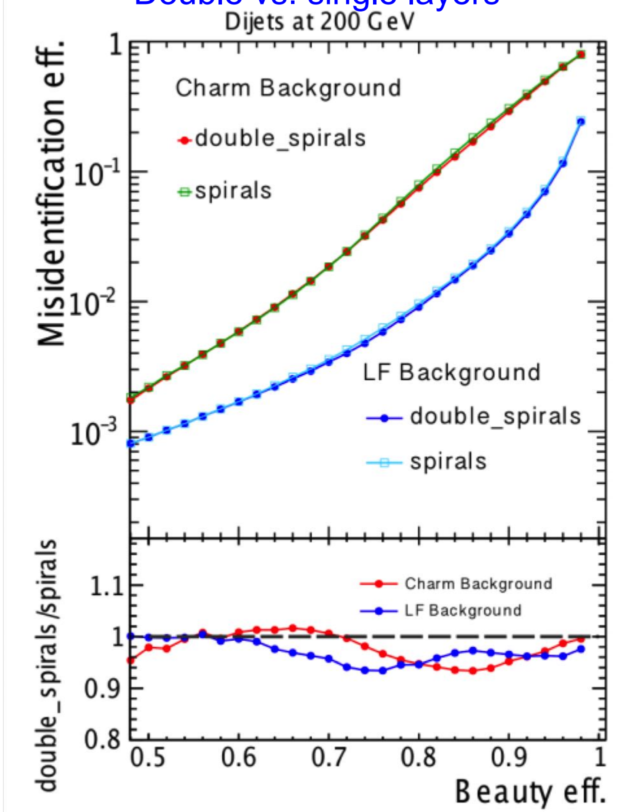
Single layers



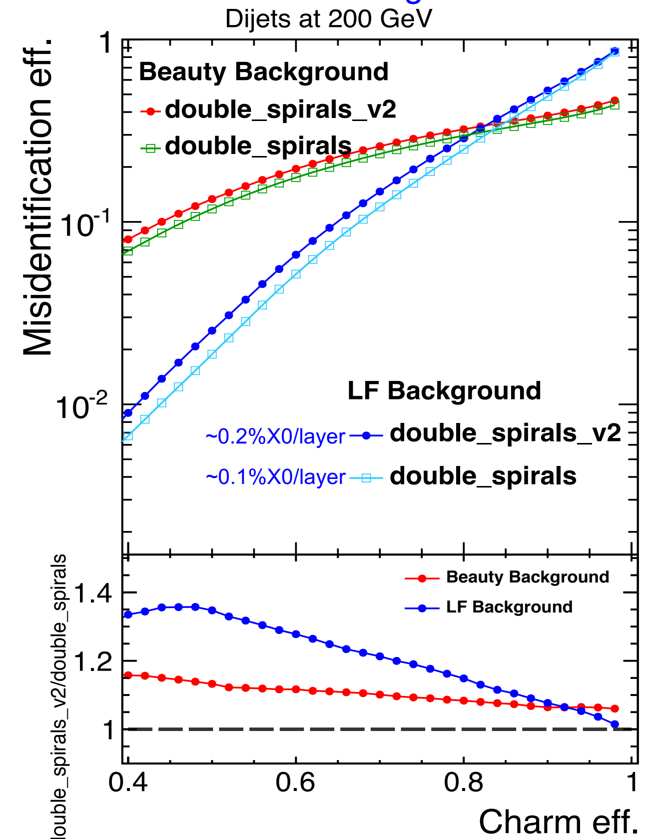
Double layers



Double vs. single layers

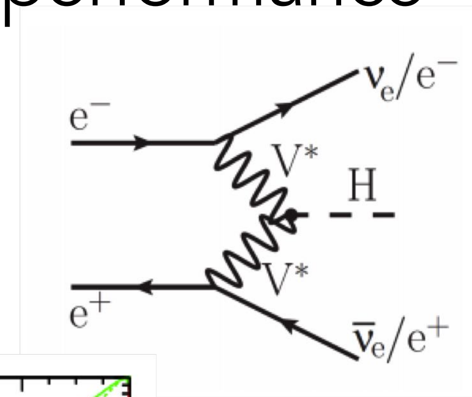


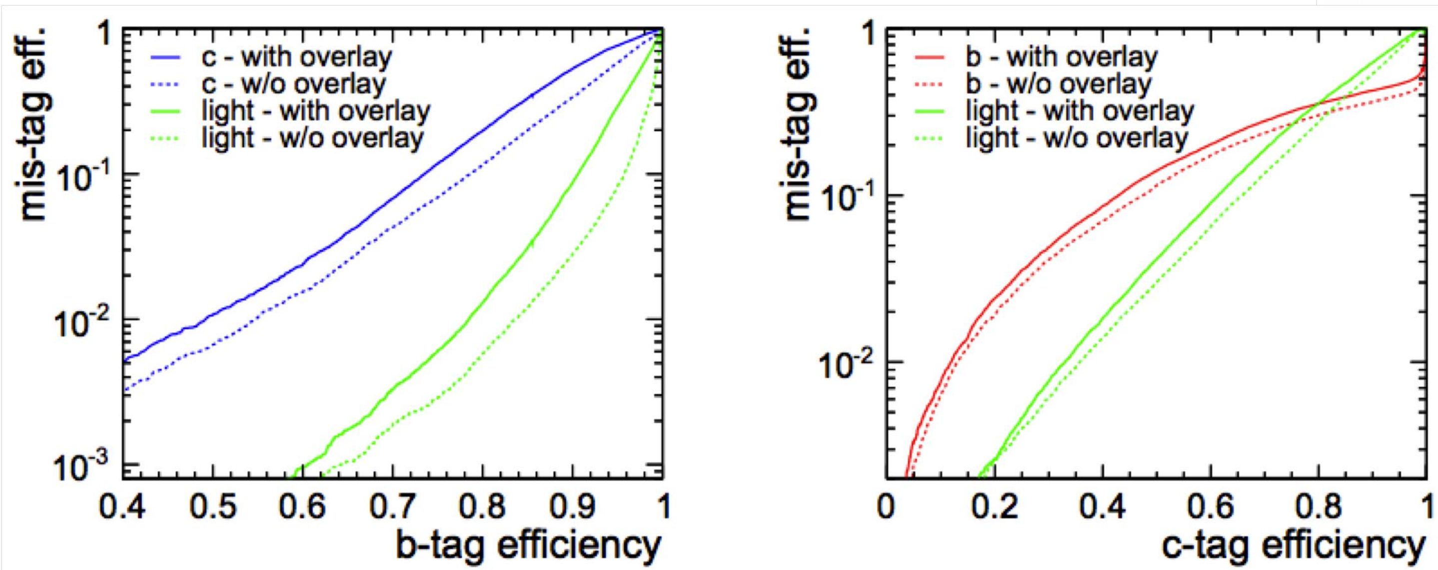
Material budget



Flavor tagging: impact on physics performance

- $e^+e^- \rightarrow H\nu\nu$: dominating Higgs production process at √s=3 TeV
- σ × BR measurement for the decays to bb and cc
- flavor tagging crucial for achievable precision





√s=3 TeV
L_{int}=2 ab^{-1}

$p_{T,jet}$~70 GeV
E_{jet}~130 GeV

channel	stat. unc. on σxBR	change for +/-20% fake r.
H→bb	0.23%	0.24% / 0.21%
H→cc	3.1%	3.6% / 2.6%

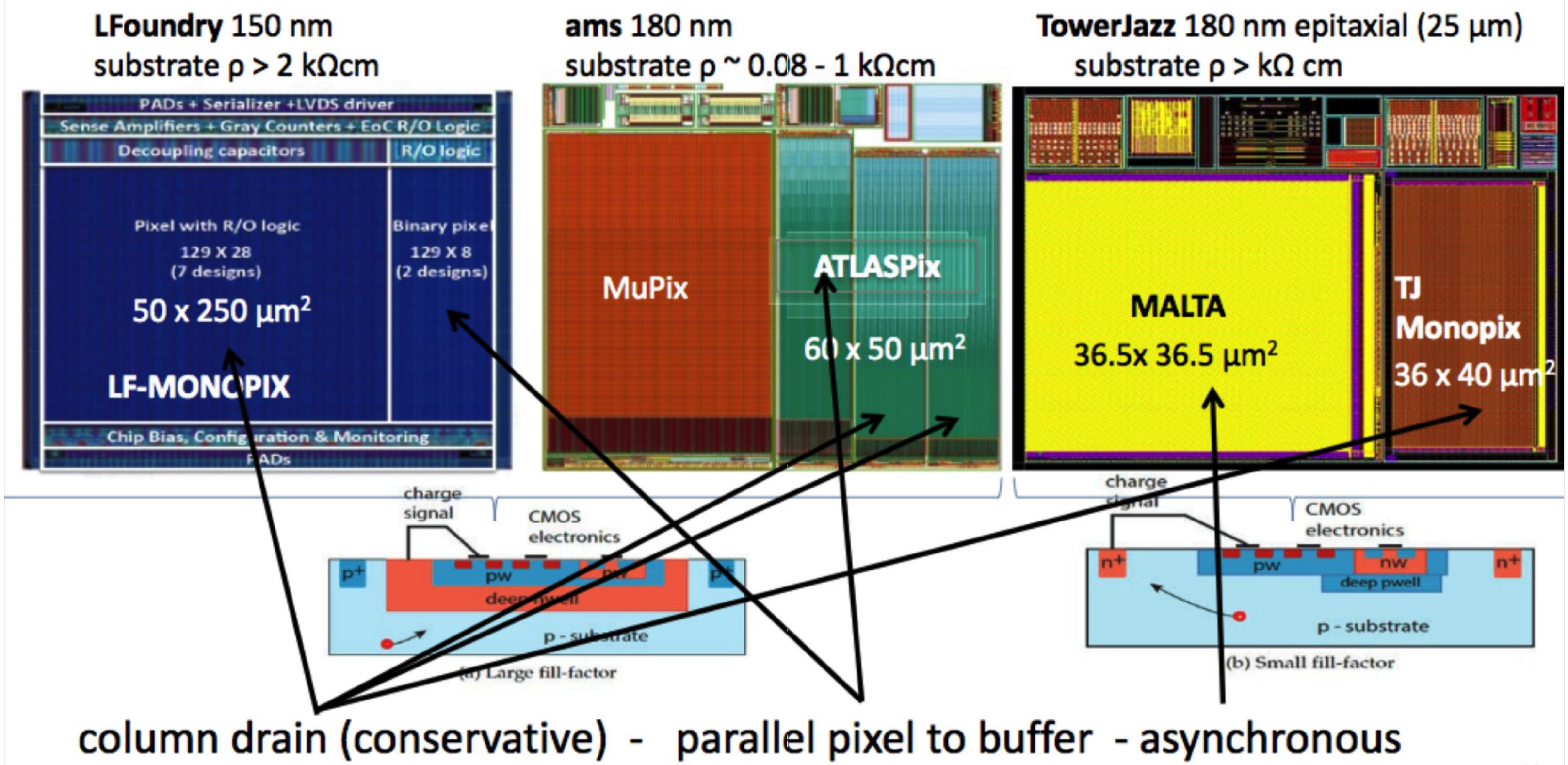
LCD-Note-2011-036, CLICdp Note-2014-002

- consider ±20% change in fake rates
- sizeable effect, in particular for H→cc: 30% more integ. luminosity required for same precision when increasing fake rate by 20% (>1 year of additional running!)

CMOS sensor developments for ATLAS

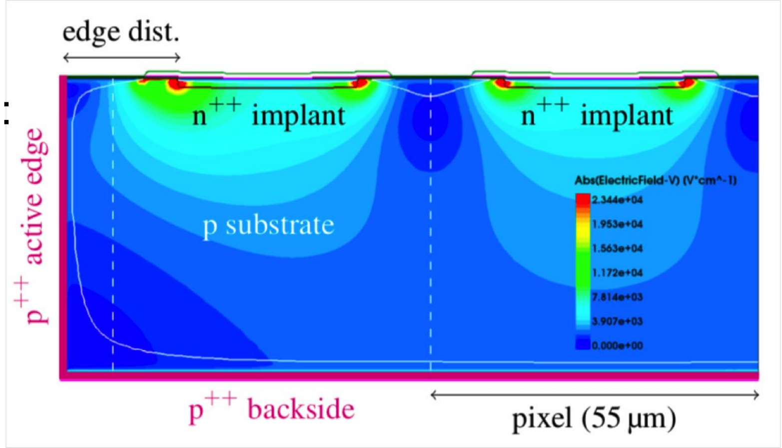
H. Pernegger @ BTT7
https://indico.cern.ch/event/731649

- Collaboration of 25 institutes
- Targeted towards outermost ITK pixel layer

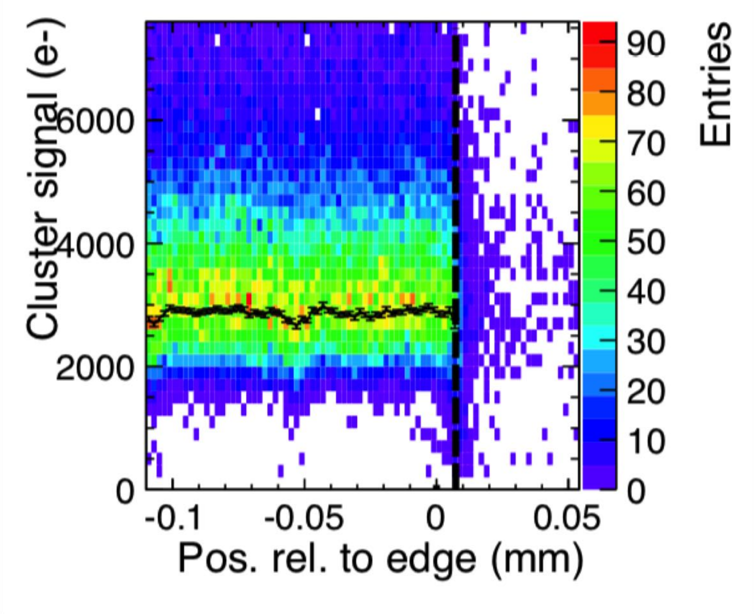


Active-edge sensors

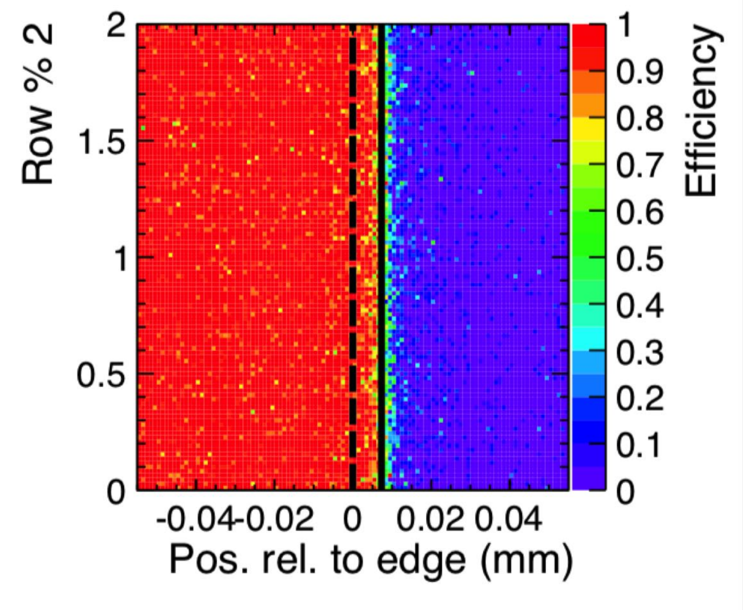
- Deep Reactive Ion Etching (DRIE) process (Advacam):
  - Implantation on the sensor sidewalls: extension of the backside electrode to the edge
  - Efficiency extends to the physical edge → allows for seamless tiling of sensors



Cluster signal at the edge of 50 μm sensor



Edge efficiency 50 μm sensor

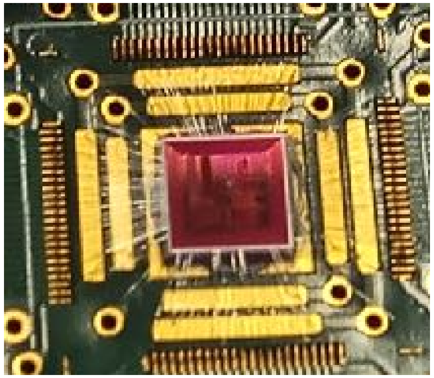


→ Active-edge sensors fully efficient up to the cut edge

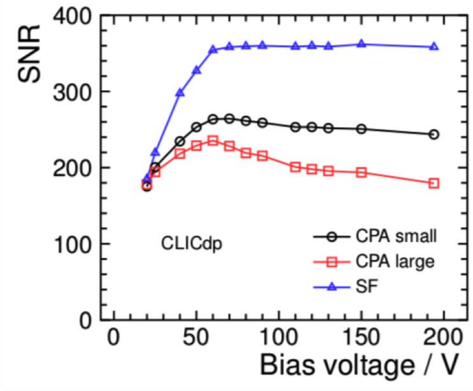
Cracow SOI sensors

- Cracow SOI test chip in 200 nm LAPIS SOI process, with various geometries and technology parameters: >=30x30 μm^2 pitch, single SOI and double SOI, rolling shutter r/o
- Test results for 300, 500 μm thickness, 30x30 μm^2 pitch
  >99% efficiency, σ_{SP}~2-5 μm

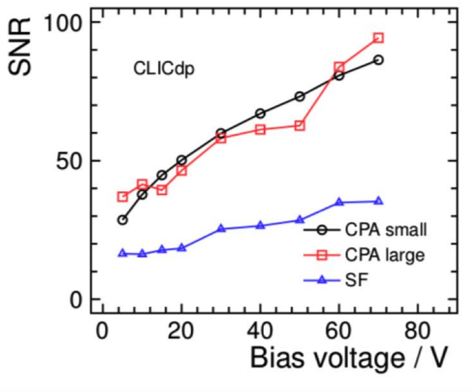
Cracow SOI test chip



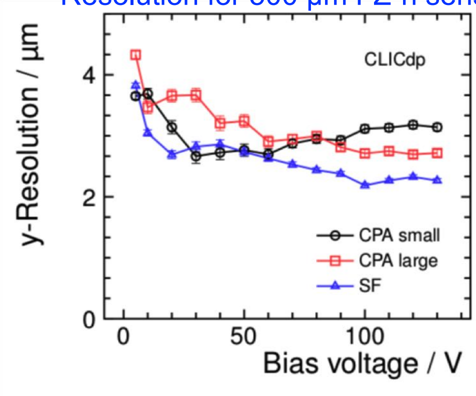
S/N for 500 μm FZ-n sensor



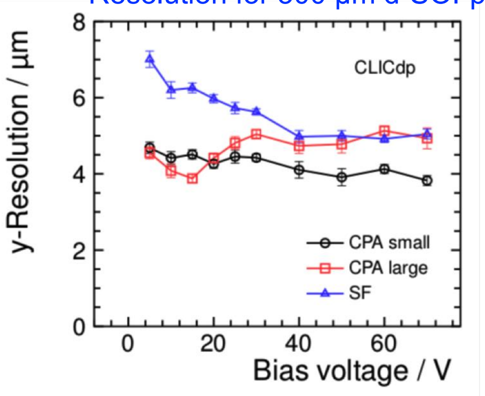
S/N for 300 μm d-SOI-p sensor



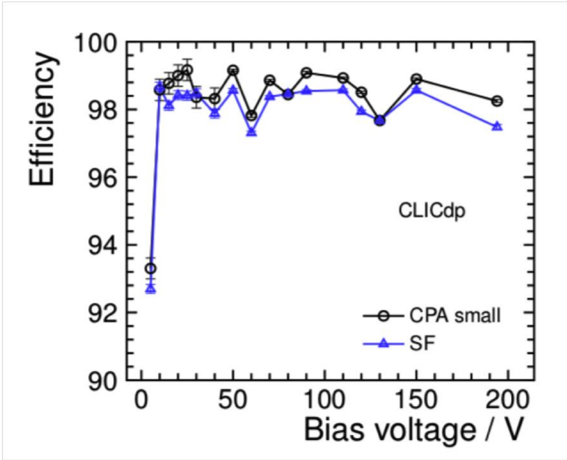
Resolution for 500 μm FZ-n sensor



Resolution for 300 μm d-SOI-p sensor



Efficienchy for 500 μm FZ-n sensor



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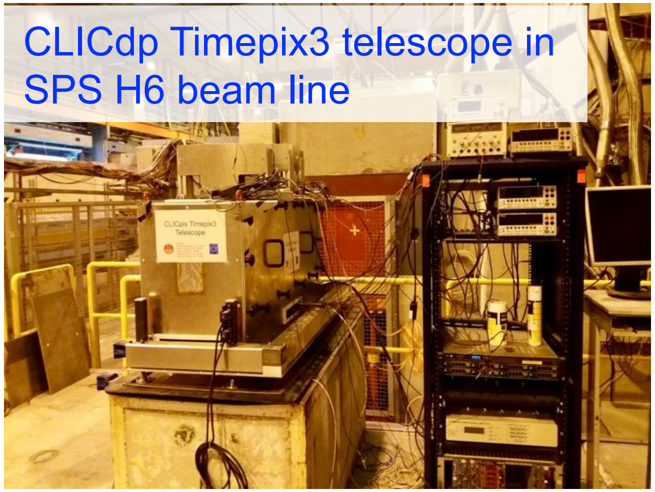
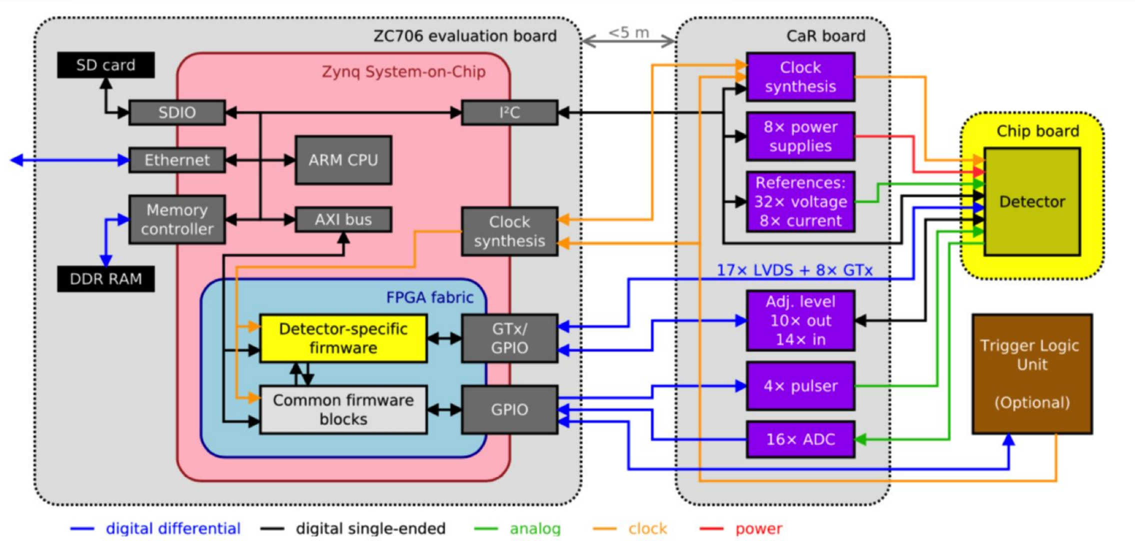
DAQ

- Lab and beam tests require flexible scalable DAQ hardware and software
- High-rate beam telescope with 7 Timepix3 detector planes (~1 MHz track rate, ≲2 µm resolution, ~1 ns time resolution), SPIDR r/o system (NIKHEF/CERN)
- CaRIBOu universal r/o system developed with ATLAS:
  - System-on-Chip (SoC) architecture
  - Peary DAQ software in Linux system inside FPGA core
  - Integration of CLICpix2, C3PD, ATLASpix

CLICdp Timepix3 telescope in SPS H6 beam line

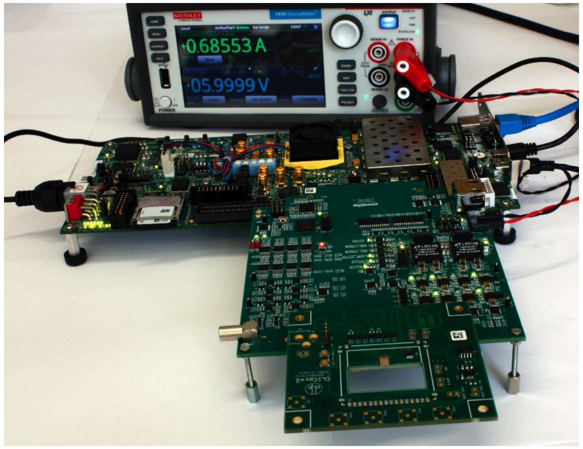


CaRIBOu hardware architecture



Universal r/o system proved very useful for lab + beam tests
→ could be suitable for development phase of MUonE

CaRIBOu with CLICpix2 r/o ASIC

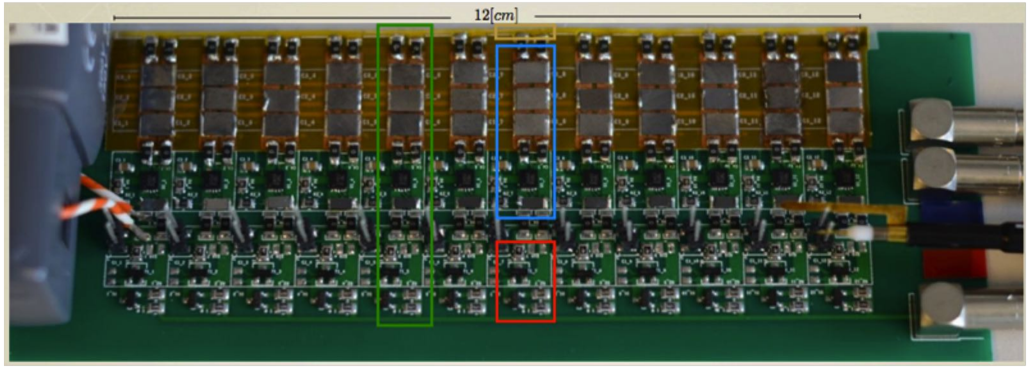


Powering

- Powering concept has major impact on material budget and heat load
- Small duty cycle of CLIC machine (<10^{-5}) allows for power pulsing, reducing average power consumption

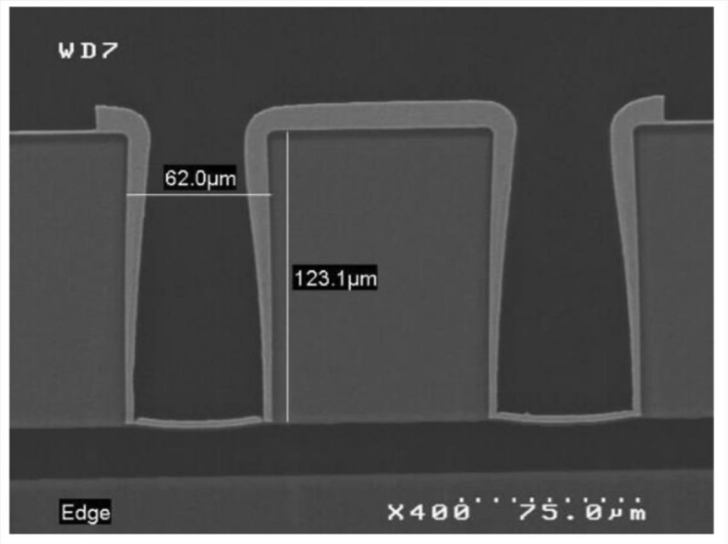
- Prototypes for low-mass power pulsing and power delivery concept for vertex detector
- Local energy storage and voltage regulation
- Small continuous current through low-mass Al cables, stable voltages for r/o ASICs
- ~0.1%X0 material in detector area, expected to decrease to 0.04%X0 in future
- Through-Silicon-Via (TSV) interconnect process (developed for Timepix3 ASICs)

Power-pulsing prototype



CLICdp-Note-2015-004

TSV in Medipix3RX

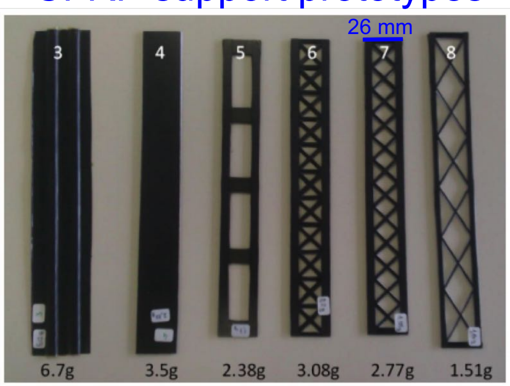


Mechanical integration

Material budget allows for only ~0.1%X0 from cables+supports in vertex region, <1%X0 in tracker
→ Development of low-mass supports with sufficient rigidity required
→ Low-mass services, optimized routing concepts

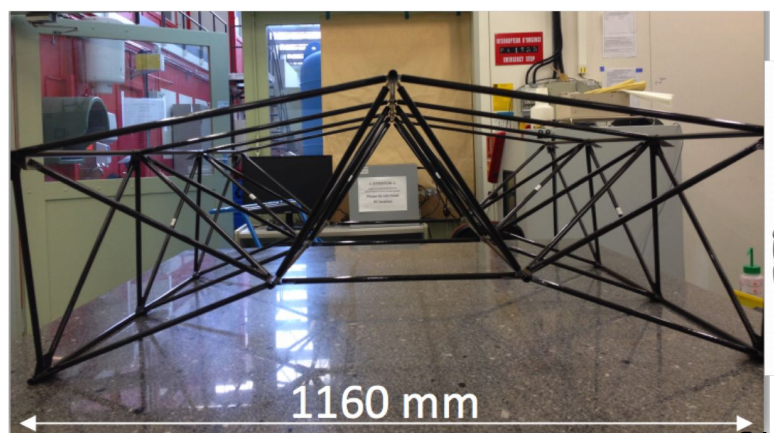
- Low-mass CFRP stave prototypes for vertex detector, FE simulations
- Concept for supports, beam pipe and cabling in vertex region, FE simulations
- Low-mass tracker support-structure concept, validated in FE simulations
- Prototype for outer tracker support segment

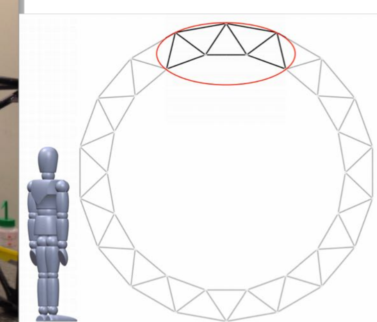
CFRP support prototypes



X/X0					
0,156 %	0,134 %	0,091 %	0,118 %	0,106 %	0,058 %

Prototype of outer barrel tracker support structure





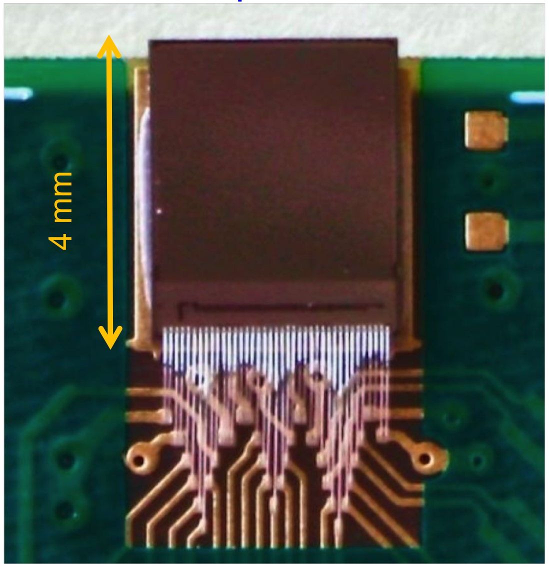
CLICdp-Note-2015-002

CLICpix2 r/o ASIC

- New CLICpix2 in same 65 nm process as CLICpix:
  - Increased matrix size to 128 × 128 pixels
  - Longer counters for charge (5-bit) and timing (8-bit) measurements
  - Improved noise isolation and removal of cross-talk issue observed in first CLICpix
  - More sophisticated I/O with parallel column readout and 8/10 bit encoding
  - Integrated test pulse DACs and band gap

- Test results with chips from Multi-Project-Wafer-Run
- Same chip on RD53 wafer, received in Dec 2017 (change from 5+1 to 7+1 metal layers) → access to full wafers for bump-bonding process development

CLICpix2



CLICpix2 analog F/E specifications

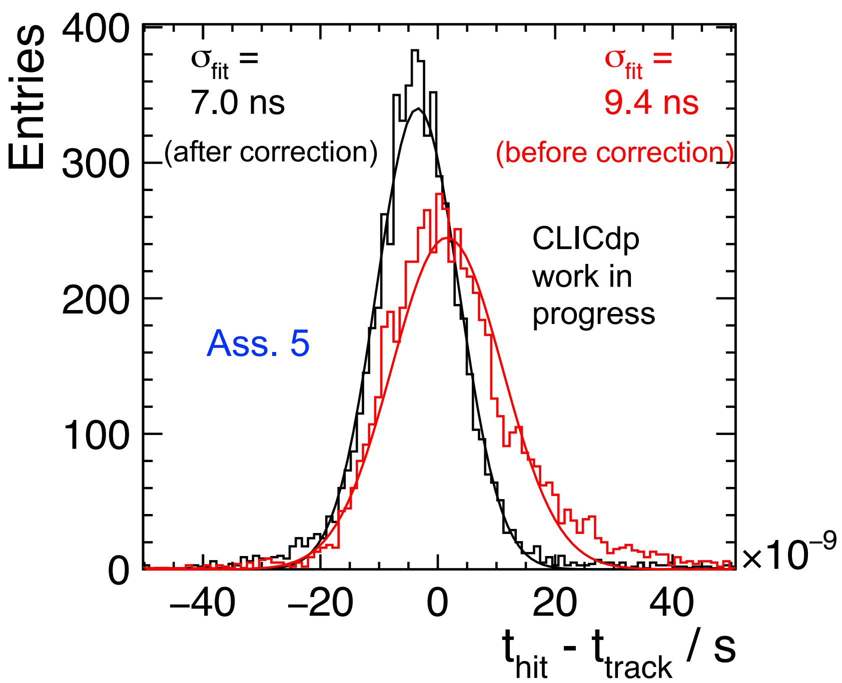
Parameter	Value
Power dissipation	≤ 12 μW
Area	≤ 12.5x25 μm^2
Input charge, Q_{in}	nominal 4 ke-, max. 40 ke-
Minimum threshold, $Q_{th,min}$	≤ 600 e-
Equivalent input-referred noise, $Q_{n,in}$	≤ 70 e-
ToT dynamic range	≥ 40 ke-
ToA accuracy	≤ 10 ns
Total ionizing dose (for 10 yr)	1 Mrad
Input charge types	e-, h+
Testability	in-pixel test pulse (i.e. Q_{test}) injection

C3PD+CLICpix2 time resolution

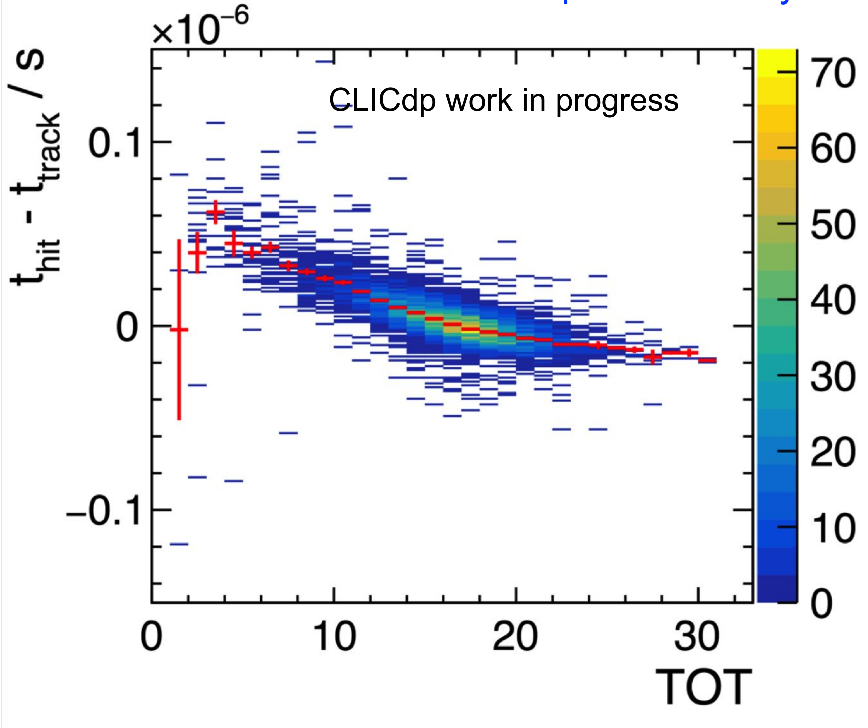
- Track time resolution of CLICdp Timepix3 telescope <~1 ns
  → precise characterization of DUT timing capabilities
- CLICpix2: 100 MHz ToA clock → 10 ns time binning
- Gauss fit of time residuals shows width of ~9 ns
- Tail towards later times, as expected from time walk

→ Time residual reduced to ~7 ns after time-walk correction

Hit time residuals in C3PD+CLICpix2 assembly



Time Walk in C3PD+CLICpix2 assembly



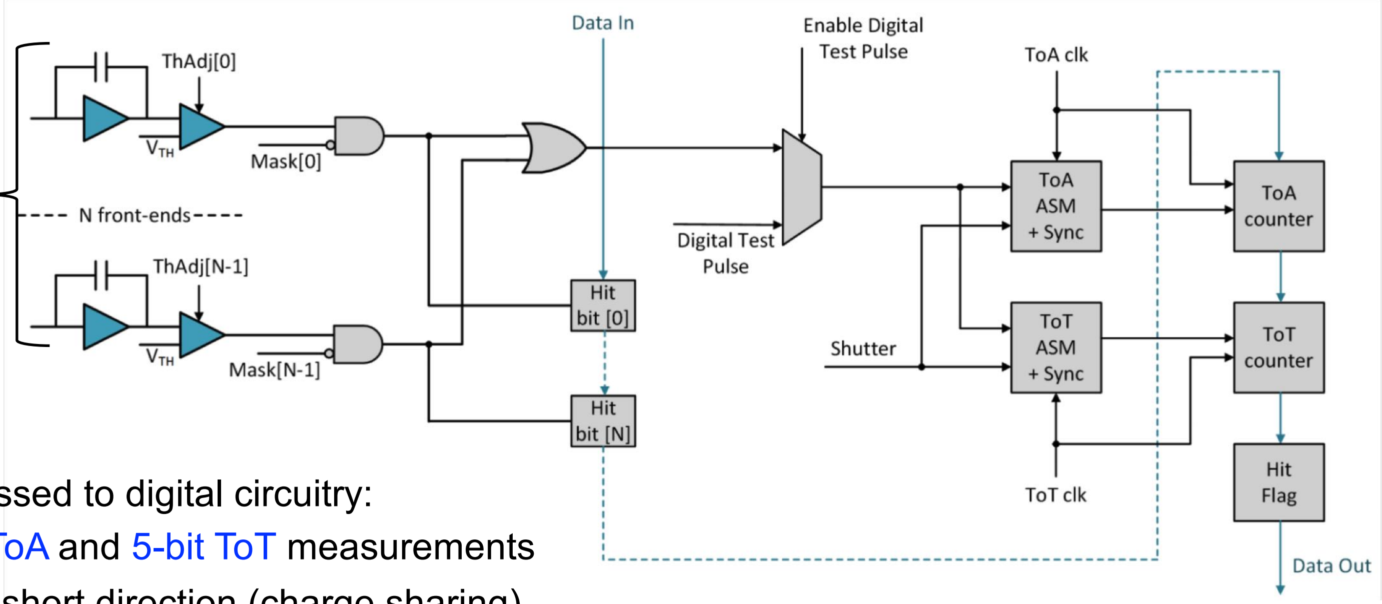
CLICTD monolithic HR-CMOS tracker chip

Good performance of studied 180 nm HR-CMOS technology with respect to requirements of CLIC tracker
→ Technology used for ongoing design of a fully integrated chip for the CLIC tracker

CLIC Tracker Detector (CLICTD) – monolithic HR-CMOS sensor with 30 μm x 300 μm pixels

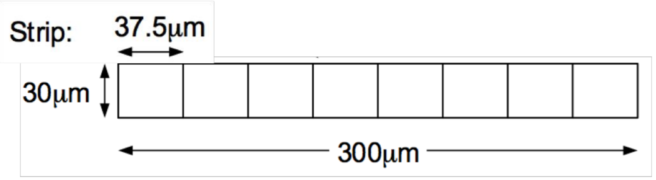
Segmented macro-pixel structures to maintain advantages of small collection diode (prompt and fully efficient charge collection) while reducing digital logic:

Discriminator output of 8 collection diodes combined in logical OR



Output of logical OR passed to digital circuitry:

- Simultaneous 8-bit ToA and 5-bit ToT measurements
- Expect σ_{SP}~7 μm in short direction (charge sharing)
- Hit bit pattern → maintain good resolution also in long direction
- 100 MHz clock to achieve 10 ns time binning



CLIC schedule

2013 – 2019

Development Phase
Development of a project plan for a staged CLIC implementation in line with LHC results; technical developments with industry, performance studies for accelerator parts and systems, detector technology demonstrators

2020 – 2025

Preparation Phase
Finalisation of implementation parameters, preparation for industrial procurement, pre-series and system optimisation studies, technical proposal of the experiment, site authorisation

2026 – 2034

Construction Phase
Construction of the first CLIC accelerator stage compatible with implementation of further stages; construction of the experiment; hardware commissioning

2020
Update of the European Strategy for Particle Physics

2026
Ready for construction

2035
First collisions