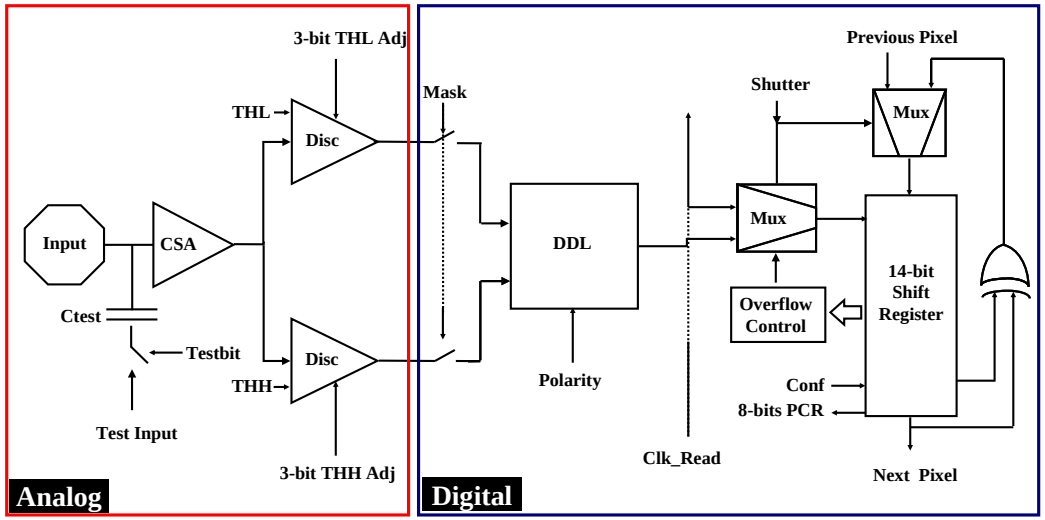
The Timepix chip family

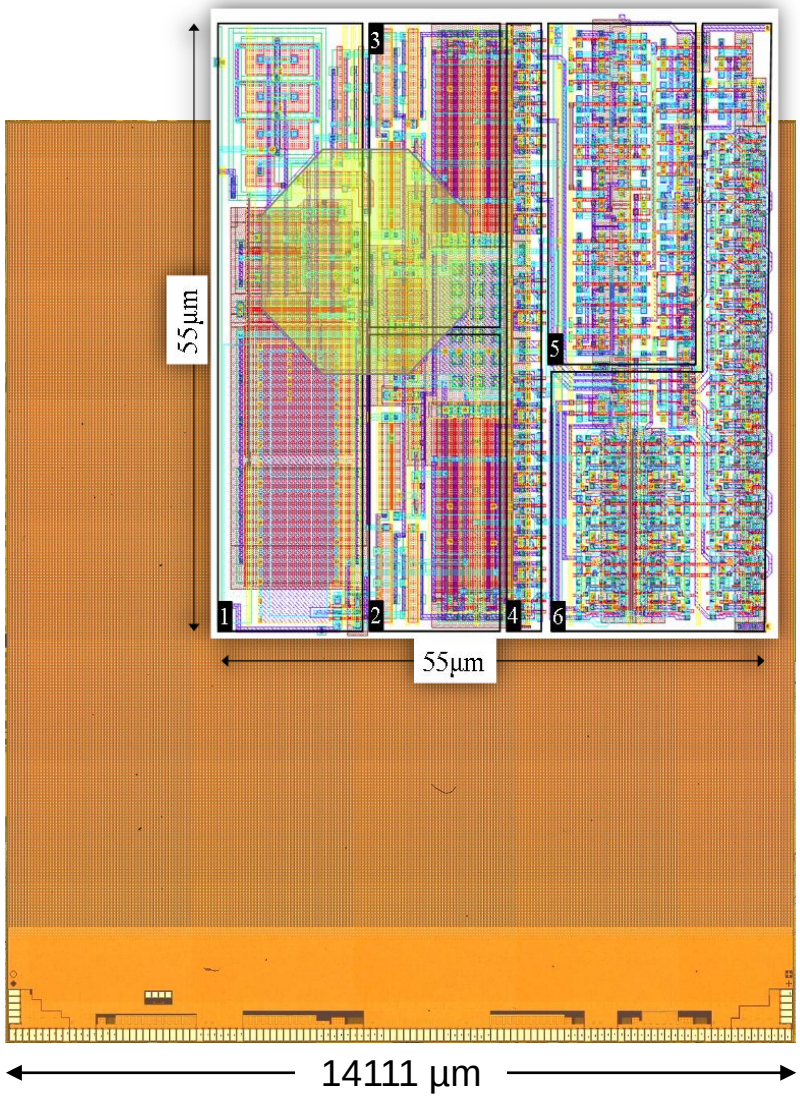
Xavier Llopart

18th September 2019

Medipix2: Mpix2MXR20 (2005)



Measured pixel gain	10.7 mV/ke$^-$
Measured ENC	~110 e$^-$ rms
Threshold dispersion before equalization	~400 e$^-$ rms
Threshold dispersion after equalization	~95 e$^-$ rms
Minimum detectable charge	~900 e$^-$
On-chip threshold DAC step	~413 µV or ~40 e$^-$
On-chip threshold DAC INL over the full range	<2 LSB (80 e$^-$)
Voltage DACs Temperature dependence	5.6 e$^-$/°C
Pixel counter depth-Overflow control	11810-Yes
Maximum serial readout clock	~180 MHz
Pixel static power consumption	~8 µW



Medipix2 Collaboration

- U INFN Cagliari
- CEA-LIST Saclay
- CERN Genève
- U Erlangen
- ESRF Grenoble
- U Freiburg
- U Glasgow
- IFAE Barcelona
- Mitthoegskolan
- MRC-LMB Cambridge
- U INFN Napoli
- NIKHEF Amsterdam
- U INFN Pisa
- FZU CAS Prague
- IEAP CTU in Prague
- SSL Berkeley

http://medipix.web.cern.ch/MEDIPIX/

From Mpix2MXR20 to Timepix

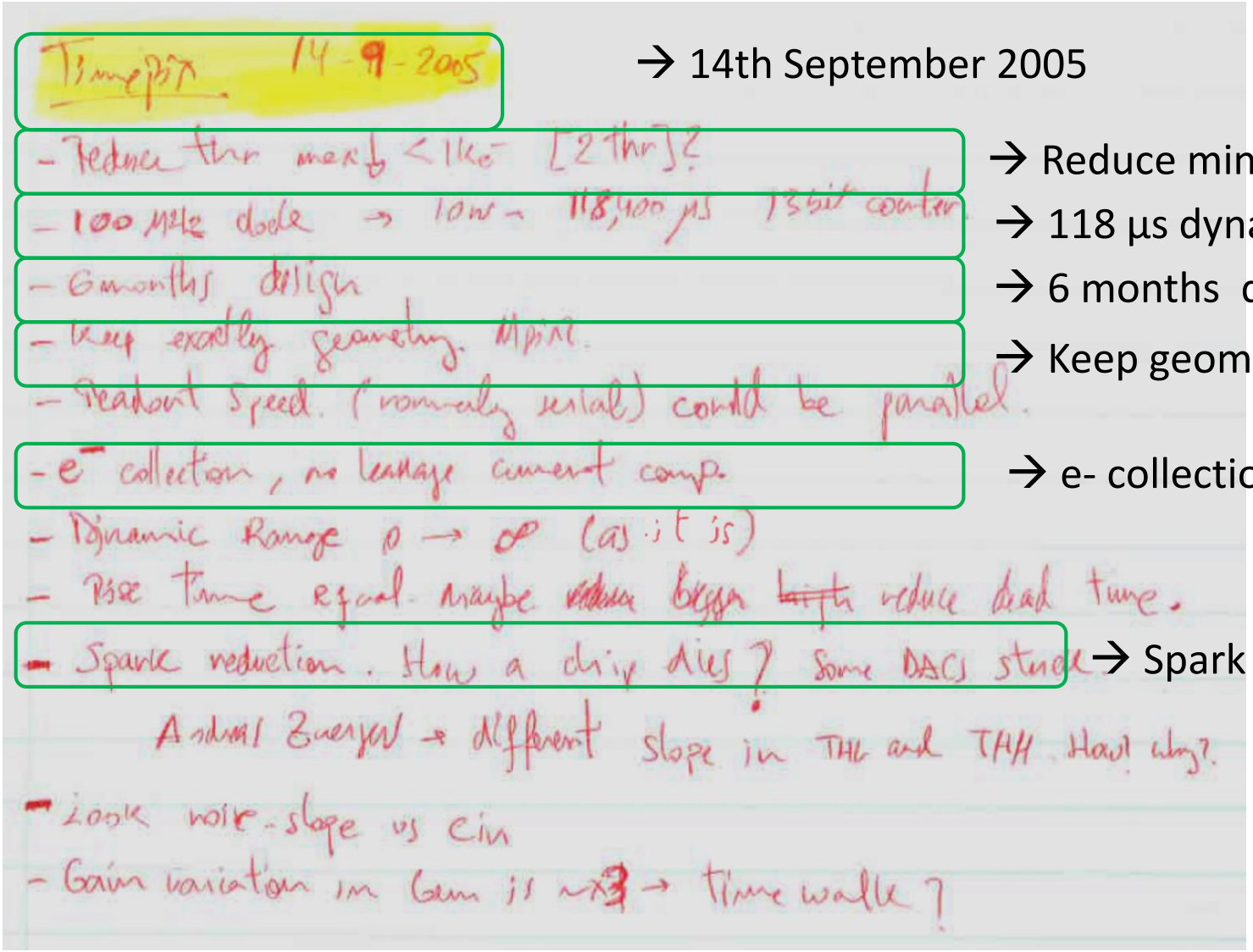
- First Idea by J. Visschers (NIKHEF): “Count arrival time by adding a clock in pixel”

- Design requested and funded by EUDet Collaboration:
  - EUDet collaboration finished in 2010 → AIDA

- Main features requested:
  - Change counter function from particle counting to arrival time measurement (clock tick counting) to provided depth dimension in gas detectors
  - Keep Timepix as similar as possible to Medipix2 series in order to benefit from large prior effort in R/O hardware and software

- Operating modes:
  - Particle counting
  - Arrival time:
    - 10ns resolution @100MHz
    - 118.1 µs dynamic range @100MHz

From Mpix2MXR20 to Timepix



→ 14th September 2005

→ Reduce min threshold

→ 118 µs dynamic range

→ 6 months design

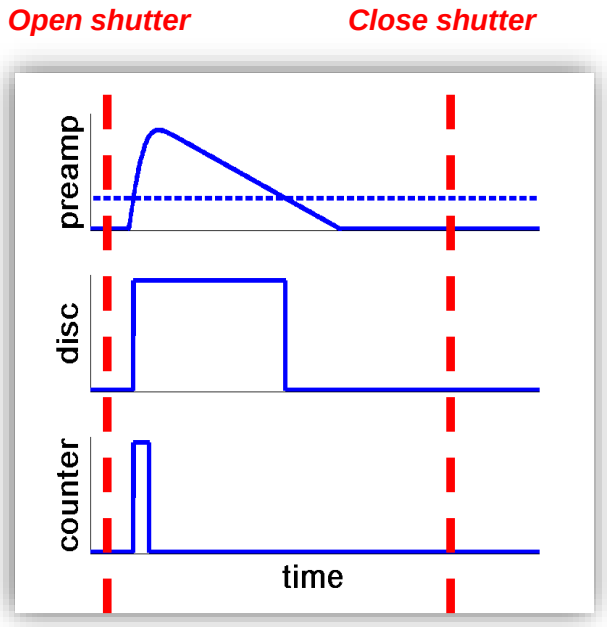
→ Keep geometry as Mpix2

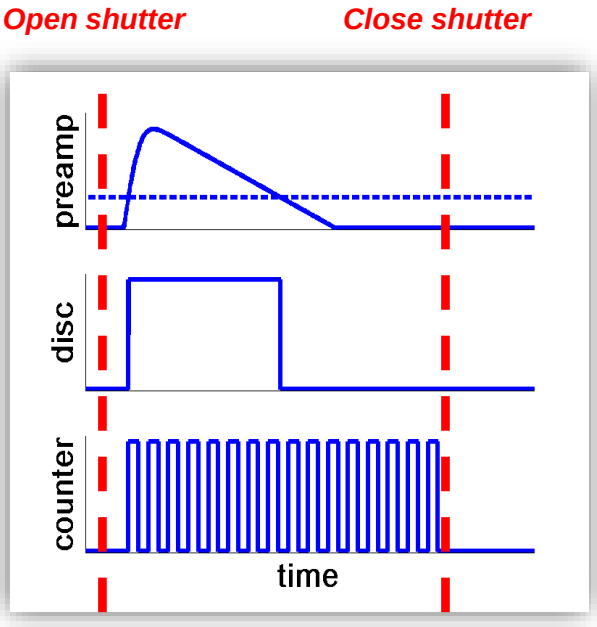
→ e- collection only (!?)

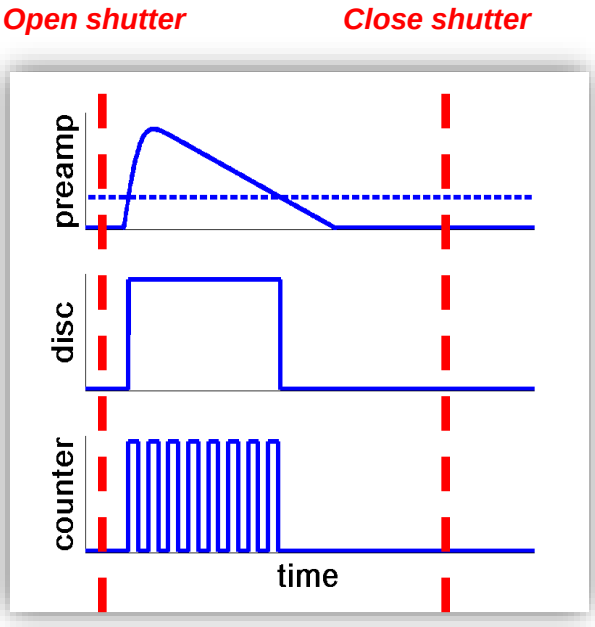
→ Spark reduction (!?)

Timepix Operation Modes

- Particle counting
- Arrival Time
- Time over threshold





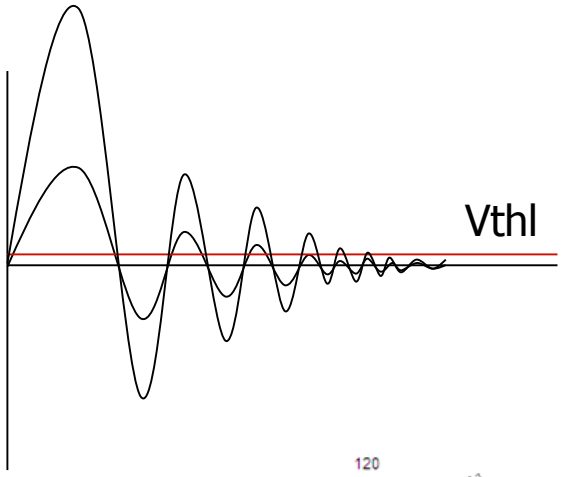


- TOT mode was added during the design phase:
  - Linear response up to ~300 Ke^-/pixel

First TOT measurements with a Medipix2 chip (I)

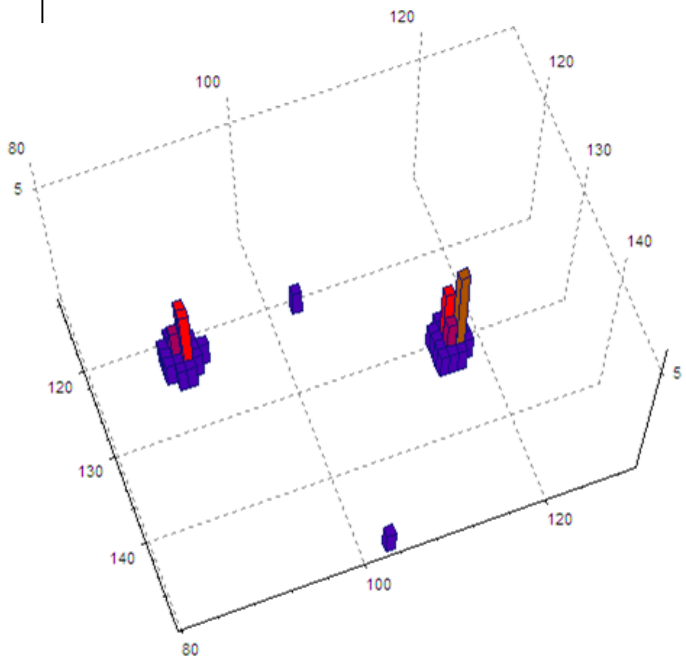
Medipix2: ADC using oscillating Front-End:

- Discharging in amplifier is too fast (Ikrum) → overshoots
- Several overshoots can cross threshold level → several counts per single event.
- Count depends on amplitude → **ADC in each pixel**



Tests:

- Tests with Medipix2 varying Ikrum
- Temperature of the device held low (10°C) to decrease noise
- Alpha particle source used (alpha energy ~5MeV).
- Up to 6 counts per pixel per event

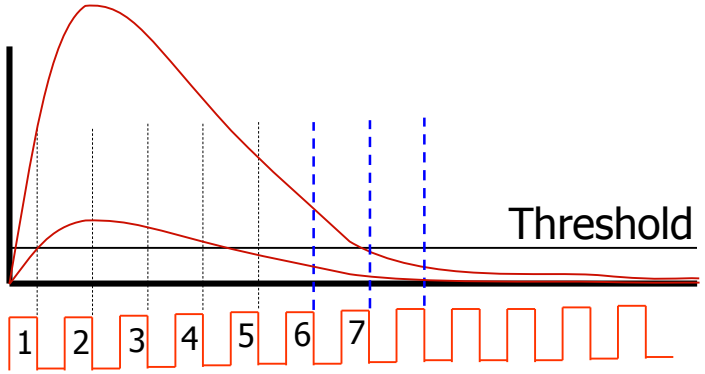


Jan Jakůbek
Medipix Meeting CERN, 21st September 2005

First TOT measurements with a Medipix2 chip (II)

Medipix2: ADC by high frequency shutter:

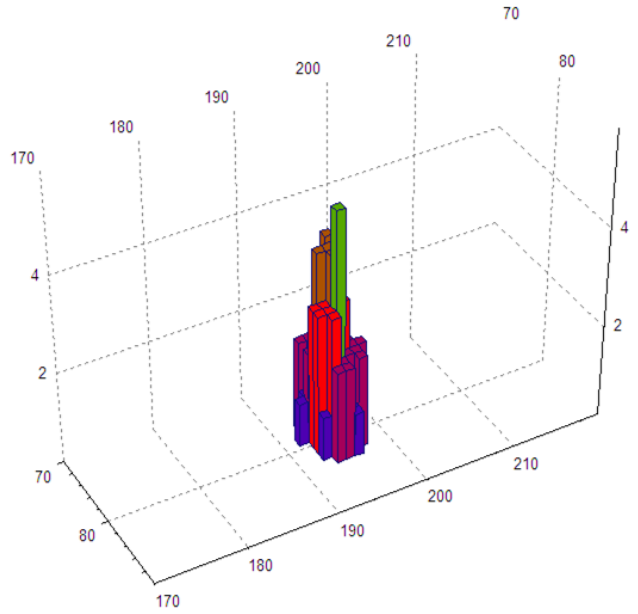
- Counter is incremented if
  - signal is higher then threshold
  - and shutter is opened
- This condition can be valid several times during single pulse
- Number of counts depends on amplitude → ADC
- Response can be linear if constant current is used for discharging.
- Principle is similar to Wilkinson ADC type.



Tests:

- Medipix2 with 5MHz on shutter input irradiated by cosmic rays.
- Playing with Ikrum parameter
- Up to 10 counts per event.

=> Resolution of 7-8 bits is possible at 100MHz

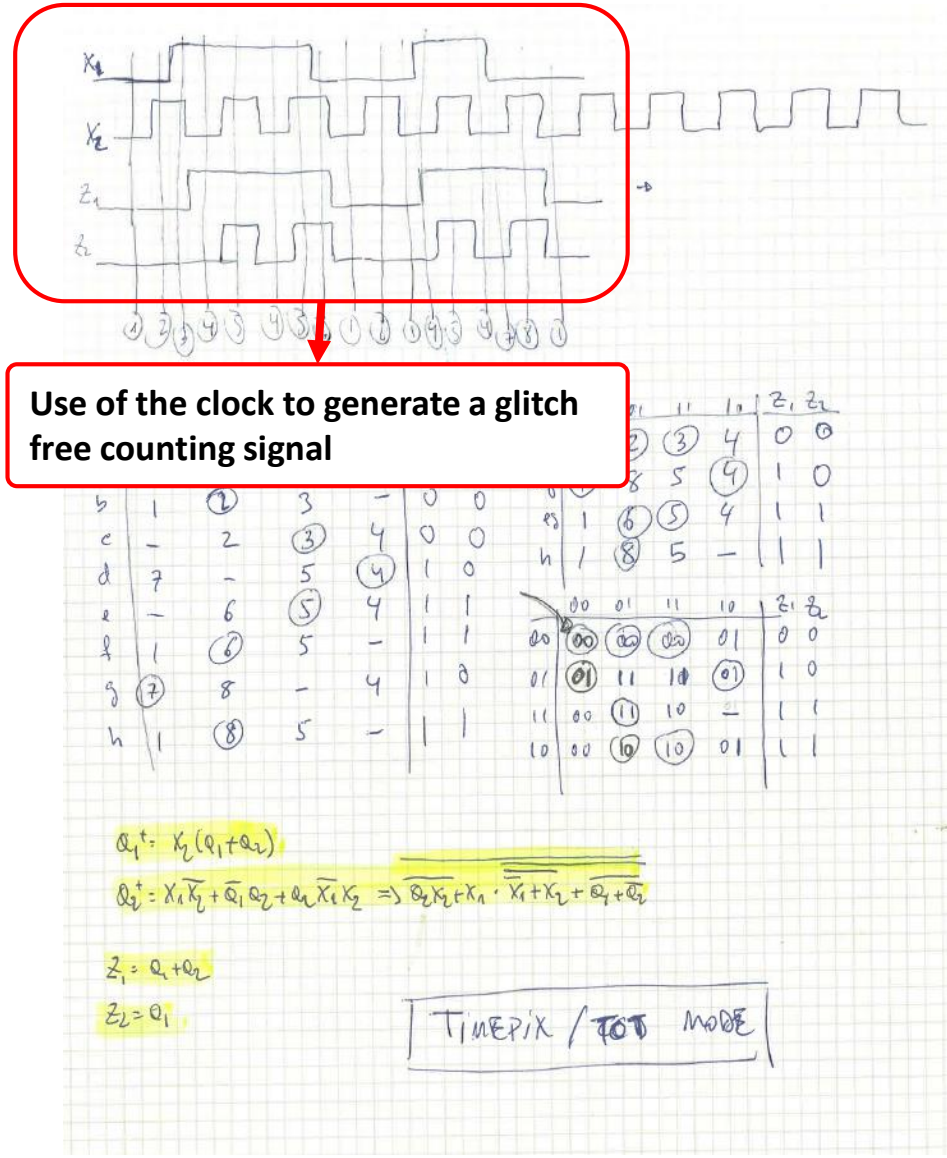


Disadvantage:

- Slightly higher noise

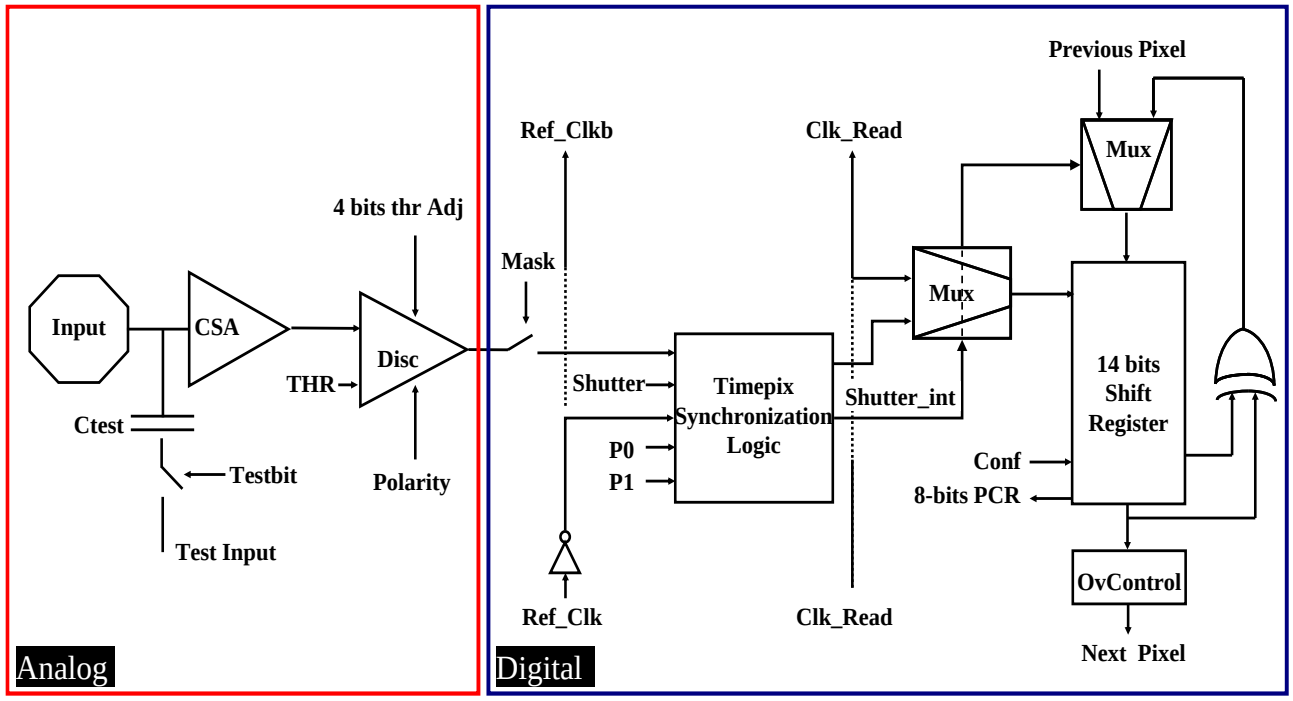
Jan Jakůbek
Medipix Meeting CERN, 21st September 2005

On-pixel Asynchronous state machine



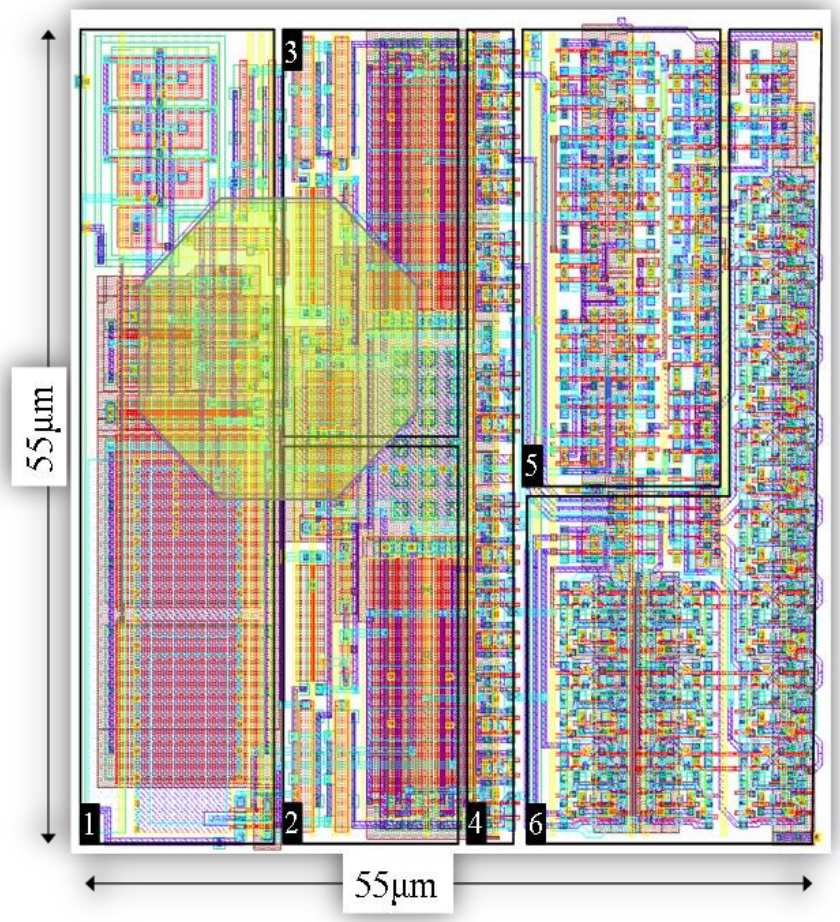
Timepix pixel schematic (2016)

- Improved CSA gain by adding a cascode in the OTA
- There is a single threshold with one 4-bit threshold adjustment DAC.
- Each pixel can be configured independently in three different operation modes (P0 and P1):
  - Arrival time mode
  - Energy mode (TOT)
  - Event counting
- In acquisition mode there is a counting clock (*Ref_Clk*) distributed to the entire pixel matrix which is synchronised with the discriminator output (*HIT*)

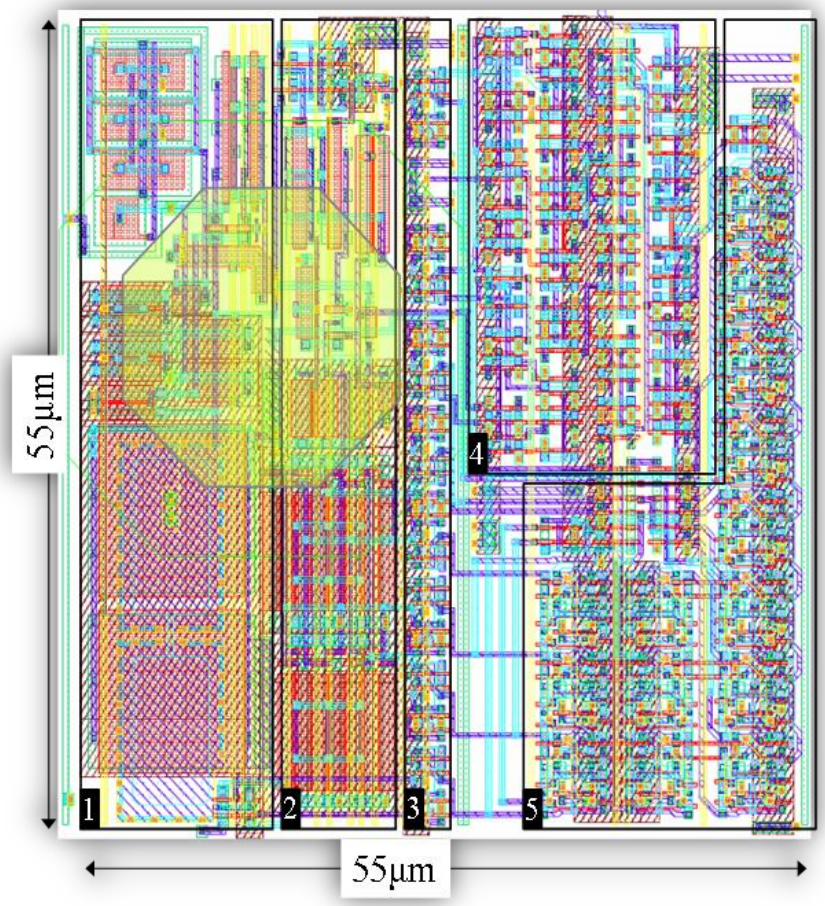


Mpix2MXR20 → Timepix Layout

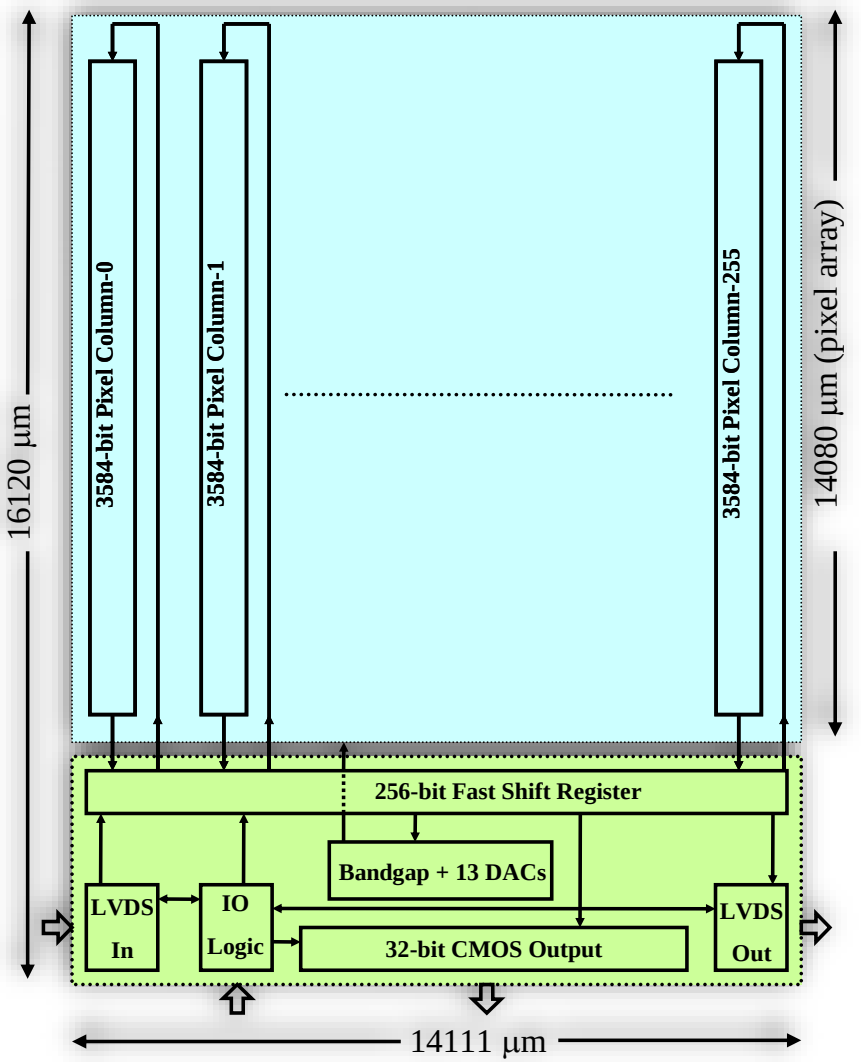
Mpix2MXR20 (2005) pixel layout



Timepix (2006) pixel layout



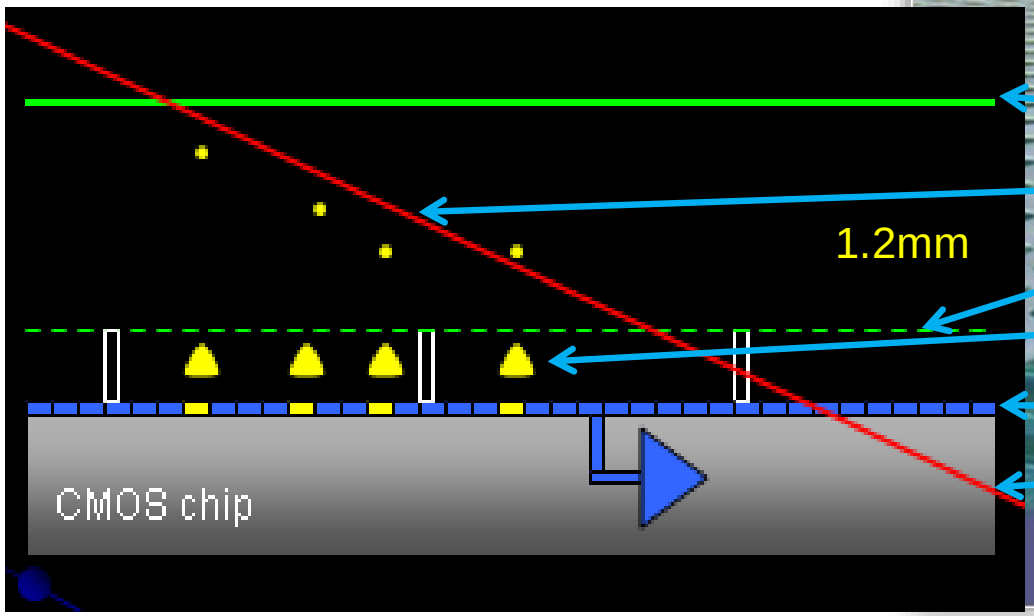
Timepix (2006) chip architecture

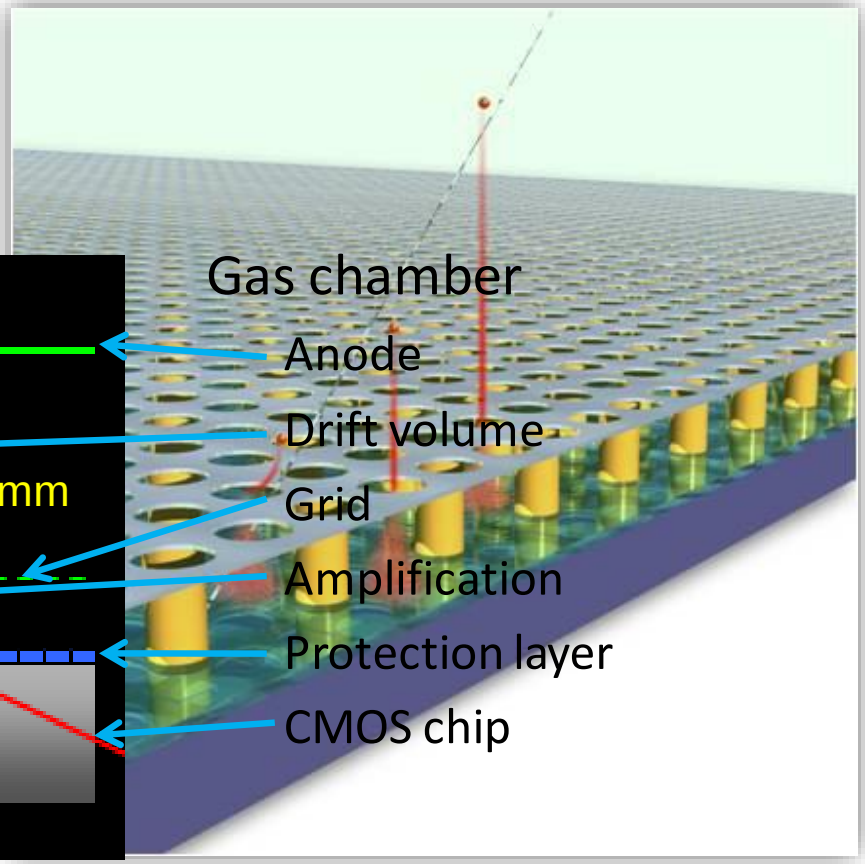


- Chip architecture almost identical to Mpix2MXR20
- In acquisition mode chip an external clock is used as a time reference (up to 100 MHz)
- 256x256 55µm square pixels
- Analog Power -> 440mW
- Digital Power (Ref_Clk=50MHz) → 220mW
- > 36M Transistors
- Medipix2 and Timepix was designed as a system on chip design:
  - On-chip digital global biasing:
    - 14 DACs + Bandgap
  - Simple control logic
  - Serial readout (@100MHz) → 9.17 ms
  - Parallel readout (@100MHz) → 287 µs
- Send to foundry on June 2006

Gaseous detectors

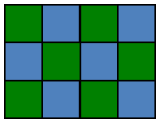
- Use of Timepix to measure the arrival time or energy of deposited primary electrons in a gas volume
- No bump-bonded detector

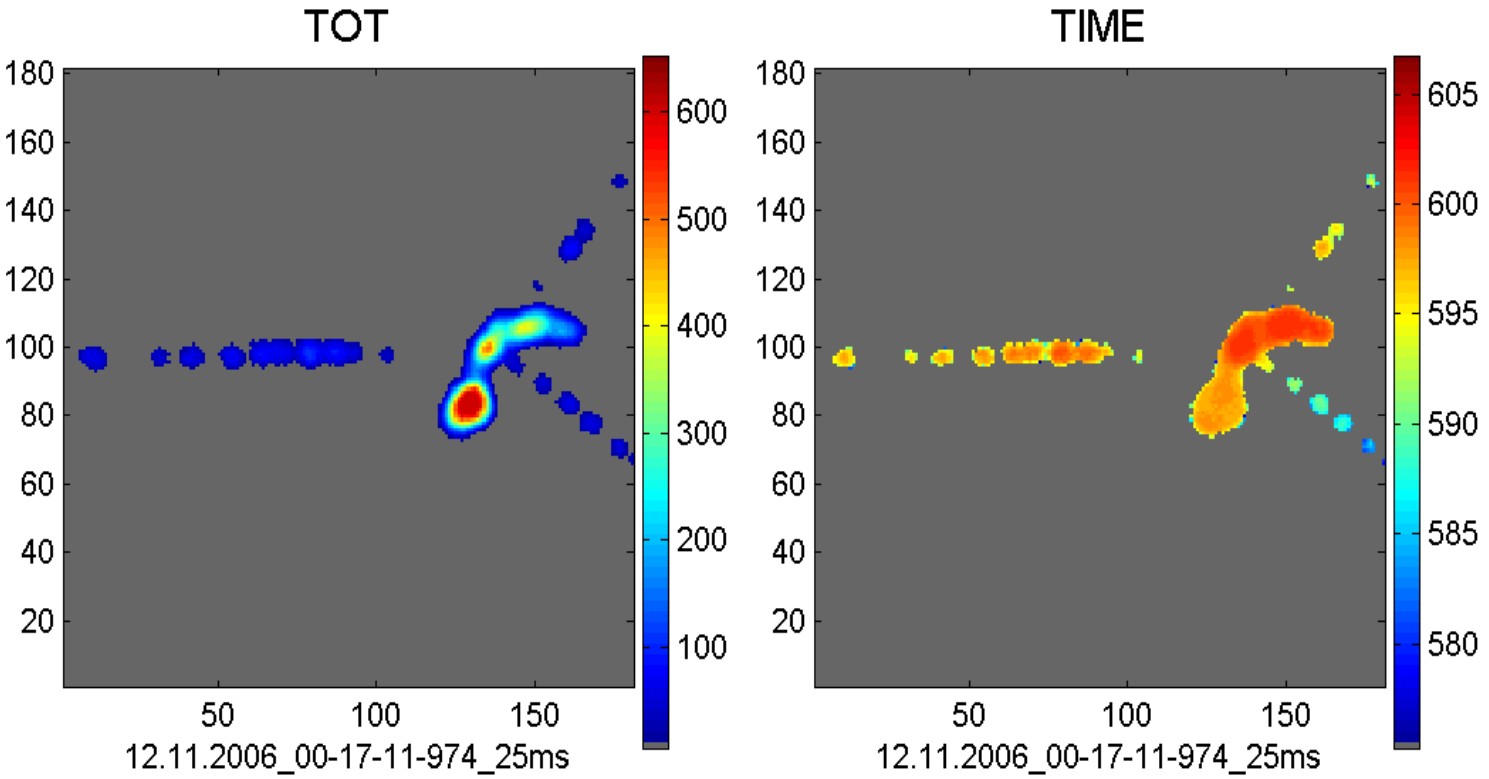




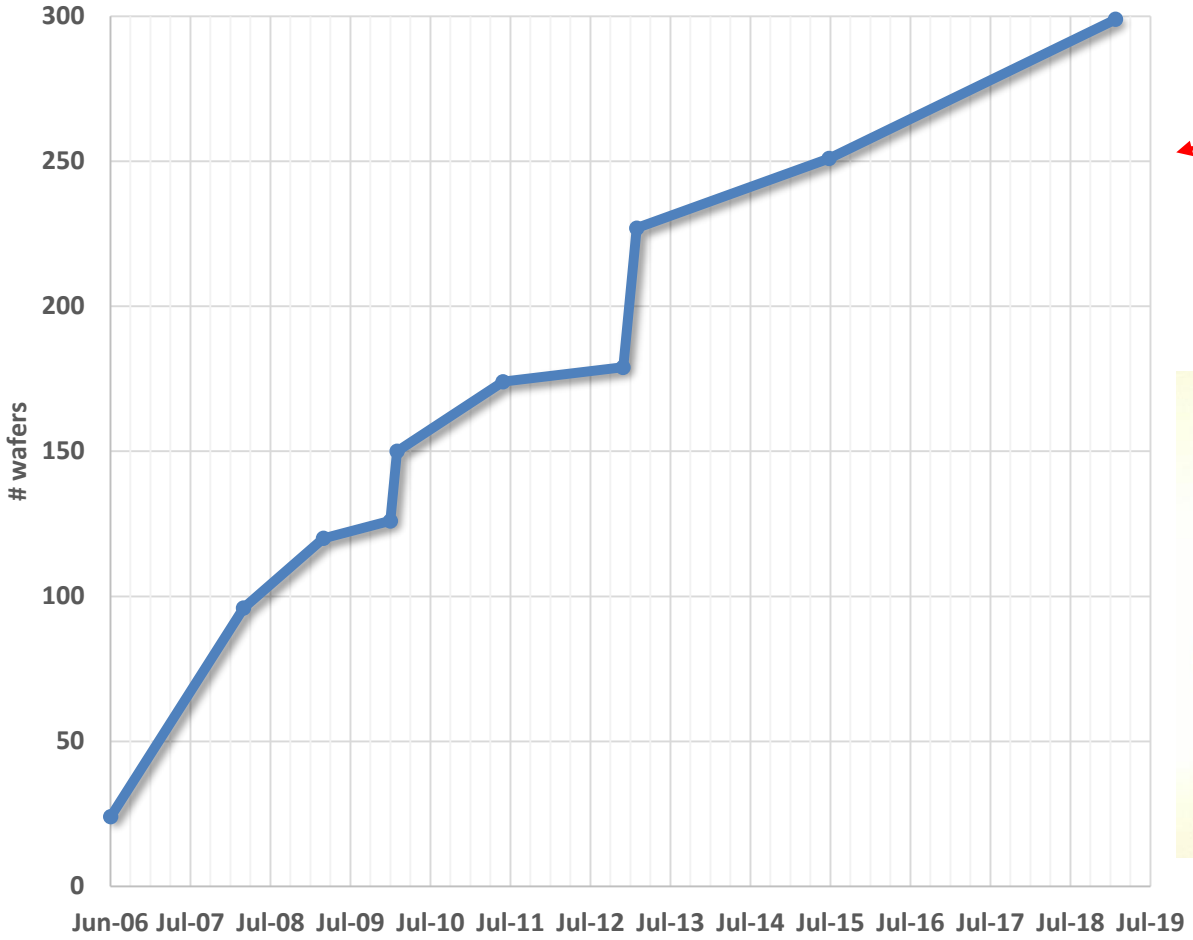
Timepix with 3-GEM detector

- DESY testbeam in November 2006 (A.Bamberger, U. Renz, M.Titov, X. Llopart)
- Checked-board pattern (TOT and TIME)



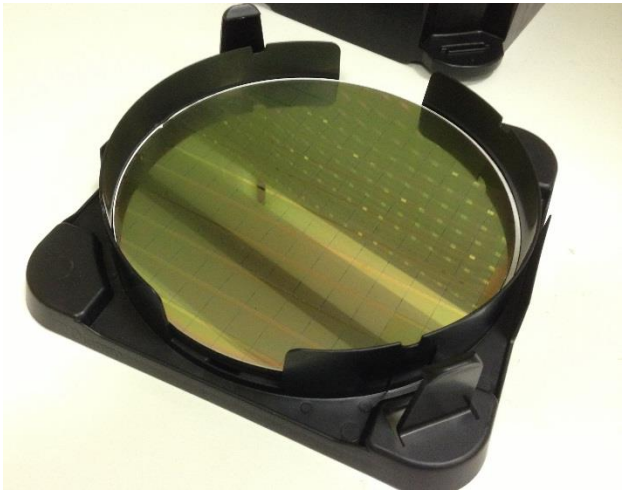


13 years of Timepix Production



299 wafers produced:

- 31395 chips
- > 2 billon pixels
- 6.3 m^2 active area



Medipix3 Collaboration (from 2005)

- University of Canterbury, Christchurch, New Zealand
- CEA, Paris, France
- CERN, Geneva, Switzerland,
- DESY-Hamburg, Germany
- Albert-Ludwigs-Universität Freiburg, Germany
- University of Glasgow, Scotland, UK
- Leiden University, The Netherlands
- NIKHEF, Amsterdam, The Netherlands
- Mid Sweden University, Sundsvall, Sweden
- IEAP, Czech Technical University, Prague, Czech Republic
- ESRF, Grenoble, France
- Universität Erlangen-Nurnberg, Erlangen, Germany
- University of California, Berkeley, USA
- VTT, Information Technology, Espoo, Finland
- KIT/ANKA, Forschungszentrum Karlsruhe, Germany
- University of Houston, USA
- Diamond Light Source, Oxfordshire, England, UK
- Universidad de los Andes, Bogota, Colombia
- University of Bonn, Germany
- AMOLF, Amsterdan, The Netherlands
- Technical University of Munich, Germany
- Brazilian Light Source, Campinas, Brazil

22 members

Timepix3 motivation

- Main driving requirements:
  1. Simultaneous TIME (TOA) and CHARGE (TOT) information per pixel
  2. Minimize dead time → Event-by-event readout and 0-supressed
  3. Monotonic TOT in both detection polarities
  4. Improve time measurements resolution

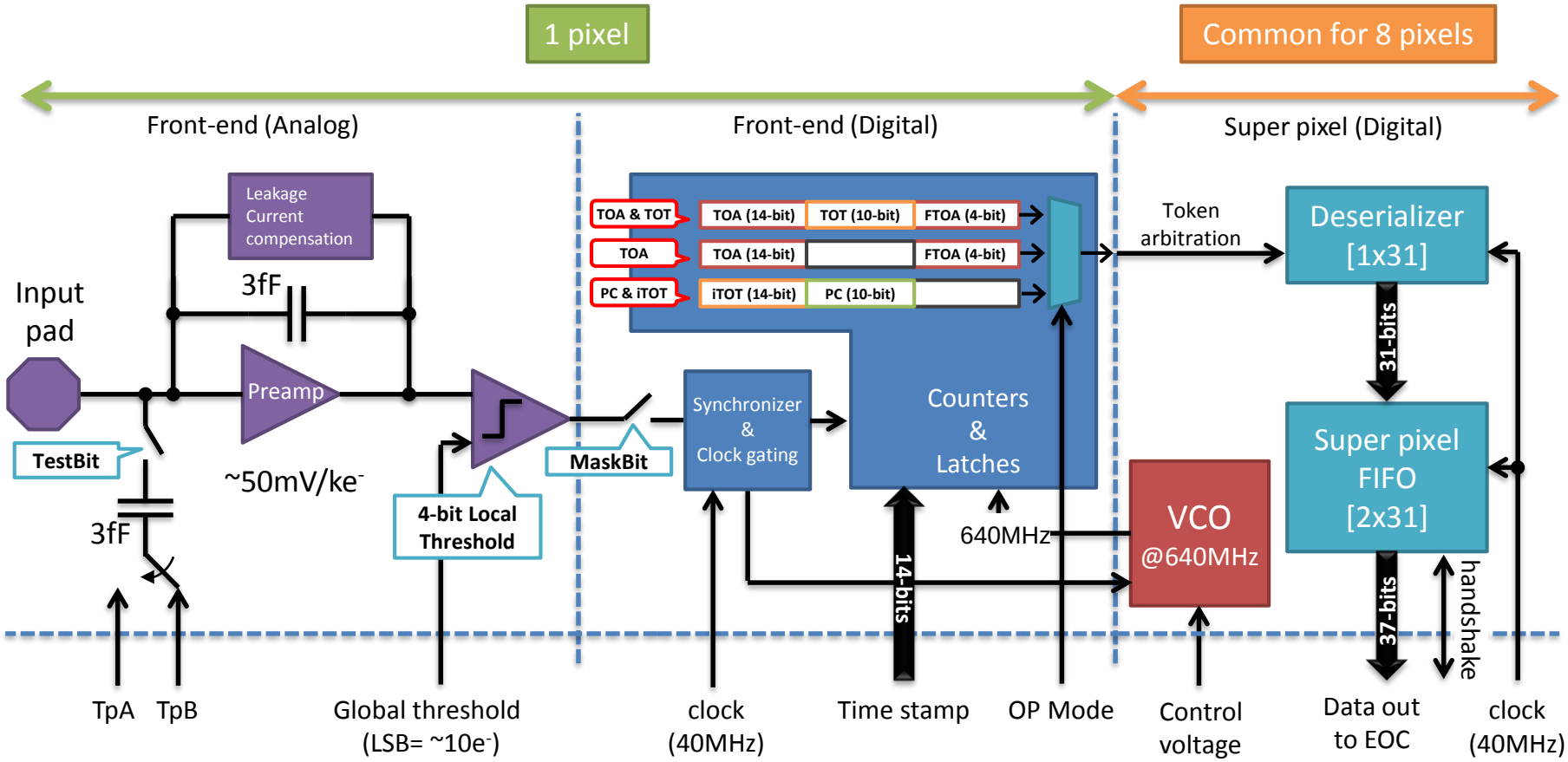
- Experience gained in the design of the Medipix3 chip (2009):
  - Technology (130nm CMOS)
  - Building blocks recycled (CERN's HD Standard Cell library, DACs, …)

- Designed by CERN, Nikhef and Bonn University with the support of the Medipix3 Collaboration

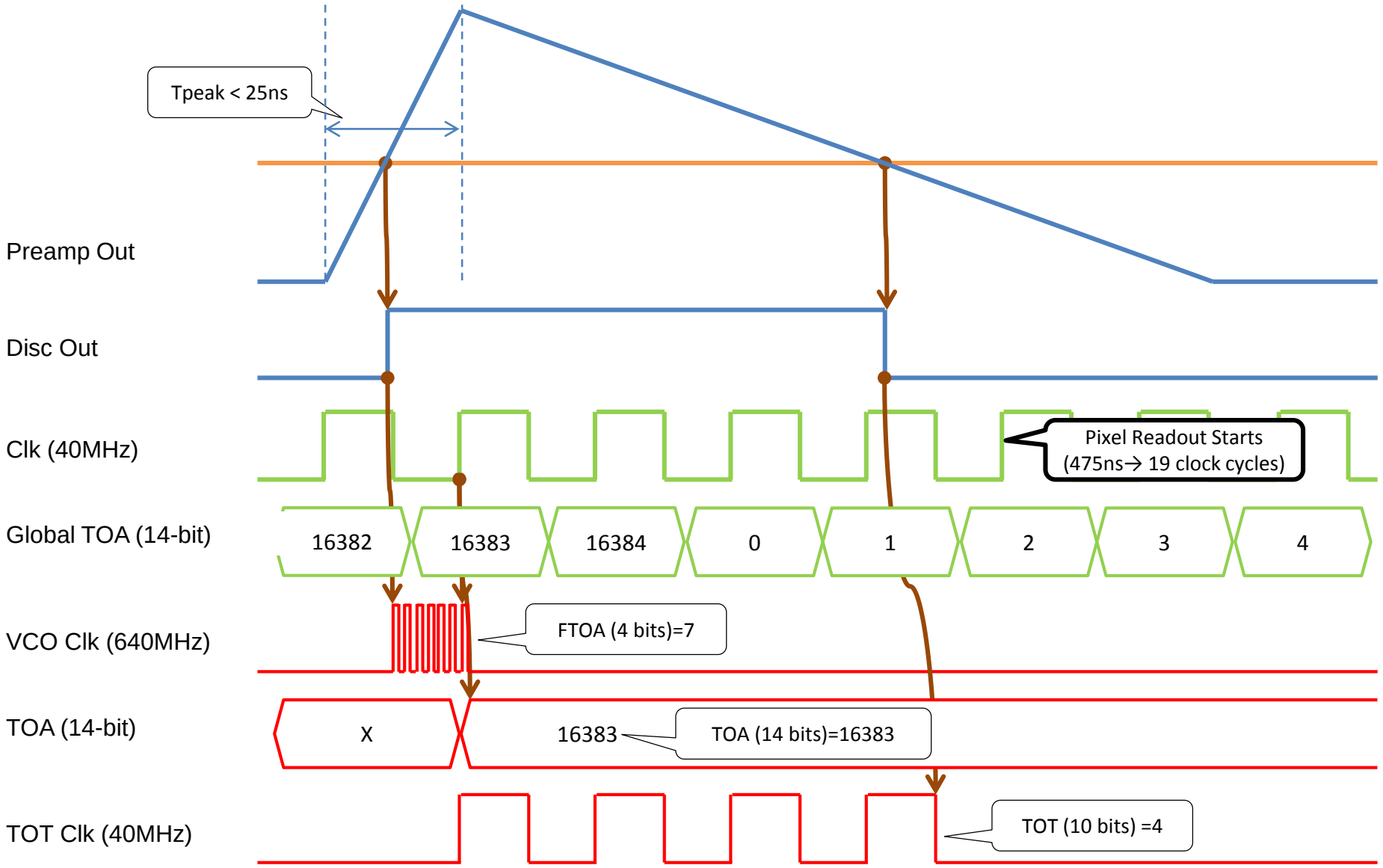
Timepix → Timepix3

	Timepix (2006)	Timepix3 (2013)
Pixel arrangement	256 x 256	
Pixel size	55 x 55 µm²	
Technology	250nm CMOS	130nm CMOS
Acquisition modes	1) Charge (TOT) 2) Time (TOA) 3) Event counting (PC)	1) Time (TOA) AND Charge (TOT) 2) Time (TOA) 3) Event counting (PC) AND integral charge (iTOT)
Readout Type	1) Frame based	1) Data driven (DD) → < 40 Mhits/s/cm² 2) Frame based (FB)
Zero suppressed readout	NO	YES
Dead time per pixel	> 300µs readout time of one frame	> 475ns Pulse measurement time + packet transfer time **~600x**
Minimum timing resolution	10ns	1.562ns **6.4x**
On-chip Power pulsing (PP)	NO	YES **Programmable turn ON/OFF time**
Minimum detectable charge	~750e-	>500e- **1.5x**
Technology	IBM 250 nm CMOS	IBM 130 nm CMOS

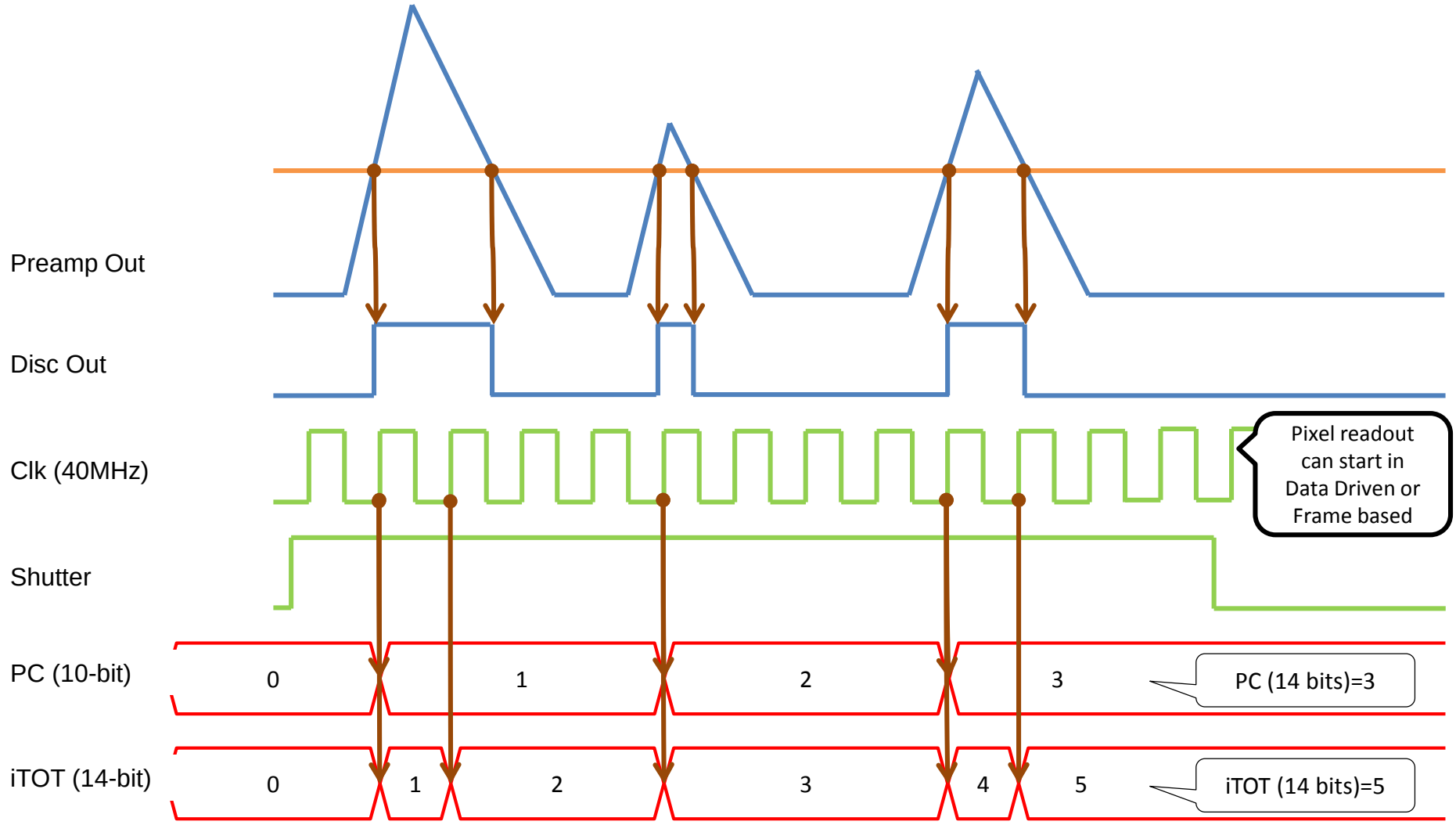
Timepix3 Pixel Schematic



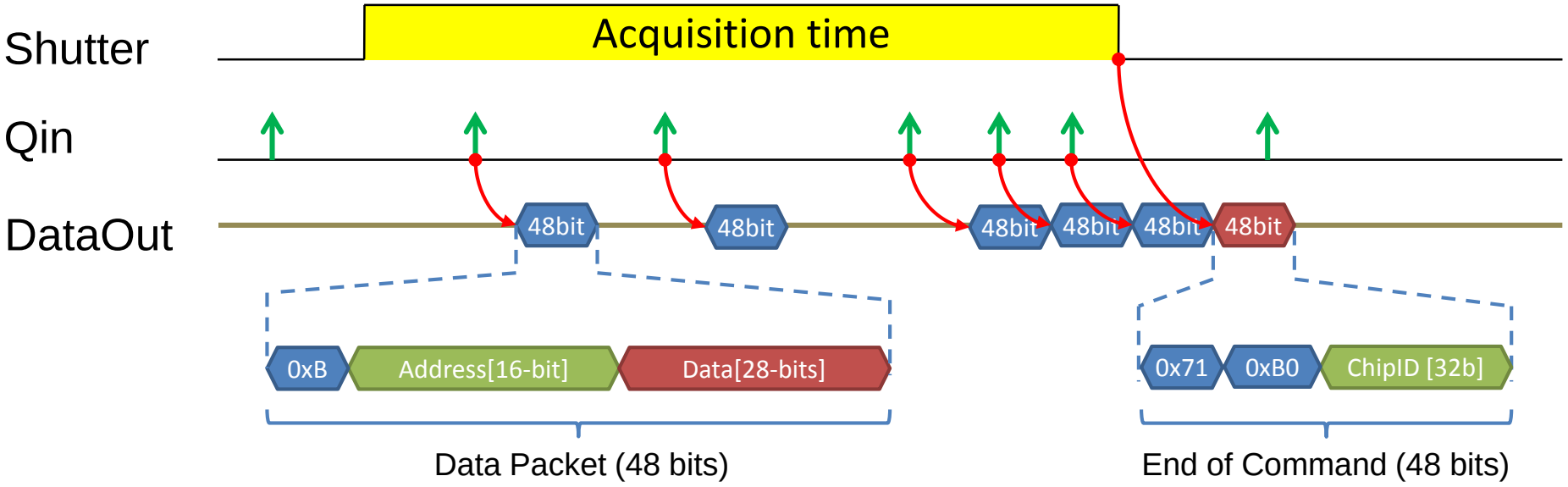
Pixel Operation in TOA & TOT [DD]



Pixel Operation in PC and iTOT [FB]

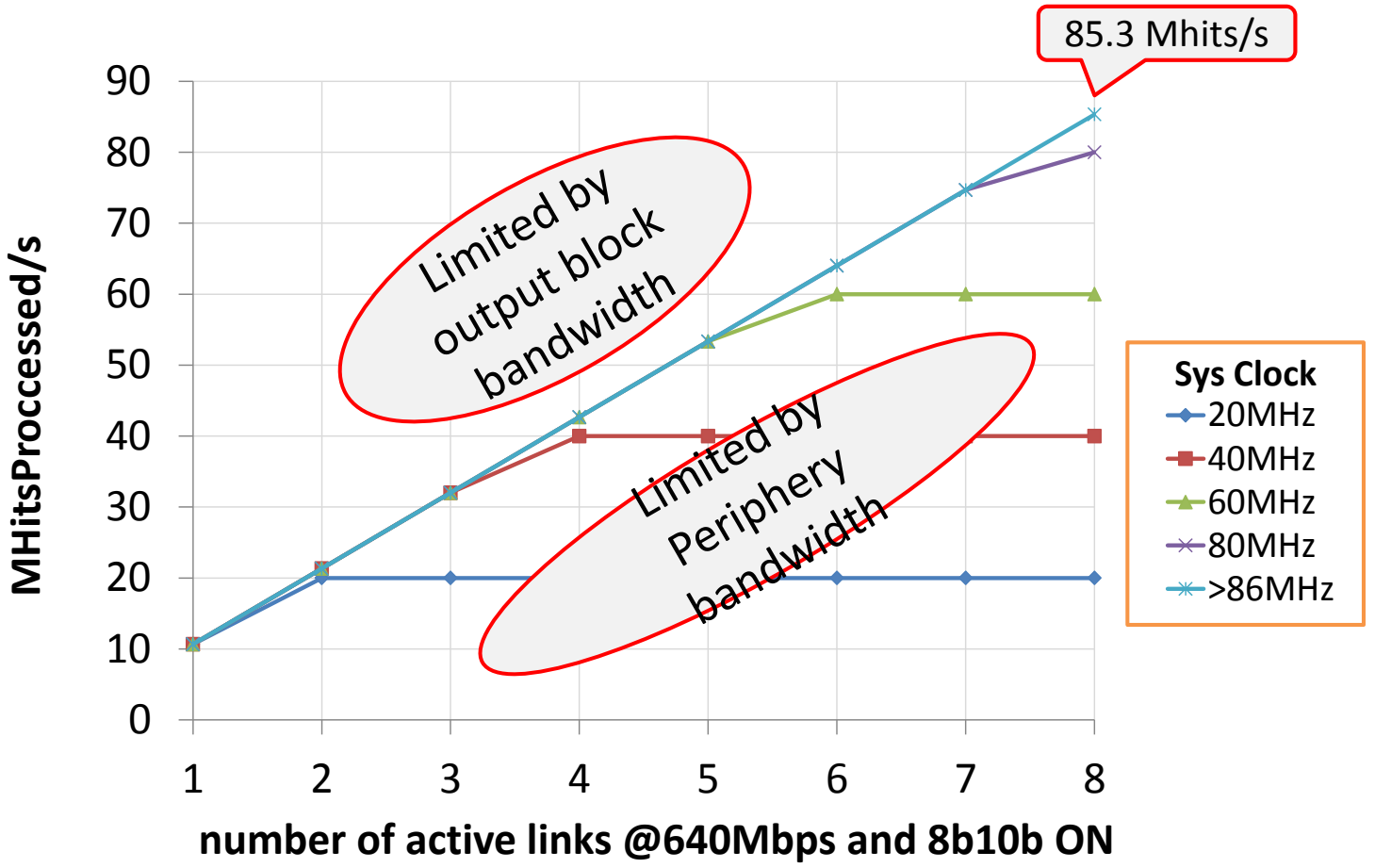


Trigger-less event-by-event data driven and zero-supressed readout



- Achievable count rate:
  - uniformly distributed events → ~40 Mhits/s/cm^2 @5.12Gbps
- Full matrix readout: ~800 µs @5.12Gbps

Maximum Event Readout
Data Driven Readout



Timepix3 (2013)

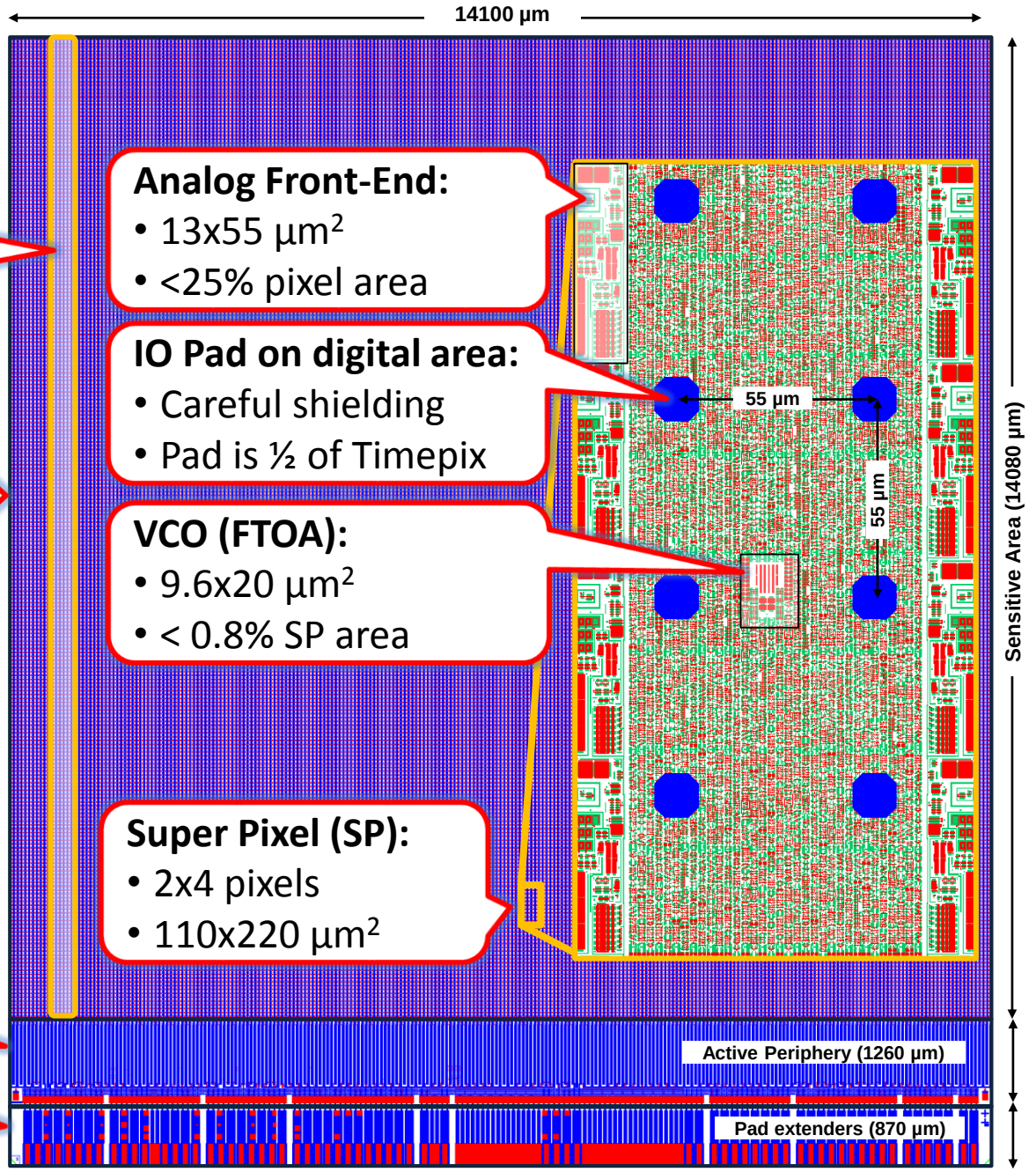
Double column:
2x256pixels
64 super pixels

Full Pixel Matrix:
256x256 pixels
128 double columns

8192 VCOs
(640MHz)
177 Mtransistors

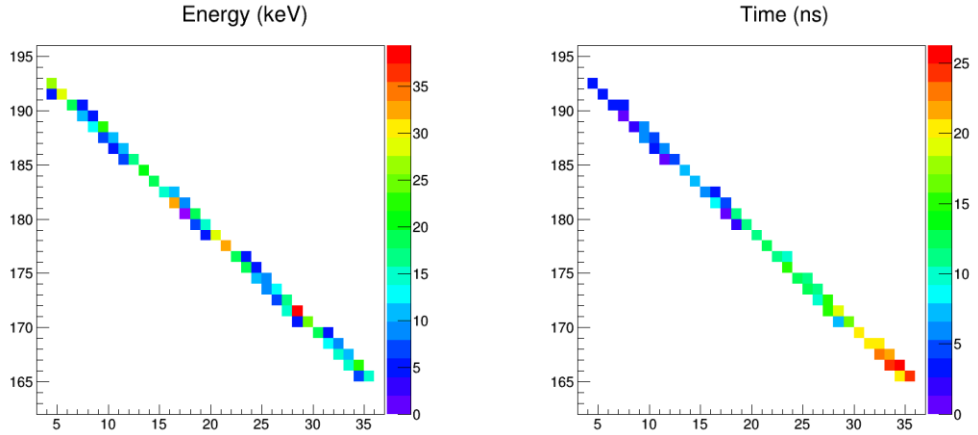
Active Periphery

Pad Extenders:
Removed if TSV

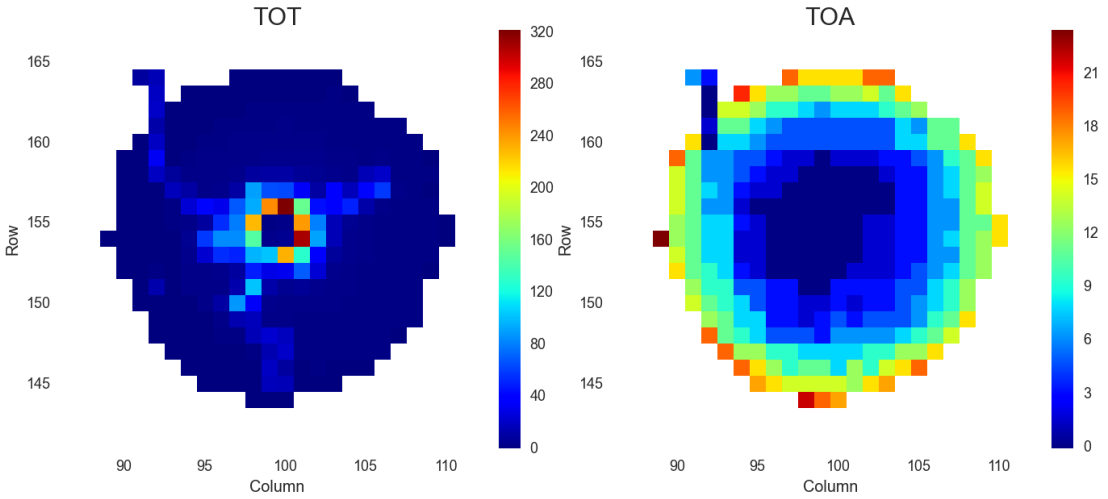


Particle detection using Timepix3

Cosmic ray



Ar 150 GeV/c
[p-on-n 500 µm sensor]



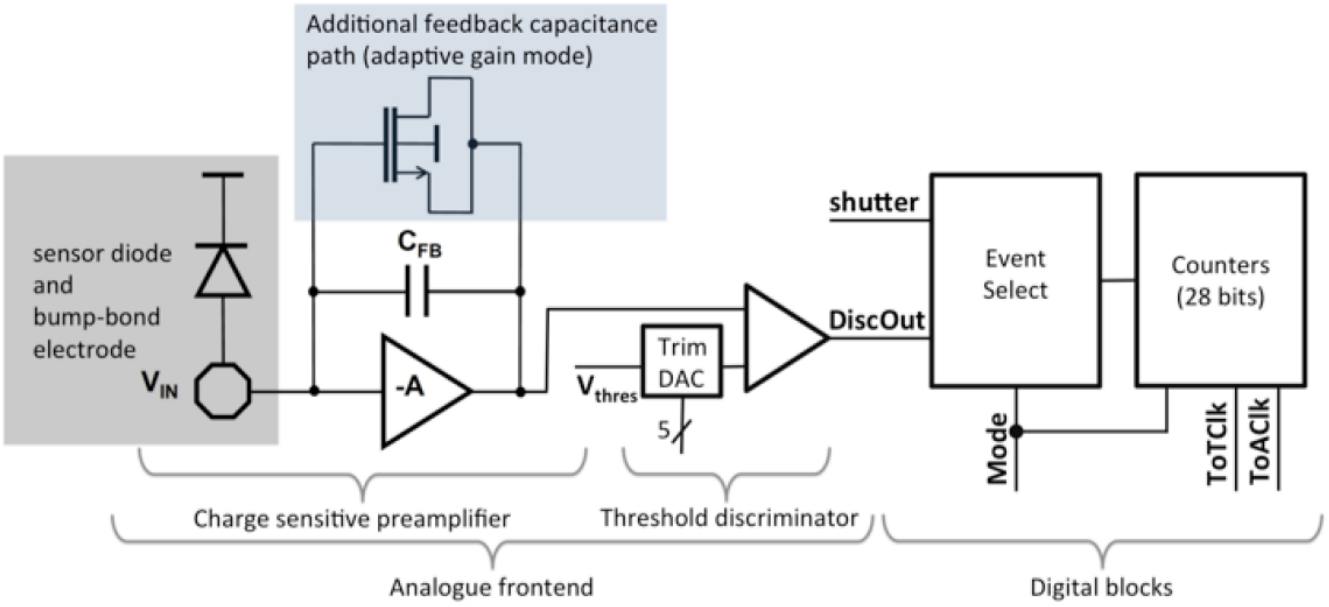
Precise arrival time information (1.56ns steps) provides depth of interaction within the sensor layer

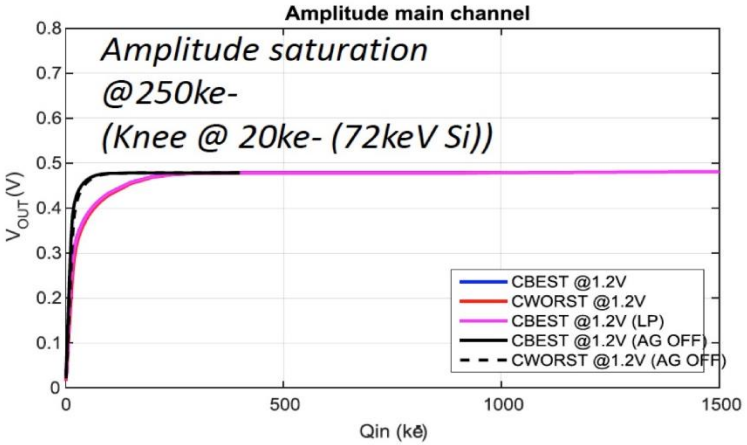
From Timepix and Timepix3→ Timepix2

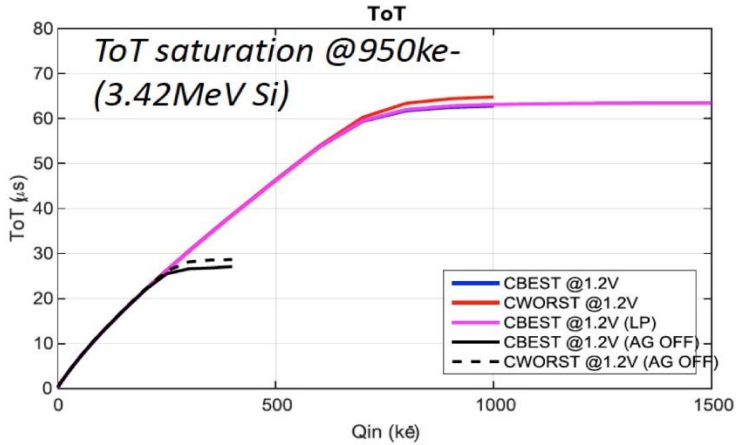
		Timepix2 (2018)
Technology		130nm - 8metal
Pixel size		55 x 55 µm²
Pixel arrangement		256 x 256
Sensitive area		1.98 cm^2
Front End	**e^- collection**	Leakage current compensation optimal (I_{DET}>I_{KRUM}) Non-monotonicity of the ToT vs Qin
	h^+ collection	Leakage current limited (I_{DET}<I_{KRUM}/2) Logarithmic gain mode
Pixel Readout	**Single Frame**	TOT 10bits and TOA 18bits 1st hit TOT 14 bits and TOA 14bits
	CRW	2x TOT 10bits and PC 4bits 2x TOT 14bits 2x TOA 10bits or 14bits 2x PC 10 or 14 bits
Readout Type		1 serial link < 100 Mbps 32 bit parallel < 3.2 Gbps
Timing resolution/range		> 10ns / 2.620 ms @ 100MHz

Medipix2 collaboration funded project

Timepix2 pixel schematic

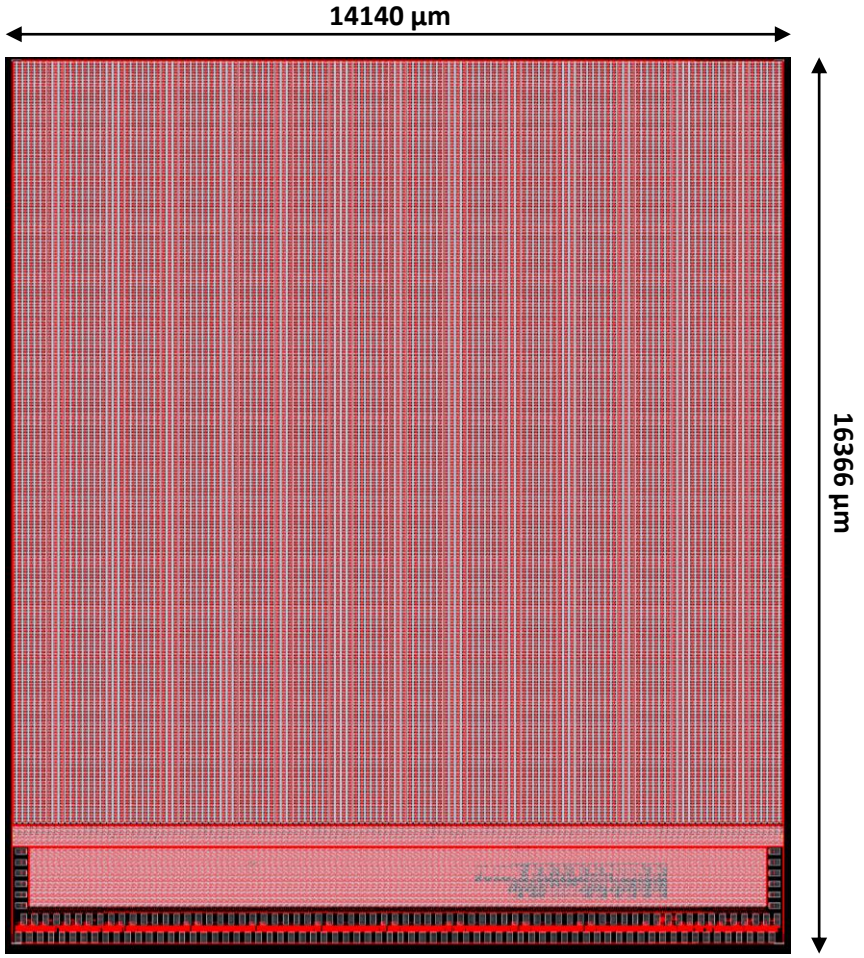






Timepix2 (2018)

- Simultaneous ToT and ToA
- Separate ToT and ToA clock
- Readout dead-time-free modes
- Fast clear
- Digital and analogue test pulses
- Digital and analogue pixel masking
  - ROI
  - coarse pitch bump bonding
- Adaptive frontend gain
- Reduced threshold dispersion
- Digital diagnostics modes
- Test points in analogue frontend
- Matrix occupancy monitor
- Digital-only pixels with wirebond input
- Serial port (full frame)
- 32b Parallel port (full frame)
- Serial port (zero column suppression)
- Serial communication with daisy-chaining (as in Medipix2/Timepix)
- IO compatible with TSVs



Medipix4 Collaboration (from 2016)

15 members

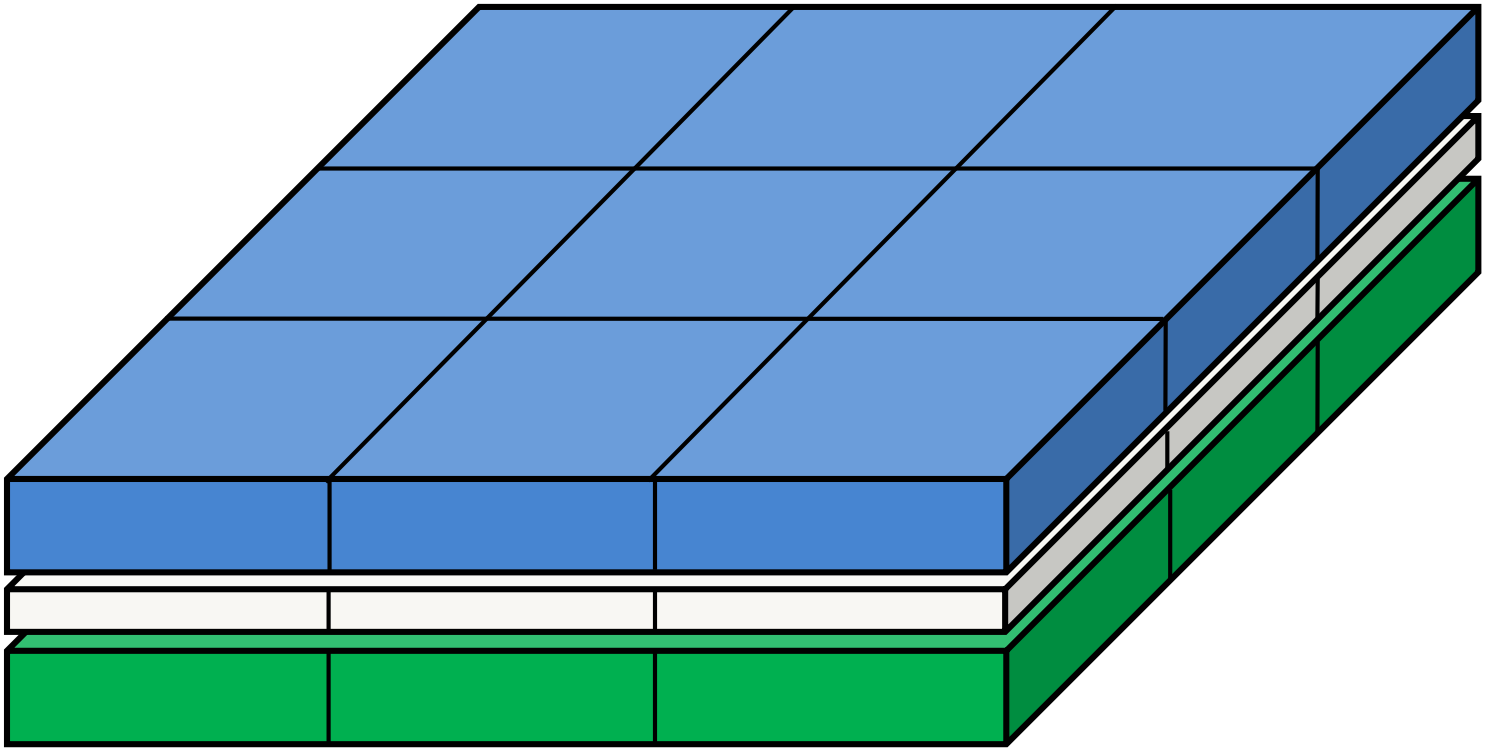
- CEA, Paris, France
- CERN, Geneva, Switzerland,
- DESY-Hamburg, Germany
- Diamond Light Source, Oxfordshire, England, UK
- IEAP, Czech Technical University, Prague, Czech Republic
- JINR, Dubna, Russian Federation
- NIKHEF, Amsterdam, The Netherlands
- University of California, Berkeley, USA
- University of Houston, USA
- University of Maastricht, The Netherlands
- University of Canterbury, New Zealand
- University of Oxford, England, UK
- University of Geneva, Switzerland
- IFAE, Barcelona, Spain
- University of Glasgow, UK

Timepix3 → Timepix4

Timepix4: A 4-side tillable large single threshold particle detector chip with improved energy and time resolution and with high-rate imaging

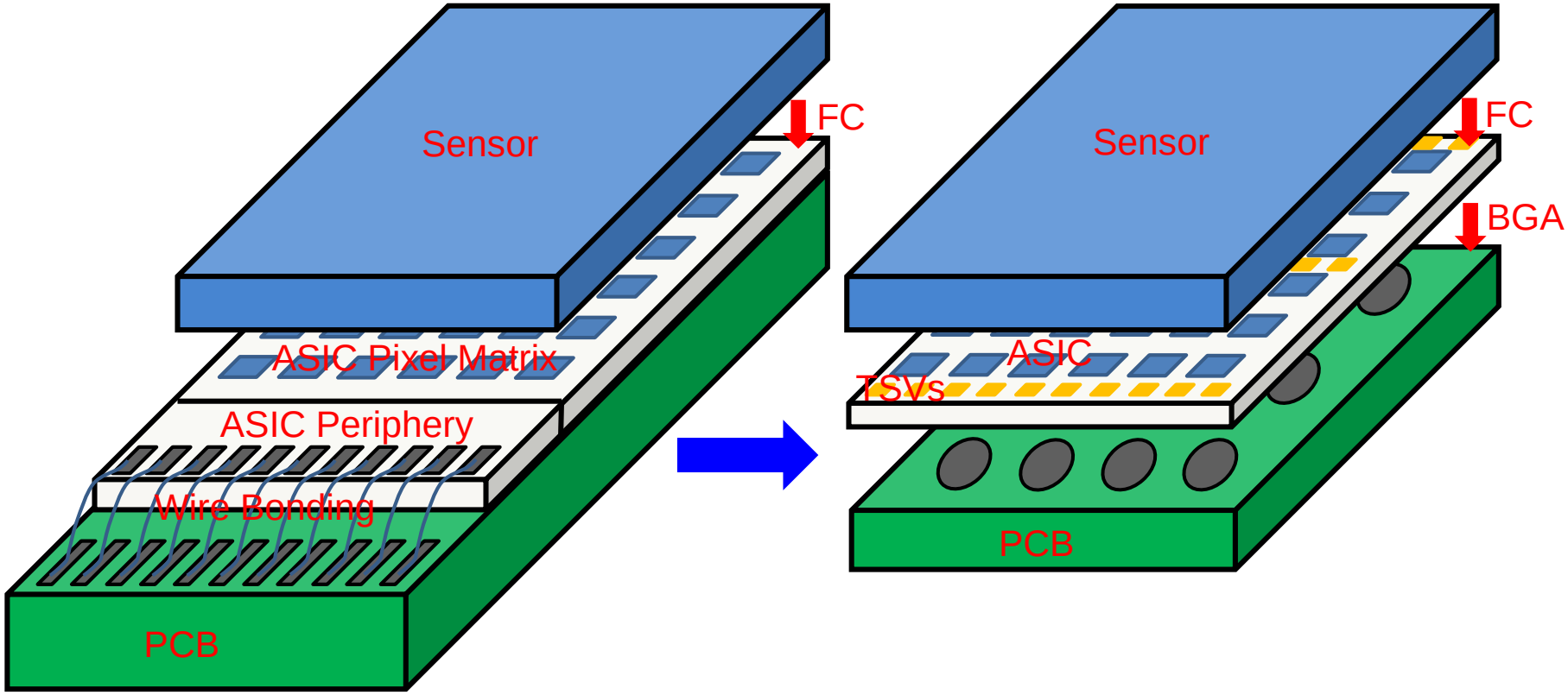
			Timepix3 (2013)	Timepix4 (2019)	
Technology			130nm – 8 metal	65nm – 10 metal	
Pixel Size			55 x 55 µm	55 x 55 µm	
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448	**3.5x**
Sensitive area			1.98 cm^2	6.94 cm^2	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA		
		Event Packet	48-bit	64-bit	**33%**
		Max rate	0.43x10^6 hits/mm^2/s	**3.58x10^6 hits/mm^2/s**	**8x**
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**	
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)	
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)	**10x**
		Max count rate	~0.82 x 10^9 hits/mm^2/s	~5 x 10^9 hits/mm^2/s	**5x**
TOT energy resolution			< 2KeV	< **1Kev**	**8x**
Time resolution			1.56ns	**~200ps**	
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	**≤163.84 Gbps (16x @10.24 Gbps)**	
Target global minimum threshold			<500 e^-	<500 e^-	

4-side buttable: Motivation



- Build **large area detectors** by combining smaller modules

4-side buttable: Challenge



- The through-silicon vias (TSVs) are the key technology for this paradigm shift

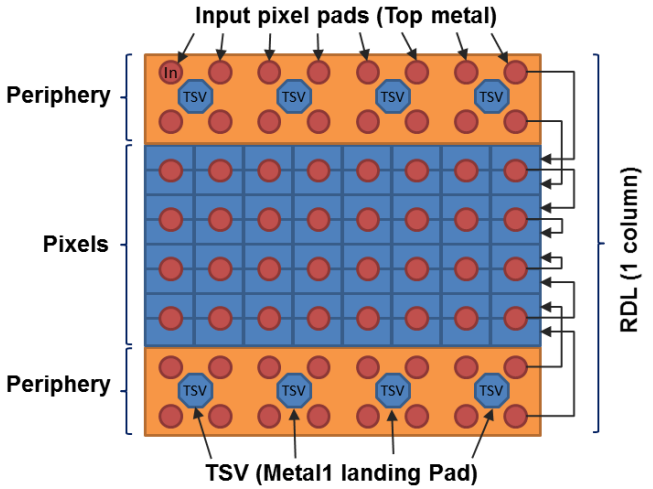
A large 4-side buttable detector

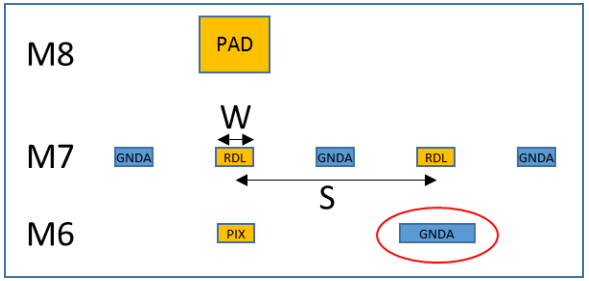
- **Advantages:**
  - Build large area detectors without dead area
  - Better power distribution on chip (TSV) → Larger single ASICs
  - Mechanically more robust (no wire-bonds)

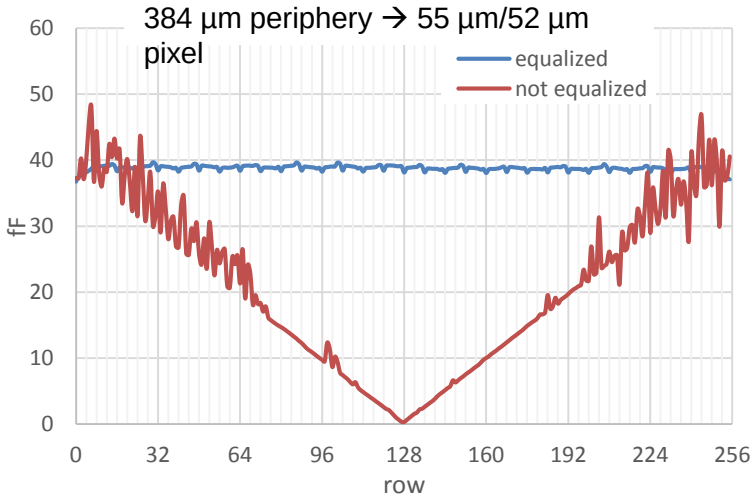
- **Disadvantages:**
  - Periphery hidden or integrated in the pixels → RDL between sensor and pixel input
    - RDL → Increase input capacitance and crosstalk (~30-50fF)
  - Top metal layers "blocked" → No MiMCaps, Inductors…
  - Devices are only available after TSV processing (no wire-bonds)

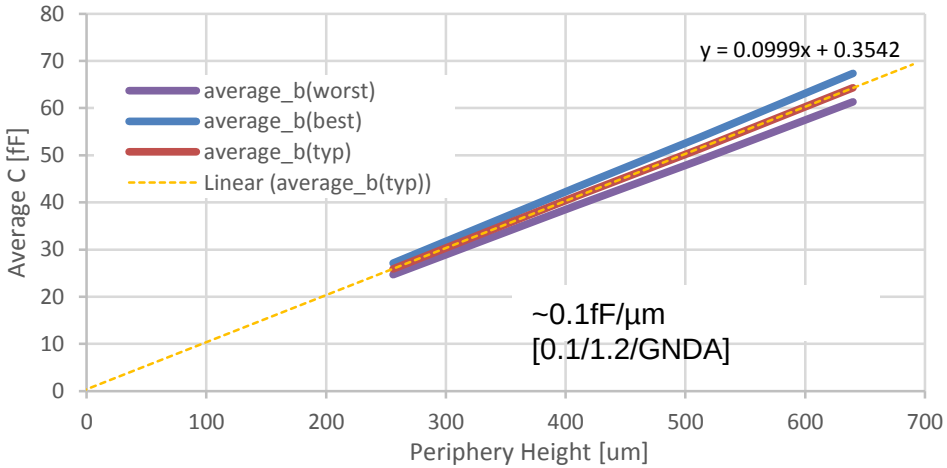
On-chip pad to pixel RDL

- Use of 10 metal option (1p9m + RDL):
  - Equalized Cin for all pixels → ~46 fF increase in Cin for a 460 µm periphery
  - Shielding of RDL layers to minimize/eliminate cross-coupling
- RDL routing over analog pixel circuitry and periphery → M7 used as shield



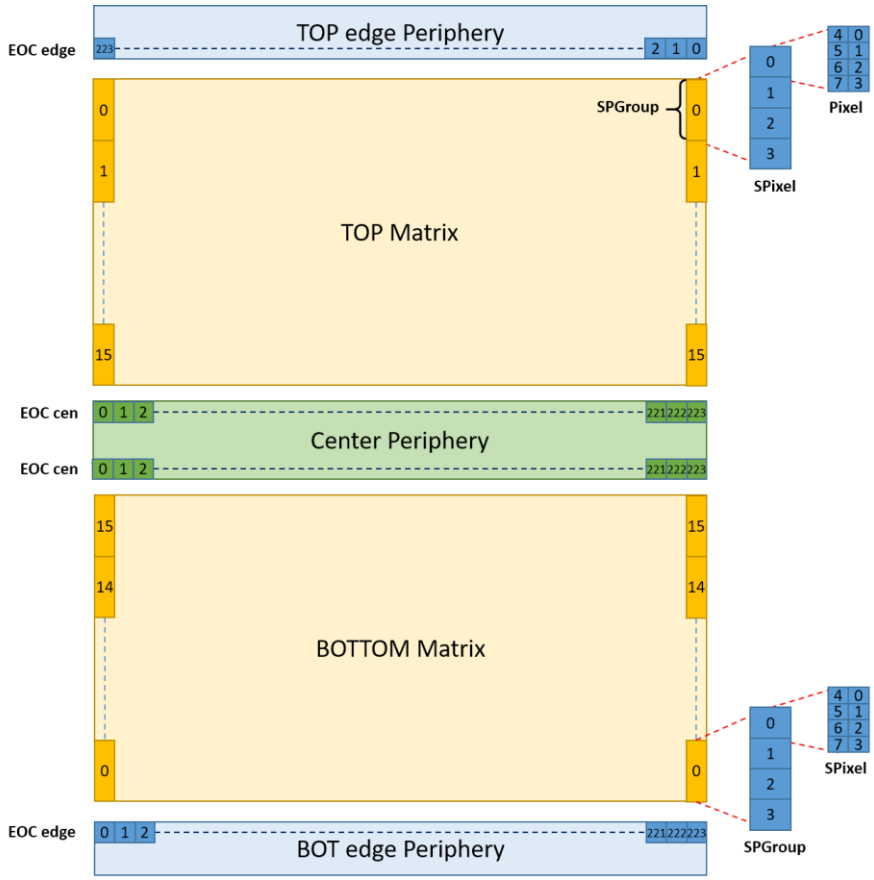






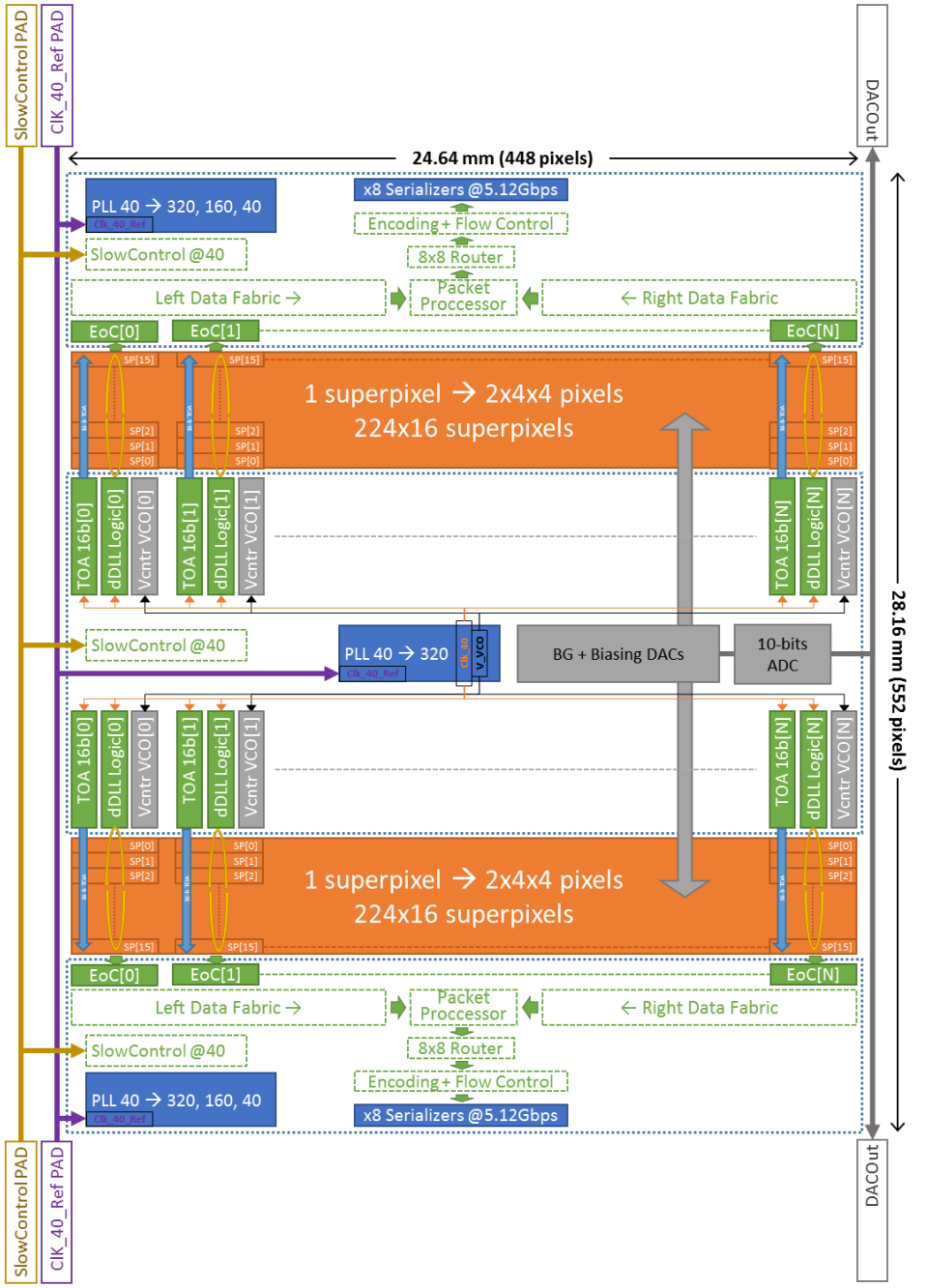
Timepix4 arrangement

- 512 x 448 of 55 x 55 µm pixels
- 3 peripheries with TSV (Through-Silicon-Vias):
  - TOP, BOTTOM: Data Readout (10 Gbps Serializers)
  - CENTRAL: Analog Blocks (DACs, ADC, Band-Gaps…)
- Edge peripheries also with ~1mm Wire Bond Pads:
  - This can be diced-off to achieve a 100% sensitive area (4-side buttable)
- Interface to DAQ:
  - Through 3xTSVs
  - Through 2xWB
    - 1xWB possible for low power applications
- Control architecture allows to operated Timepix4 from any of the 3 peripheries:
  - i2C protocol
  - Custom Slow Control protocol
- Fast readout requires at least 1 serial link enabled in each edge periphery

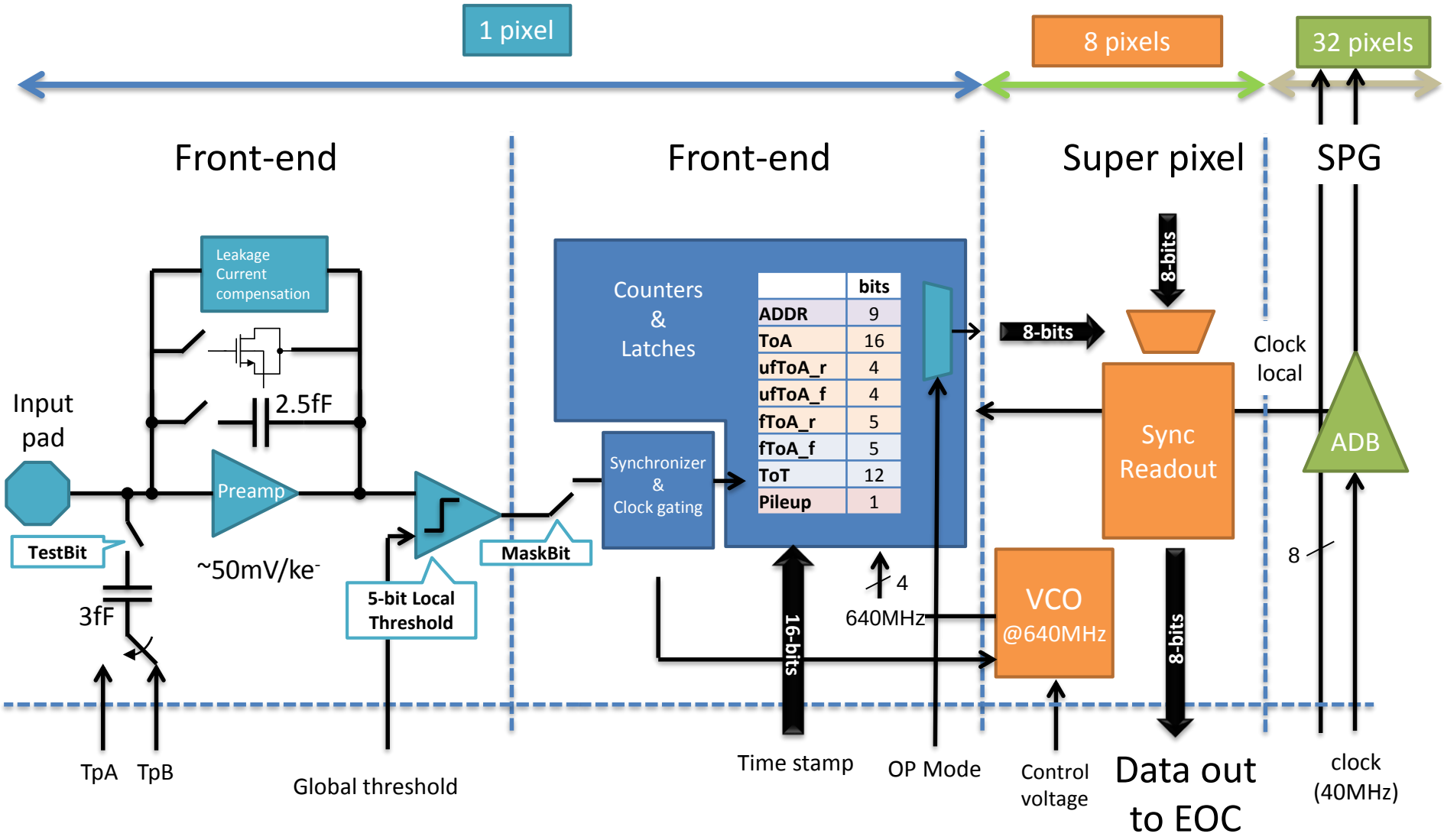


Timepix4 Floorplan

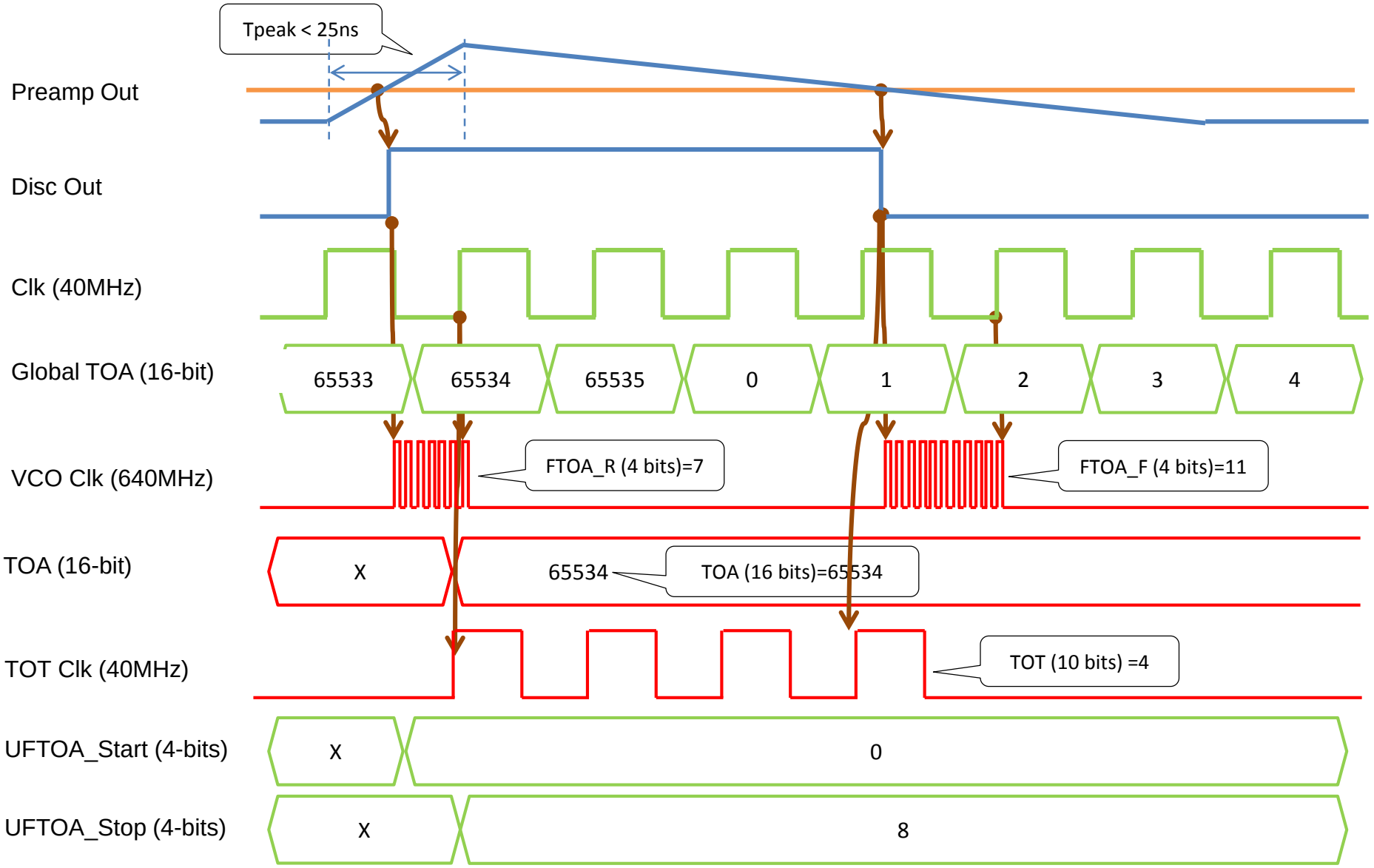
- Chip size 28.16mm x 24.64 mm (no Wirebonds)
- 512 x 448 → 229376 pixels
- Pixel size 55µm x 55µm
- Analog Periphery (920 µm):
  - BandGap + Temperature sensor
  - Biasing DACs
  - Monitoring ADC
  - PLL for time reference
  - Analog supply
  - Digital supply
- 2 x Digital Periphery (460 µm):
  - 8 x 10.28 Gbps serializers (configurable)
  - PLL(s)
  - Analog supply
  - Digital supply
- 2 x Pixel matrix (13.28 mm x 24.64mm):
  - 256 x 448 pixels 55 µm x 51.4 µm
  - 5.68% smaller than 55 µm x 55 µm
  - RDL to compensate up to 460.8 µm



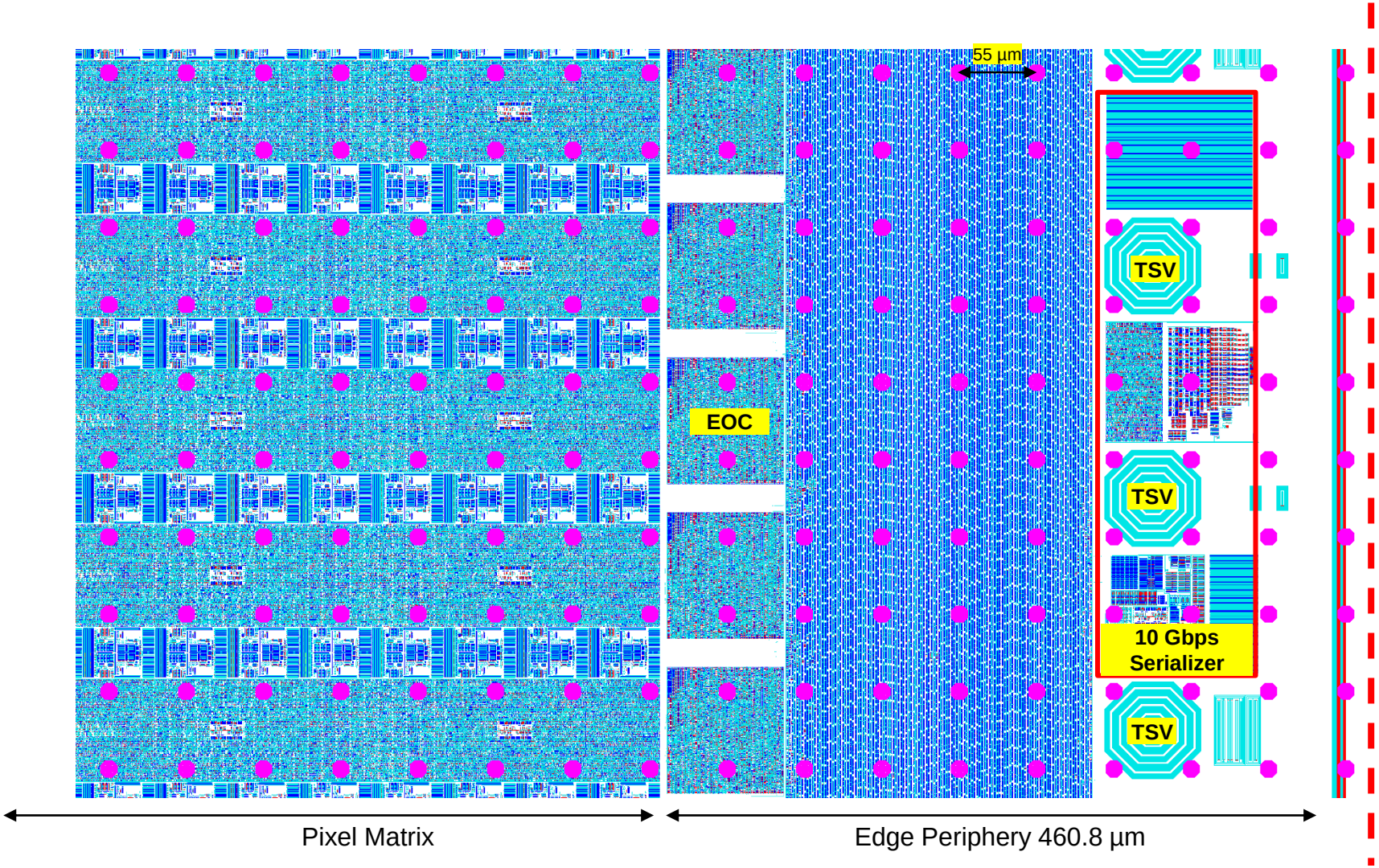
Timepix4 Pixel Schematic



Pixel Operation in TOA & TOT [DD]

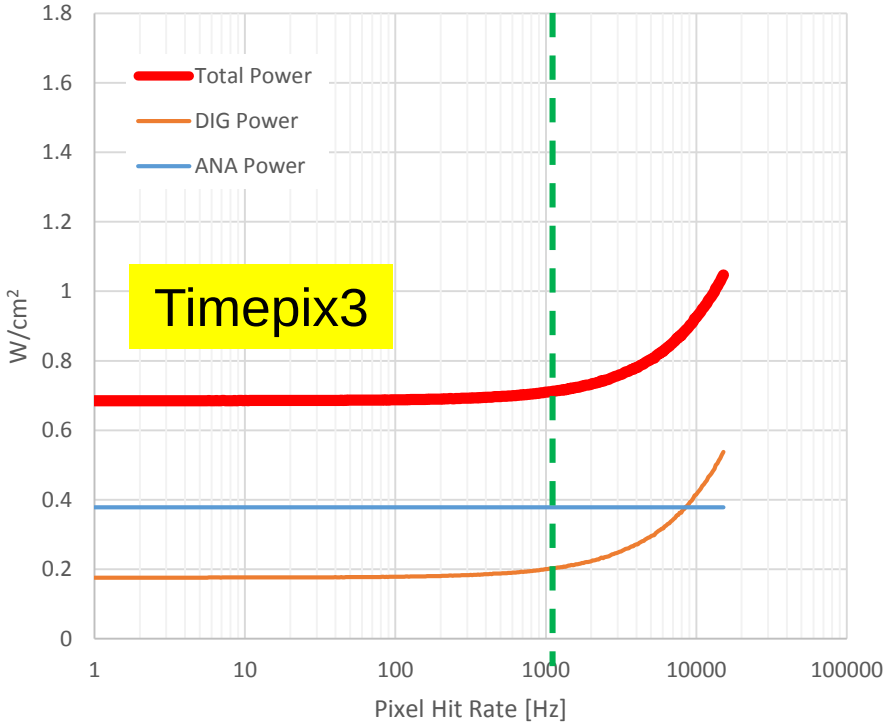


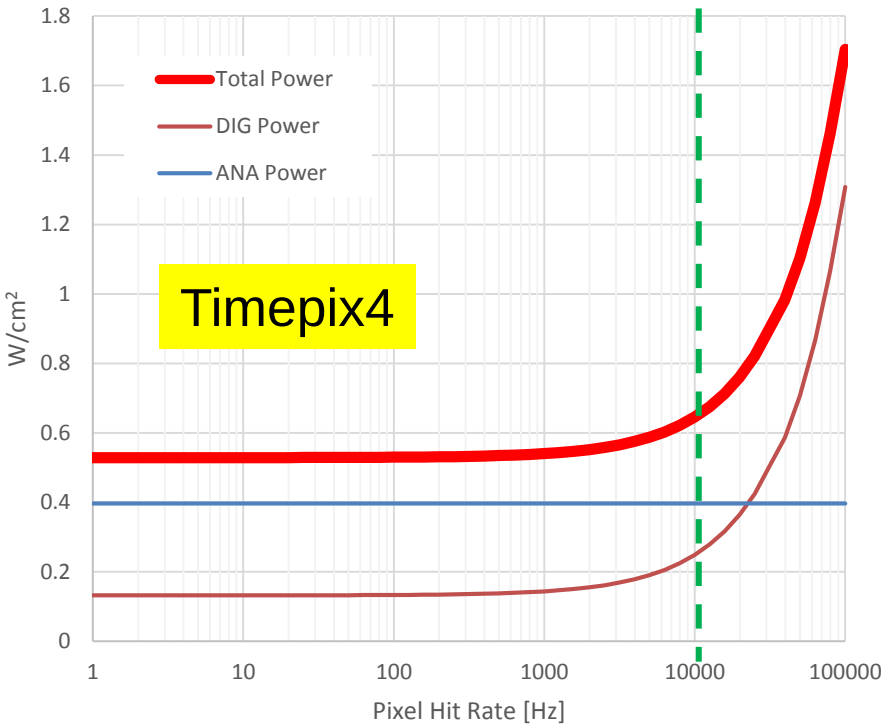
Edge Periphery



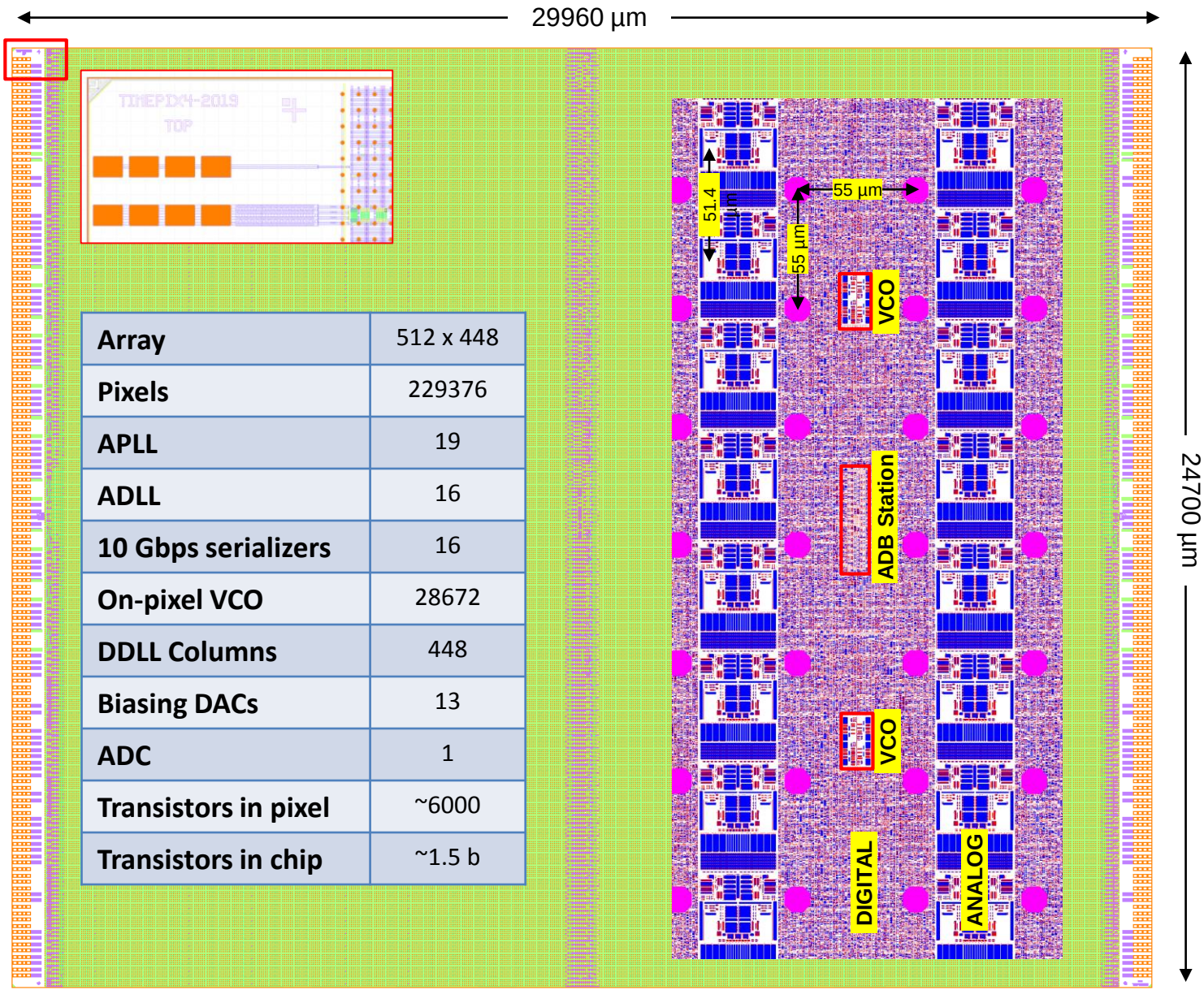
Digital (dynamic) Power Consumption [data-driven]

- Expected power consumption density to be ~20 % less of Timepix3:
  - Digital power consumption 25% less
    - Improved clock distribution (DDLL)
    - 130nm → 65nm
  - Analog consumption is ~5% more
    - Minimize jitter → < 50ps
    - Compensate increase in input capacitance





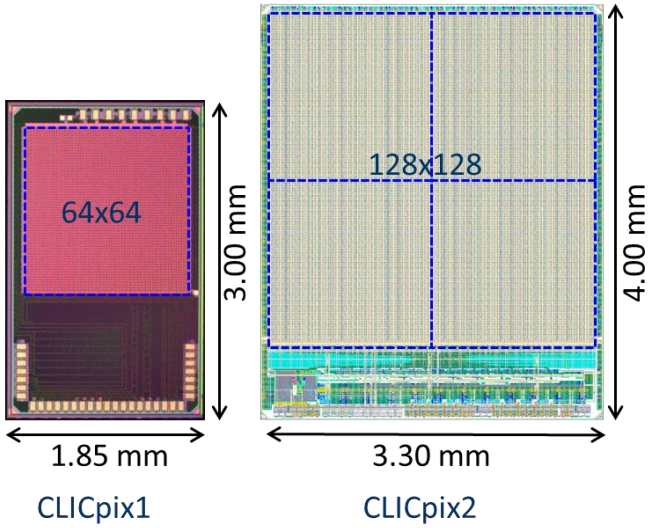
Timepix4 (2019)



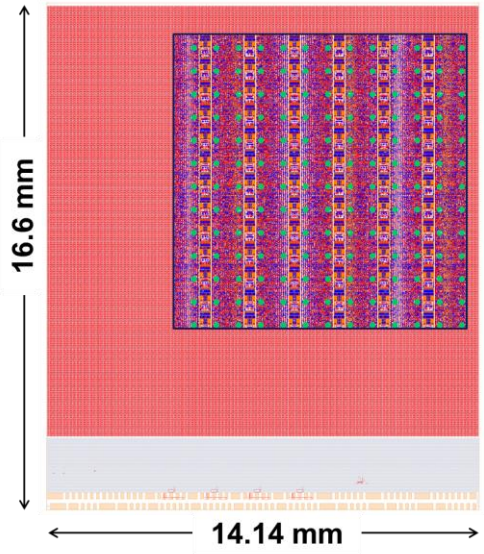
Array	512 x 448
Pixels	229376
APLL	19
ADLL	16
10 Gbps serializers	16
On-pixel VCO	28672
DDLL Columns	448
Biasing DACs	13
ADC	1
Transistors in pixel	~6000
Transistors in chip	~1.5 b

Timepix babies in HEP

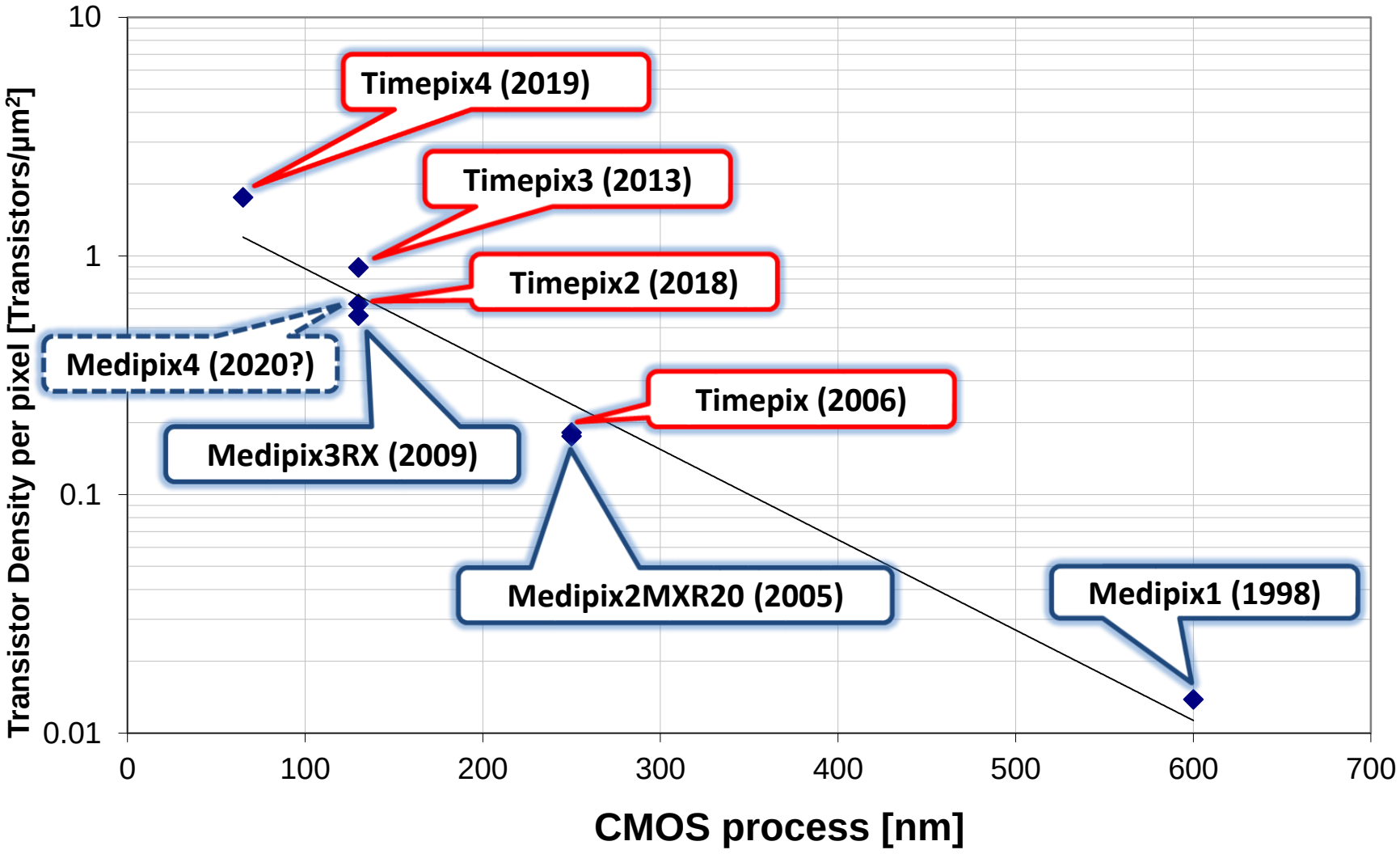
- CLICpix1 (2013) and CLICpix2 (2016):
  - 65nm technology
  - 25 µm pixel
  - TOA and TOT



- Velopix (2016):
  - Triger-less upgrade from LHCb VELO
  - 130nm technology
  - 256x256 55 µm pixels
  - Binary information
  - 20 Gbps data bandwitdth
  - 800 Mhits/s/ASIC



Medipix Family of ASICs developed @CERN



Conclusions

The Timepix family of chips has stimulated innovation for particle tracking over the last 13 years:

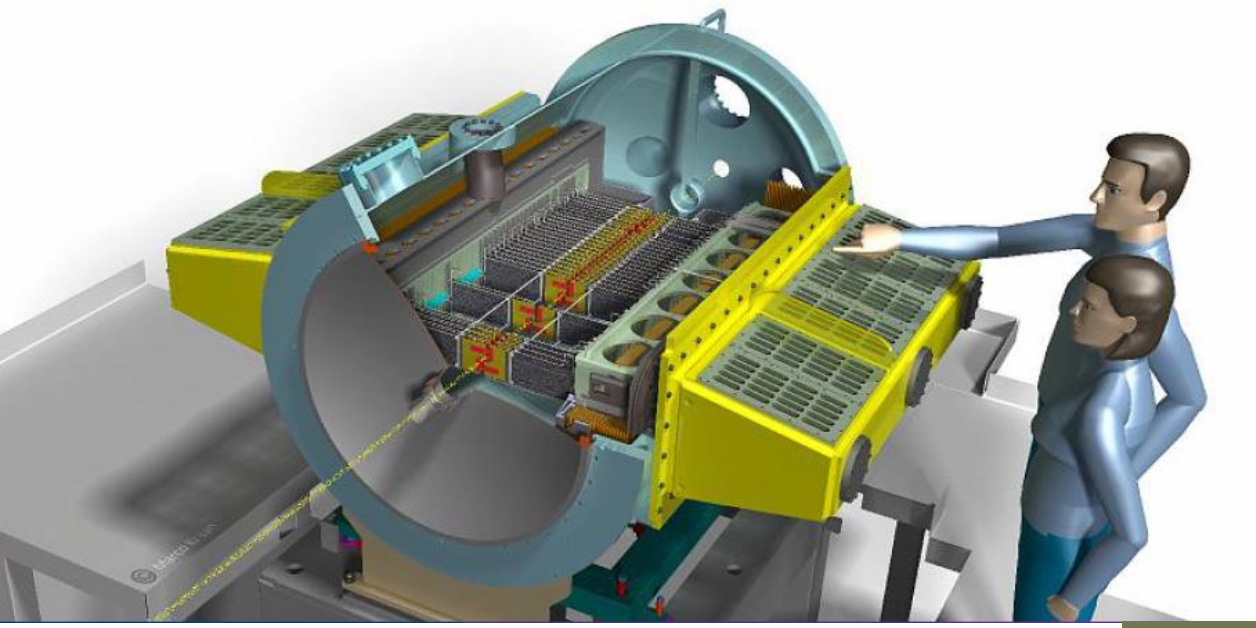
- Timepix (2006) measure time or charge in a portable/low power highly pixelated detector
- Timepix3 (2013) allowed us to measure event-by-event simultaneously time and charge with a time resolution of 1.5 ns
- Timepix2 (2018) extended the energy dynamic range measurement with a highly configurable pixel and readout architecture
- Timepix4 (2019) will give us a 4-side buttable chip with 229K pixels each on able to measure 200 ps arrival time resolution in a x4 larger sensitive area

Thank you !

Medipix Collaboration meeting in Prague 2008

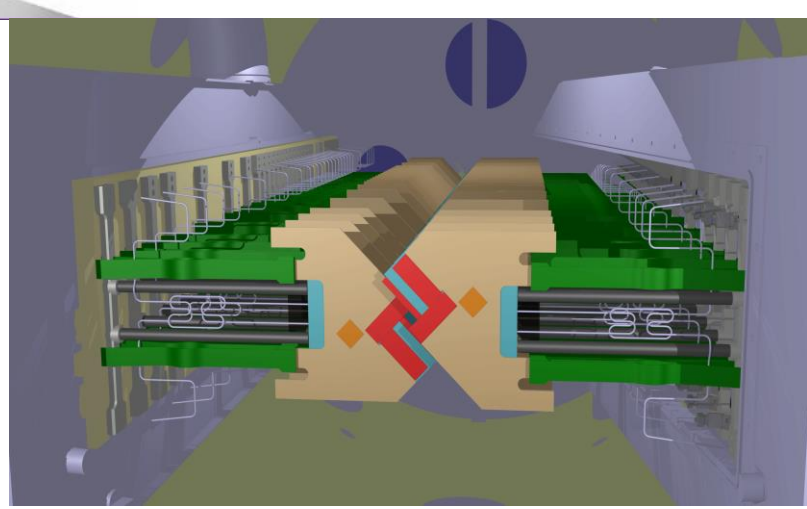
SPARE

Vertex Locator Upgrade



LHCb will be upgraded in 2019→2020
→ very tight planning

- Vertex detector surrounding collision region
  - In vacuum
  - Close to the beam: 5.1 mm
- From silicon strips to pixels
- New R/O chip VeloPix, derived from Timepix3
- In total 624 ASICs, ~41 Mpixels
- Trigger-less readout (~2.9 Tbits/s)



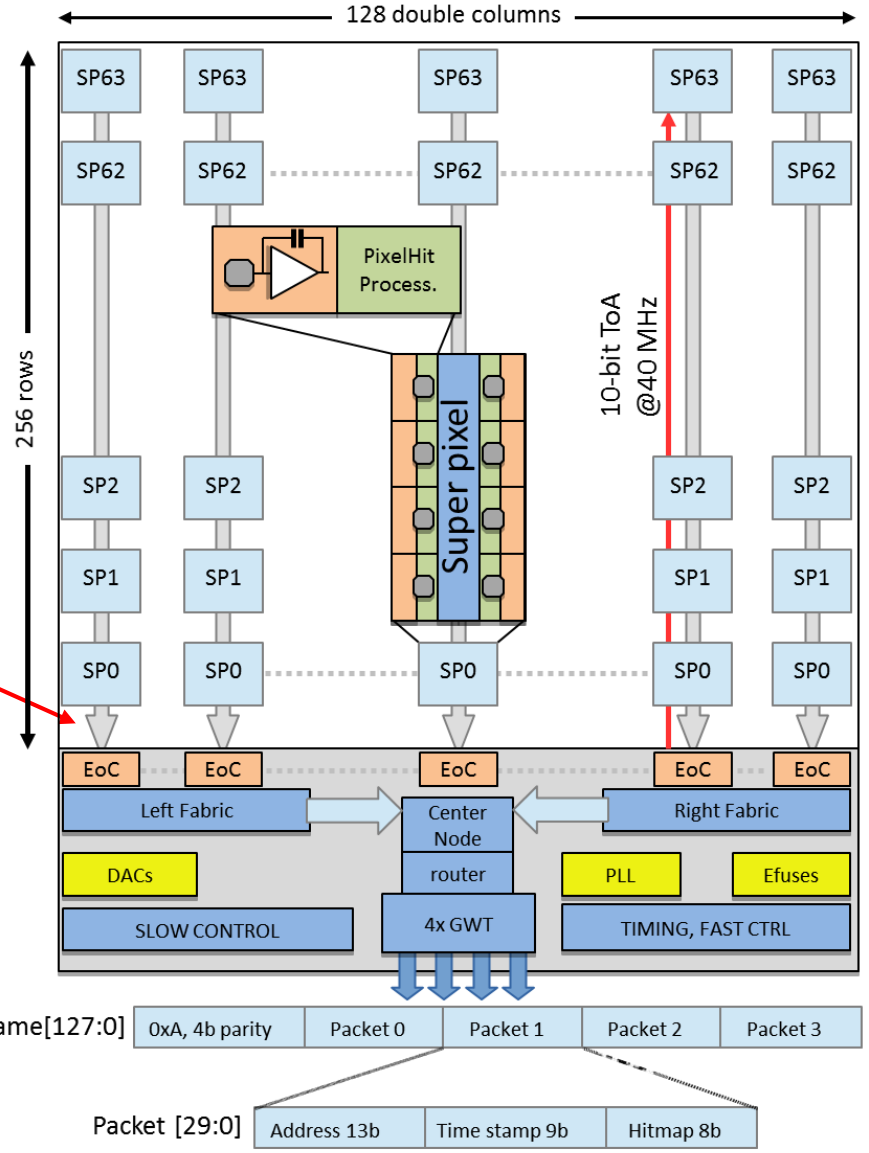
"The VeloPix ASIC test results" E. Lemos (poster)
"The LHCb Vertex Locator Upgrade" E. Lemos (talk)

From Timepix3 → Velopix

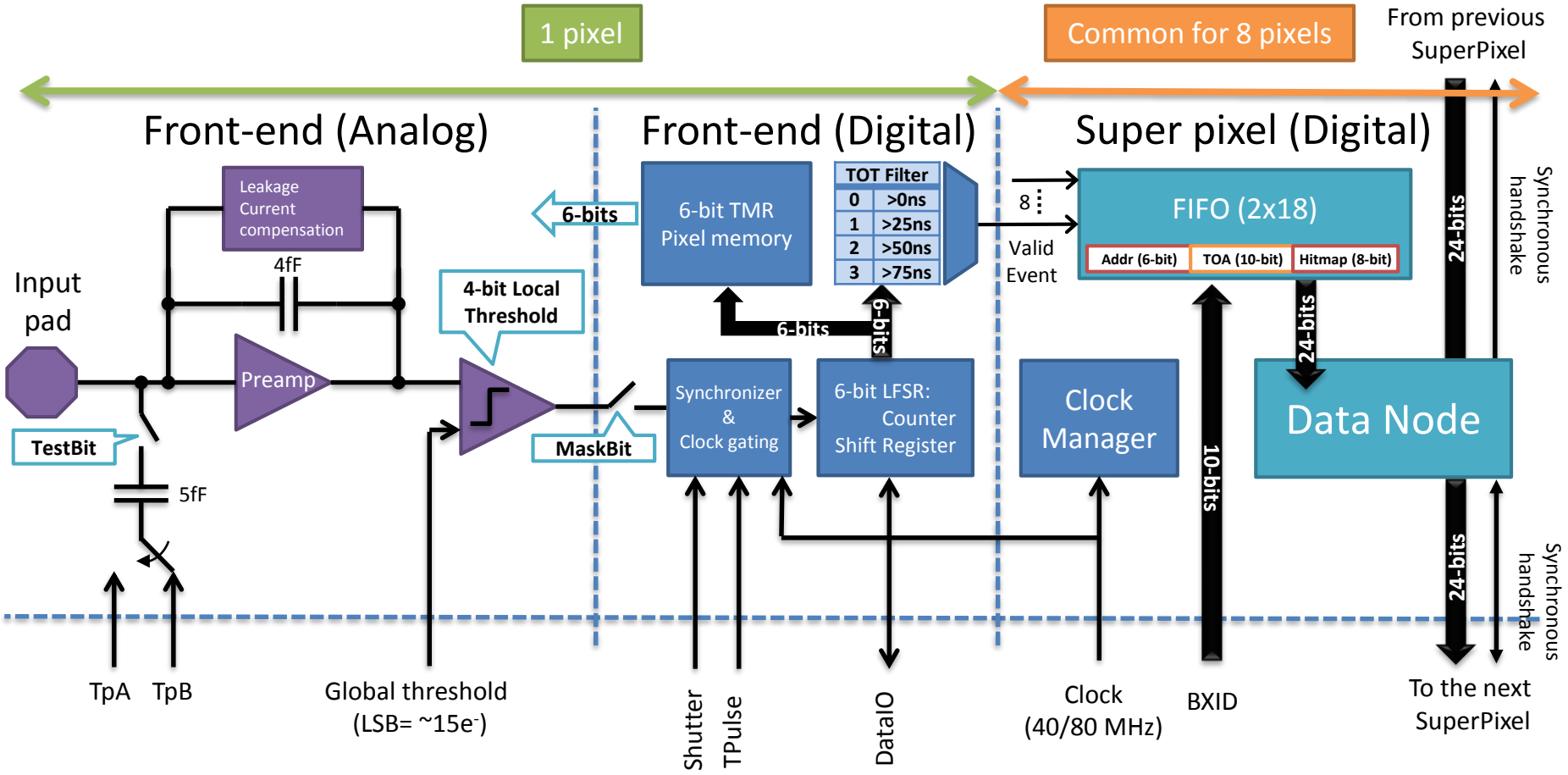
	Timepix3 (2013)	VeloPix (2016)
Pixel arrangement	256 x 256	
Pixel size	55 x 55 µm²	
Peak hit rate	80 Mhits/s/ASIC	800 Mhits/s/ASIC 50 khits/s/pixel **10x**
Readout type	Continuous, trigger-less, TOT	Continuous, trigger-less, binary
Timing resolution/range	1.5625 ns, 18 bits	25 ns, 9 bits
Total Power consumption	<1.5 W	< 3 W
Radiation hardness		400 Mrad, SEU tolerant
Sensor type	Various, e- and h+ collection	Planar silicon, e- collection
Max. data rate	5.12 Gbps	20.48 Gbps **4x**
Technology	IBM 130 nm CMOS	TSMC 130 nm CMOS

VeloPix Chip Architecture

- Pixel matrix:
  - 256 x 256 pixels
  - 128 x 64 super pixels (2x4 pixels each)
  - @40MHz
- Packet-based architecture:
  - 8 pixels/packet + 9 bit time stamp → 30% reduction in data rate
- Data-driven readout:
  - 20 Mpackets/s/double column
- 40, 80, 160 and 320 MHz TMR clock domains in the periphery
- 1 to 4 configurable serializers (GWT)
- Similar to the GBT frame



VeloPix pixel schematic

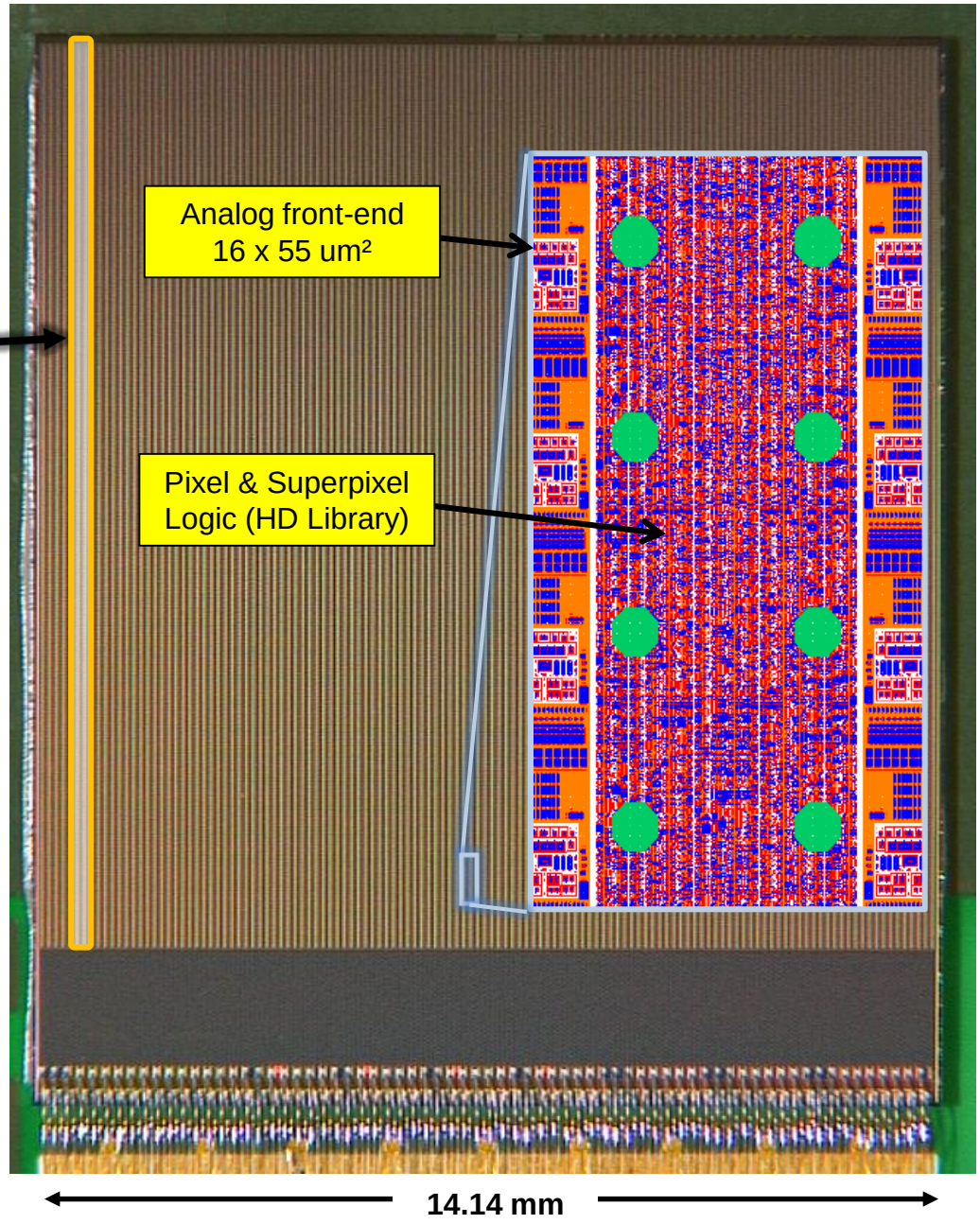


VeloPix (2016)

Double column:
2x256 pixels
64 super pixels

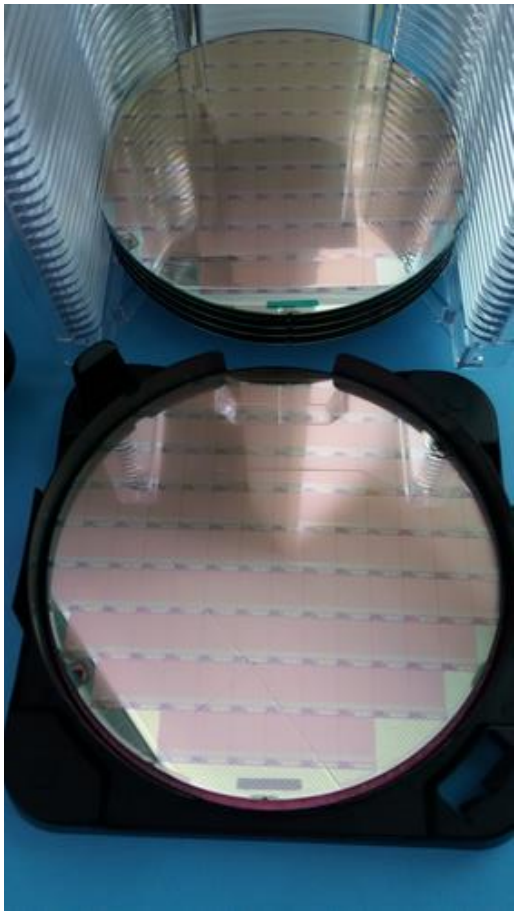
Full matrix:
128 Double columns
~190 Mtransistors

Active Periphery



VeloPix Project Overview

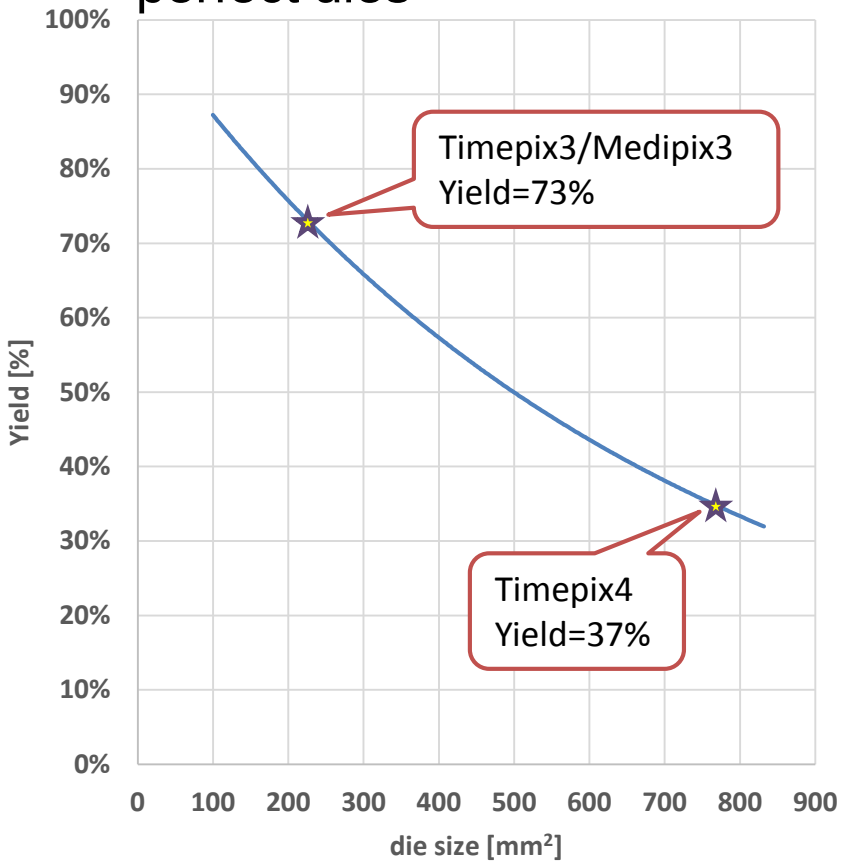
- Design started in June 2013 (after Timepix3 submission)
- Velopix1 was submitted as an engineering run on May 2016
- First wafers received on 31st August 2016
- Design work very well, but:
  - Found an unexpected SEL (Single Event Latch-up) sensitivity in the pixel matrix
  - SET (Single Event Transient) in the SLVS receivers)
  - High speed links (5.12 Gbps) showed excess jitter:
    - From the PLL
    - Internal supply VDD-GND bouncing due to not sufficient power internal decoupling
- Velopix2 submitted on August 2017 → All good
- Velopix2 is currently being integrated in the experiment

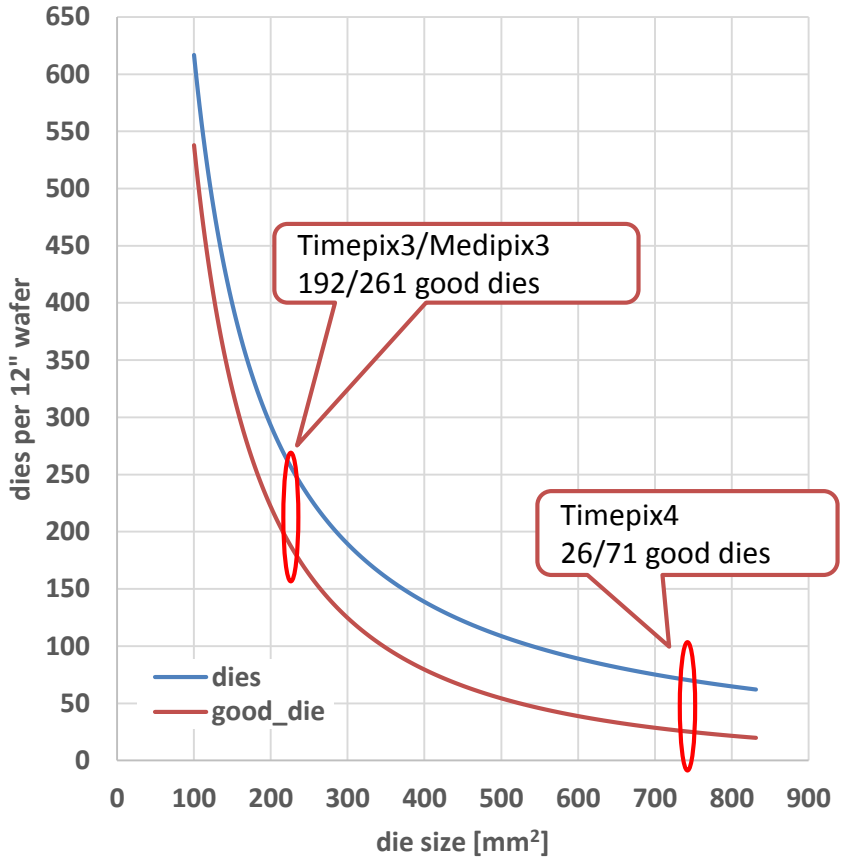


VeloPix wafers

Expected Timepix4 Yield

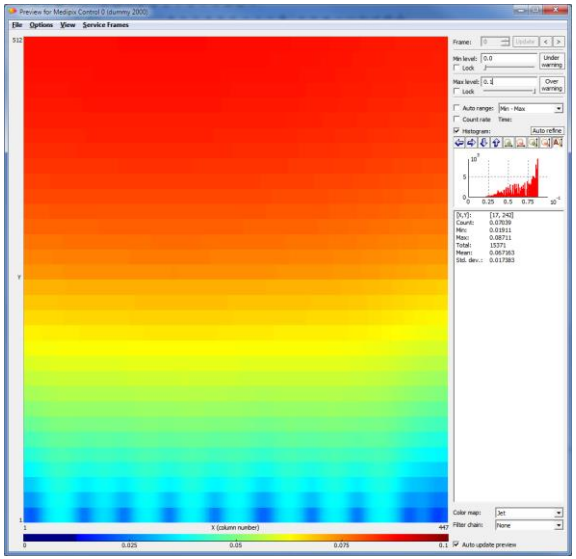
Based in the foundry yield model for perfect dies

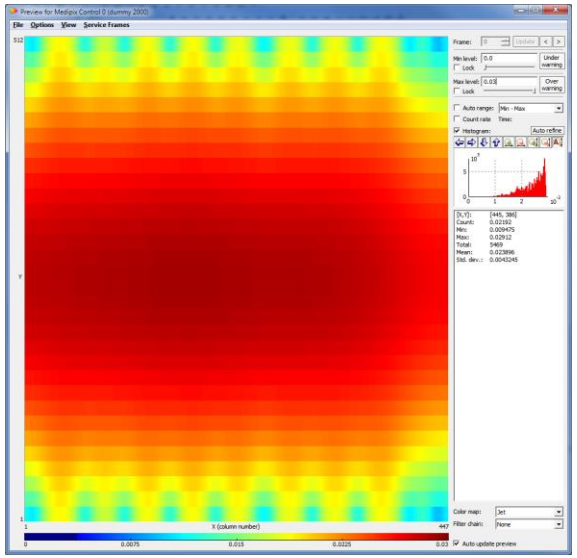


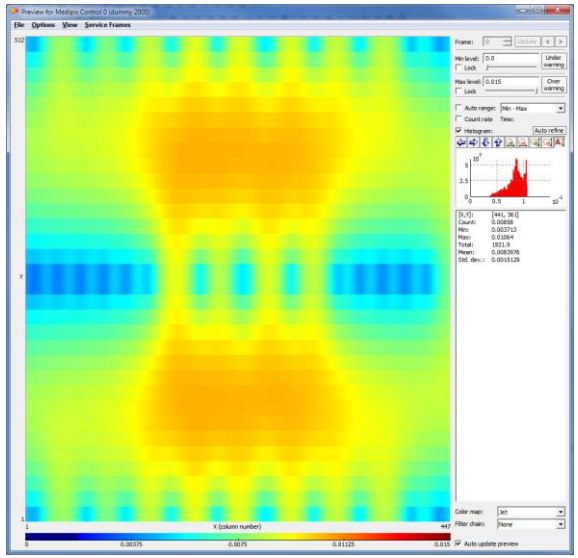


Analog (static) power supply distribution

	1 WB		2WB	3TSV
Nominal Analog Power [10 µA/pixel]	V_{drop} [max-min]	68 mV	19.6 mV	6.9 mV
	Imax pad	118 mA	60 mA	57 mA
Low Analog Power [1 µA/pixel]	V_{drop} [max-min]	6.8 mV	1.96mV	0.69mV
	Imax pad	11.8 mA	6 mA	5.7 mA





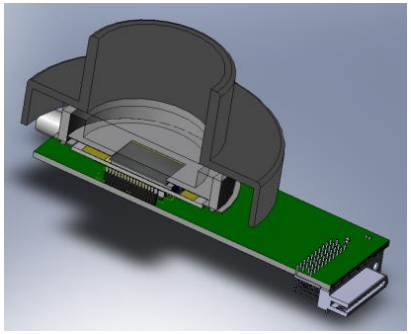


Readout systems

- Many different readout systems available:

	I/O interface	Timepix port	fps	# chips	Power
Fitpix (UTEF)	1 x USB2.0	Serial	≤80fps	≤16 in daisy chain	1 chip: USB or external (~1W) >1 chip: external
Maxipix (ESRF)	ESRF prop	Parallel	≤1400fps	1, 2x2, 5x1	External (~30W)
eX Series (xray-Imatek)	GBit Ethernet USB2.0	Parallel	≤3440fps	1, 2x2, 2x4	External (24W)
STPX-(ASI)	GBit Ethernet	Serial	≤120fps	1, 2x2,8x8	
RASPIX					

Optical High-Speed Imaging

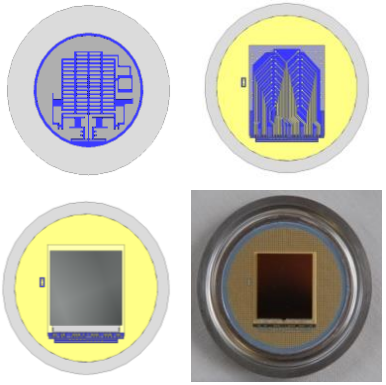


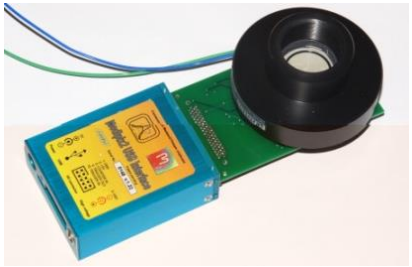
Single Photon counting

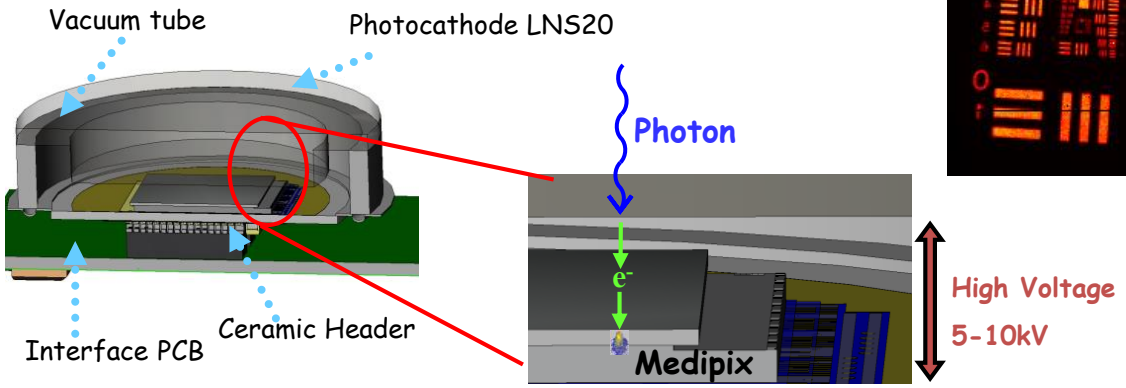
Pixelated detector

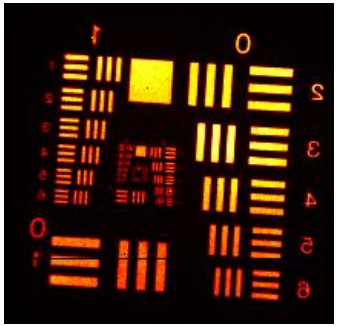
Unprecedented frame rates

Successor to the EMCCD?









K. Smith, V. O'Shea and co-workers, Glasgow, GB

APPLICATIONS

Timepix Applications

- New Tracking Technologies
  - LHCb Upgrade
  - CLIC detectors
  - Solid state Detector Development
- TPC instrumentation
  - EUDET
- Emission Channeling Crystal Lattice Experiments
  - ISOLDE
- Image Intensifiers / Optical Photon Detectors
  - Adaptive Optics
  - Bioimaging
  - LHCb RICH
- ToF Mass Spectrometry
  - Proteomic Imaging at AMOLF and Oxford
- Imaging Mass Spec
  - Functional Cellular Biology at Kiev
- Photo Electron Emission Microscopy and Low Energy Electron Micrsocopy
- Neutron Monitoring at CNGS
- Space Dosimetry
- Education - CERN@School