protoDUNE-SP LArTPC Cold Electronics Quality Control and Commissioning

BNL, 2019-07-31

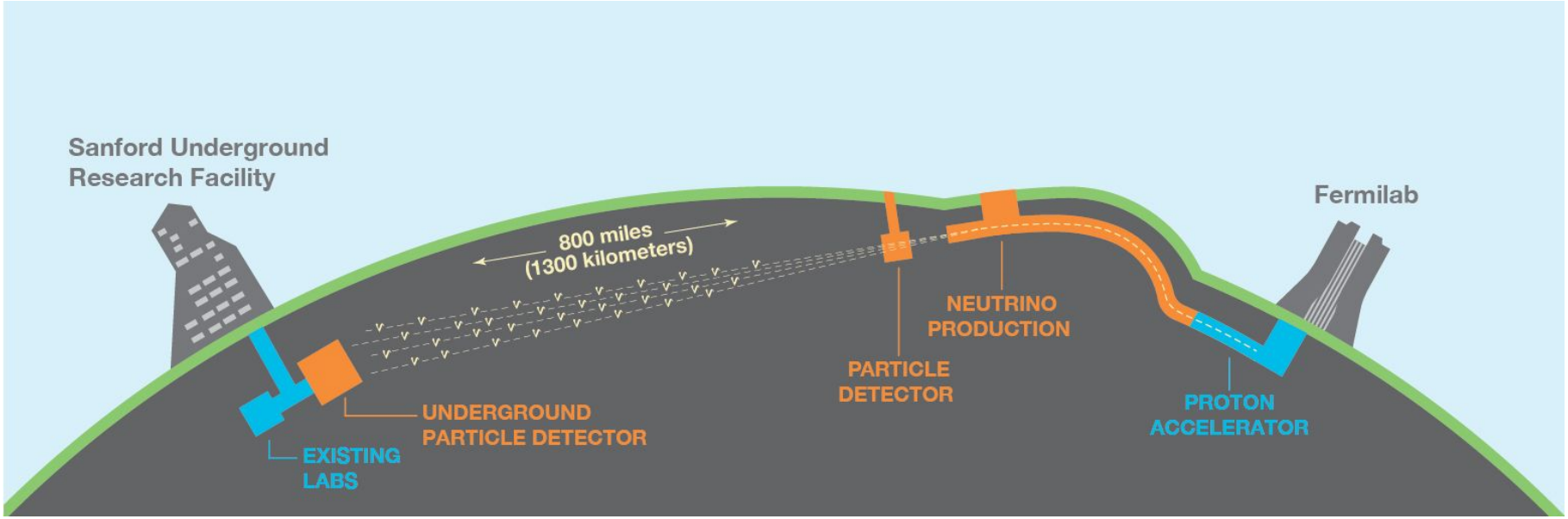
B.Kirby on behalf of the DUNE Collaboration

APS DPF 2019

DEEP UNDERGROUND NEUTRINO EXPERIMENT

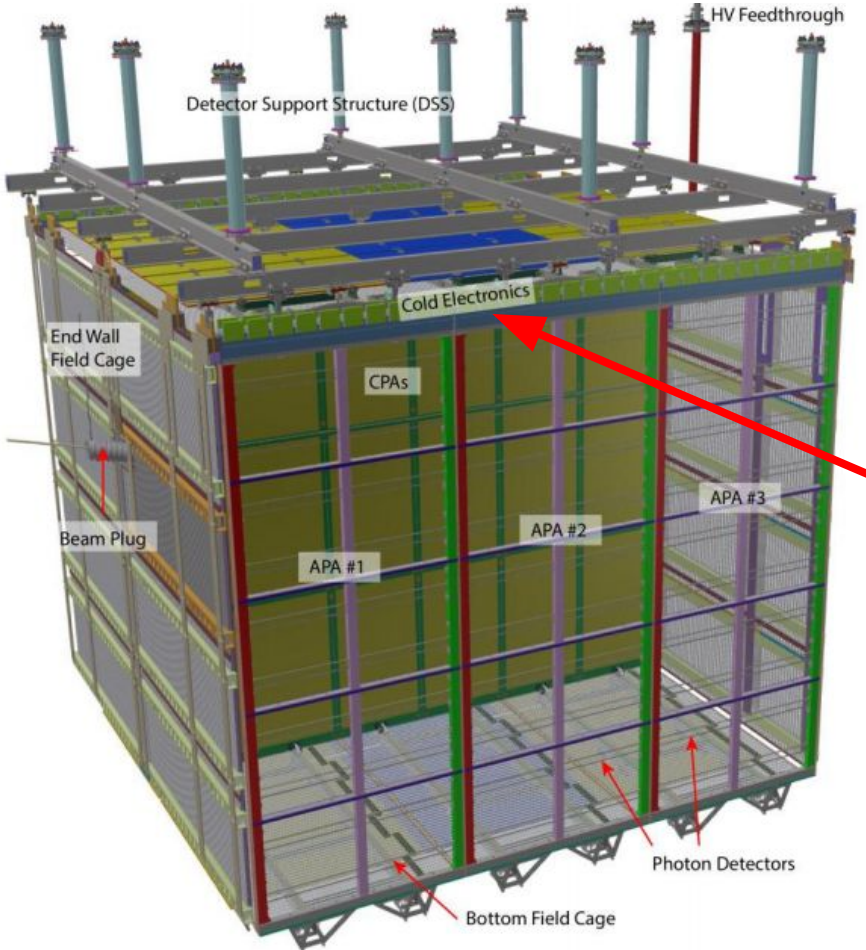
BROOKHAVEN NATIONAL LABORATORY

Deep Underground Neutrino Experiment (DUNE)



- Long-baseline neutrino oscillation experiments measure ν_e appearance amplitude and constrain neutrino mixing parameters
- Deep Underground Neutrino Experiment (DUNE) is a next-generation neutrino oscillation experiment
- 1300km baseline and 40kt active target mass in far detector

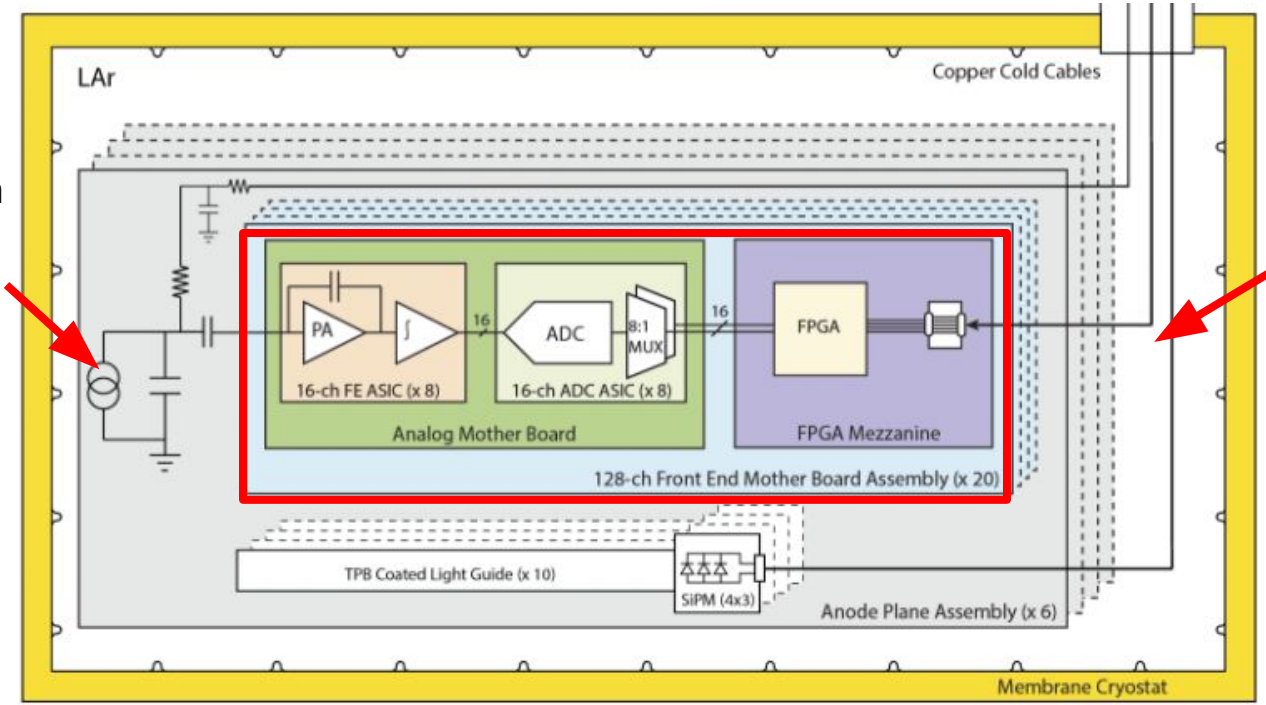
protoDUNE Single Phase (SP) Prototype



- protoDUNE-SP is large-scale prototype of DUNE single-phase Liquid Argon Time Projection Chamber (LArTPC) at CERN
- 15360 individually instrumented TPC wires in six Anode Plane Assemblies (APAs) within 770t LAr cryostat
- Low noise cold electronics operate at cryogenic temperature inside the cryostat
- **Goal: demonstrate performance and stability of DUNE single-phase far detector design**
  - **Characterize response to charged particles from CERN low energy beam line**

protoDUNE-SP LArTPC Cold Electronics Overview

Input: Current from ionization charge induced/collected on TPC Wires

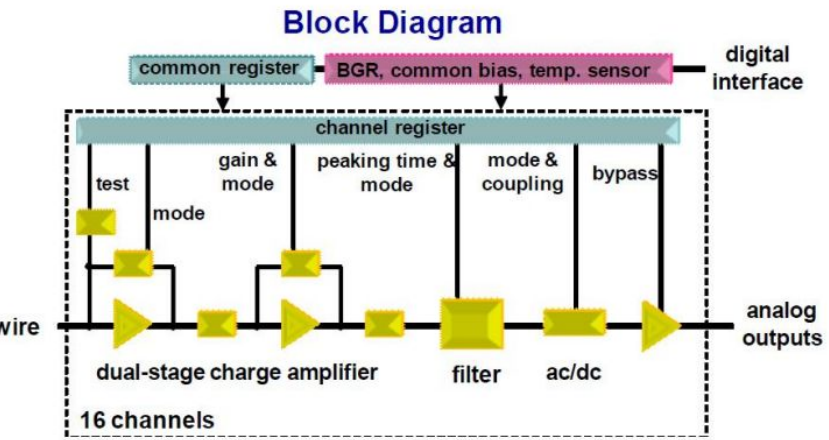


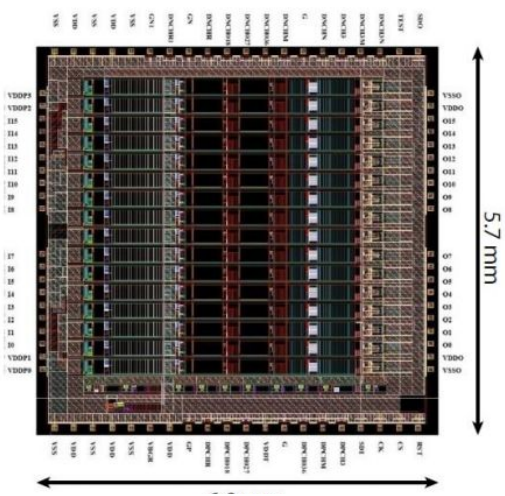
Digital and LV cabling

- Cold preamps located inside the cryostat reduces electronic noise
- Cold sampling+digital logic controls readout and simplifies cabling/feedthroughs
- Implemented in compact Front End Mother Board (FEMB) integrated wire readout

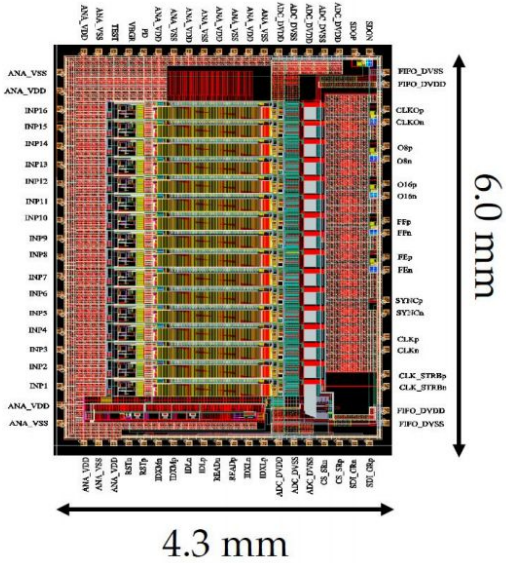
Cold Electronics: Front End and ADC ASICs

Cold FE ASIC





Cold ADC ASIC



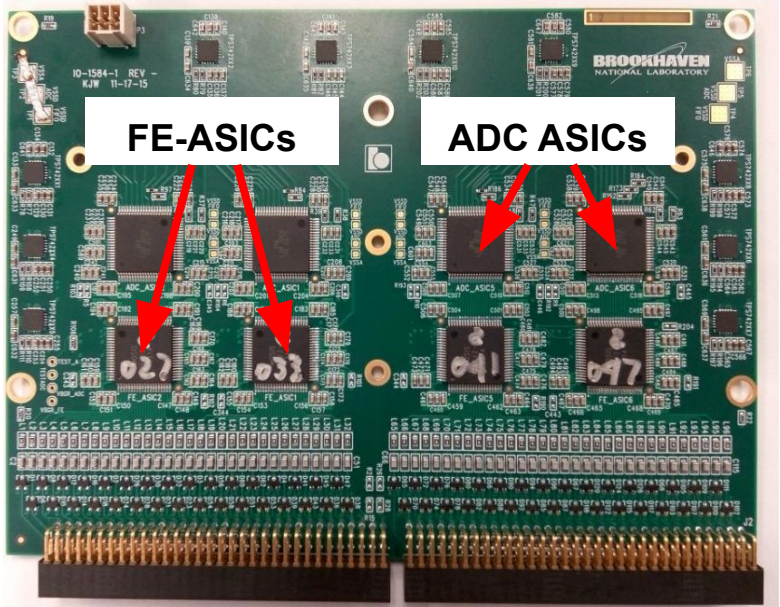
- Cold electronics include cold preamps and ADCs
- 16 channel preamp+shaper Front End ASIC (FE-ASIC)
  - Designed for low-noise cryogenic operation, long lifetime
  - LArASIC design used in multiple LArTPC experiments
- 16 channel digitizing cold ADC ASICs sample at 2MHz, 8:1 serialization

Cold Electronics: Front End Mother Boards

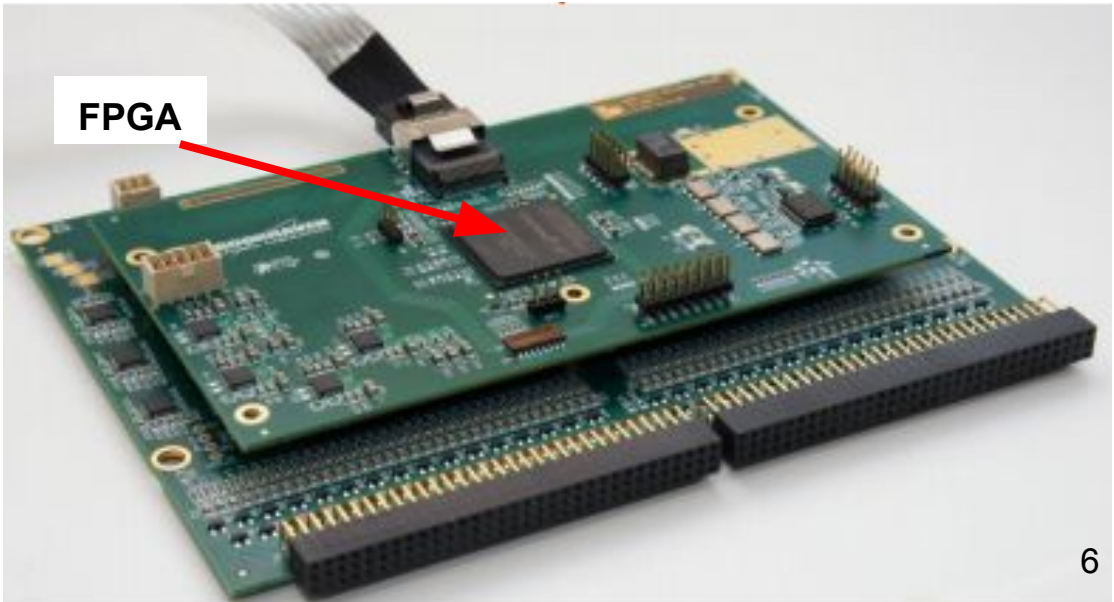
- **Front-End Mother Boards (FEMBs)** integrate analog, digital electronics
- **Analog board:** 8 pairs of FE ASICs and ADC ASICs, 128 channels total
- **FPGA board**: Programs and coordinates ASIC operation and readout, multiplexes and streams data to backend through GB transceivers

120 FEMBs required for 15360 protoDUNE-SP Wires

Analog and ADC Board



SBND/protoDUNE-SP FEMB

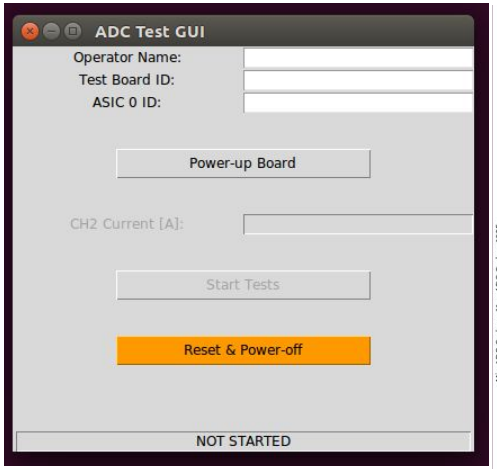


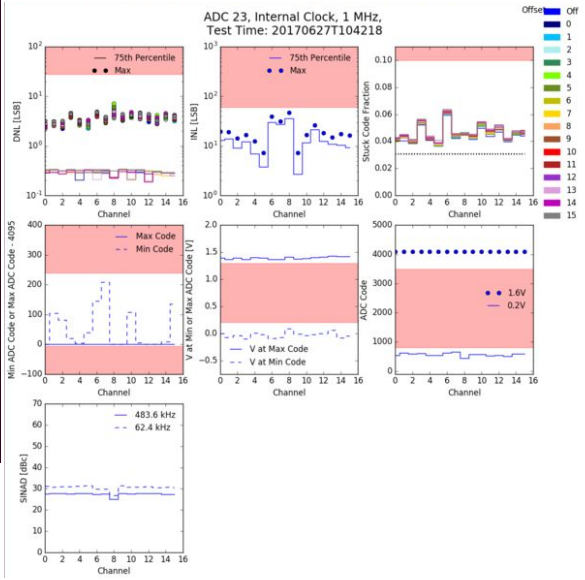
protoDUNE-SP LArTPC Cold Electronics Quality Control Effort

- 15360 cold electronic channels requires large electronics production and quality control (QC) effort
  - Cryogenic testing requirement introduces additional challenges
- Implemented a set of semi-automated test stands to address QC challenge:
  - Developed open-source quality control test automation software
  - Implemented dedicated quality control test stands for:
    - On-board oscillators - 120 required
    - Flash Memory - 120 required
    - FE ASICs - 960 required
    - ADC ASICs - 960 required
    - Fully assembled FEMBs - 120 required
- Electronics production tests performed at BNL
  - Relied on large number of protoDUNE collaborators to operate test-stands (**Thanks!**)
- Acceptance tests at CERN ensured performance of delivered boards

Quality Control:Test Software

Example ADC ASIC Test GUI and Online Summary Plots



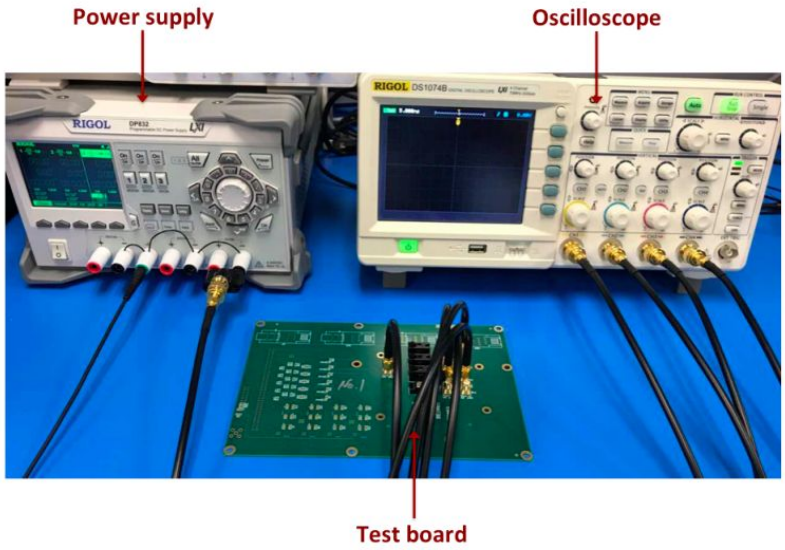


- Production electronic test processes and validation data-taking controlled by python-based software package
  - Automated data-taking, archiving
  - Online analysis to determine if component is accepted
  - Simplified interface for shifters
  - Full documentation of test procedures and reproducibility via version control

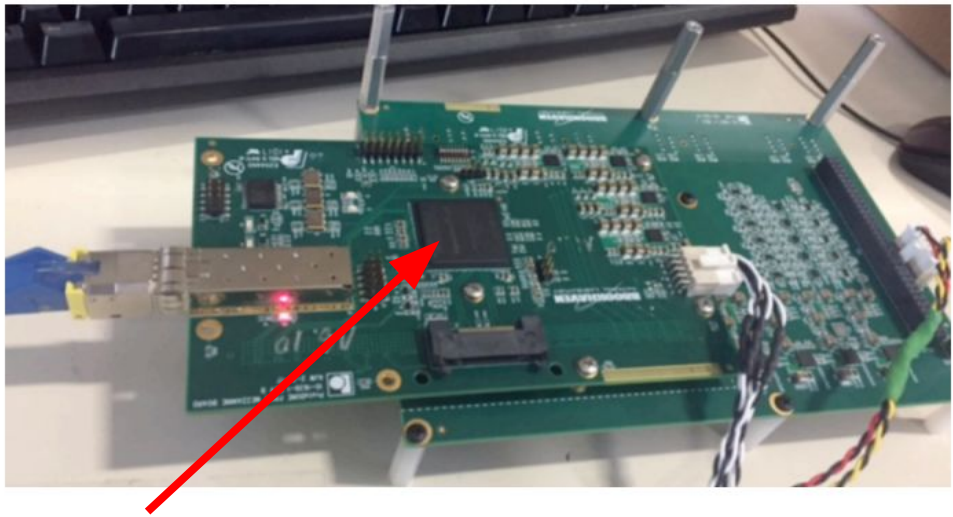
Enables systematic evaluation+QC of protoDUNE-SP electronics production

Quality Control: Oscillator + Flash Memory Tests

100MHz Oscillator Test Board



Flash Memory Test Board

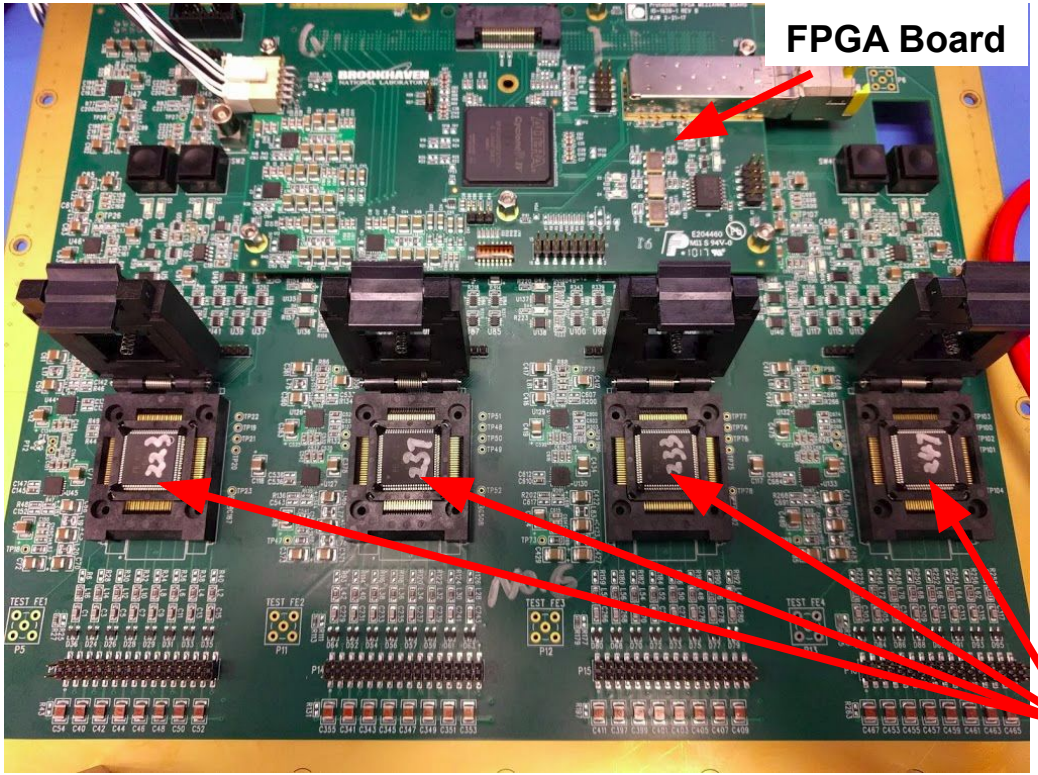


FPGA - Flash memory sockets underneath board

- Oscillator and flash memory tests evaluate cryogenic functionality
- Identify oscillators/flash memories likely to fail after assembly
  - Avoid reworking assembled boards!

Quality Control: Front-End ASIC Tests

FE ASIC Quad Chip Tester



- Quad-chip tester designed at BNL qualifies up to 4 FE ASICs at a time
- Initially only room temperature tests, cold tests later implemented
- Verified FE ASIC functionality: SPI configuration, internal ASIC DAC, detect bad pins
- Measured FE ASIC performance channel pedestal, gain, ENC etc
- ASICs accepted based on functionality and passing z-cuts on measured performance

Quality Control: ADC ASIC Chip Tests

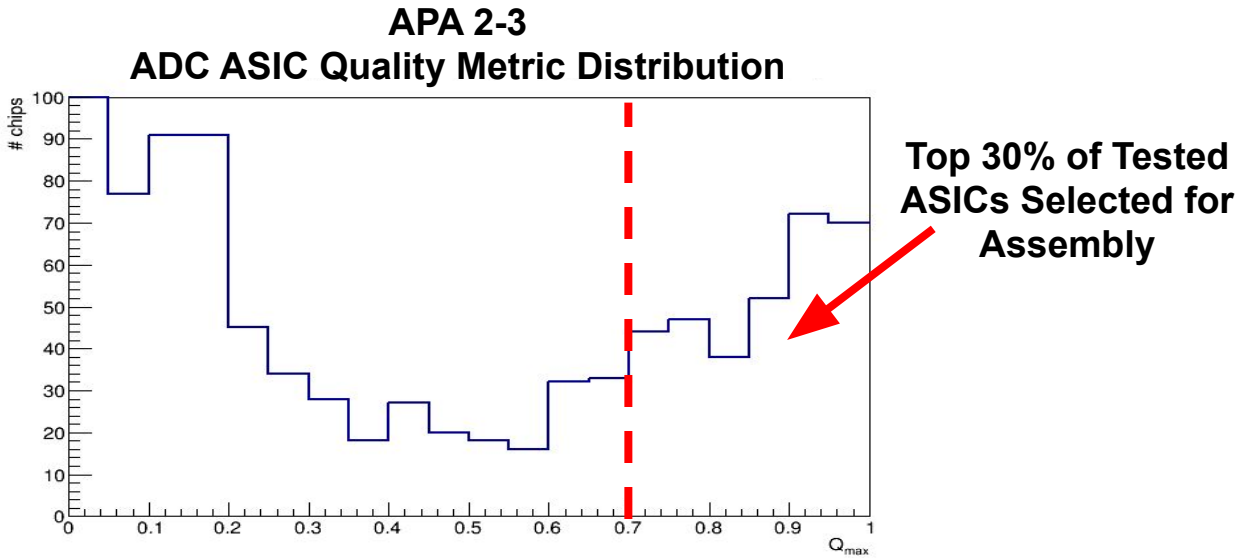
ADC ASIC Chip Tester

ADC ASIC Chip with ASIC Immersed in Liquid Nitrogen

- ADC ASIC tests performed at room and cryogenic temperature using single socket board
- Tests evaluated ADC ASIC functionality and performance
  - Measured ADC linearity, INL, DNL, detect broken pins etc
- Identified measures to simplify cryogenic testing, improve test reliability

Quality Control: ADC ASIC Selection

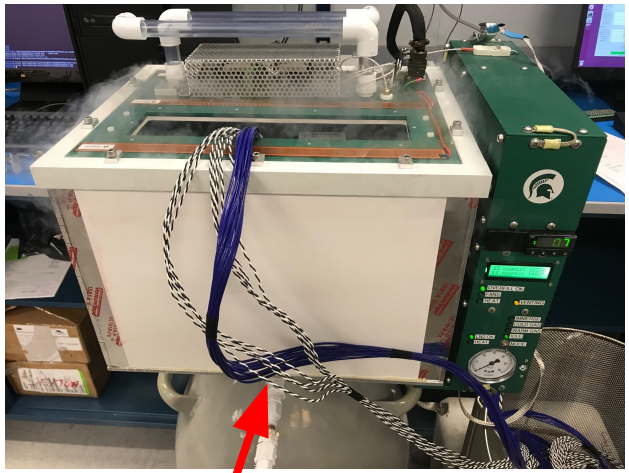
- Metric developed to quantify ADC ASIC relative performance
  - Combines dynamic range and DNL information for all 16 channels
- **Significantly more** ADC ASICs tested than required to assemble FEMBs
  - Selection applied to use higher performing ASICs in detector
  - Only fully-functional ASICs (ie no dead channels) included in selection



Quality Control: Assembled FEMB Tests

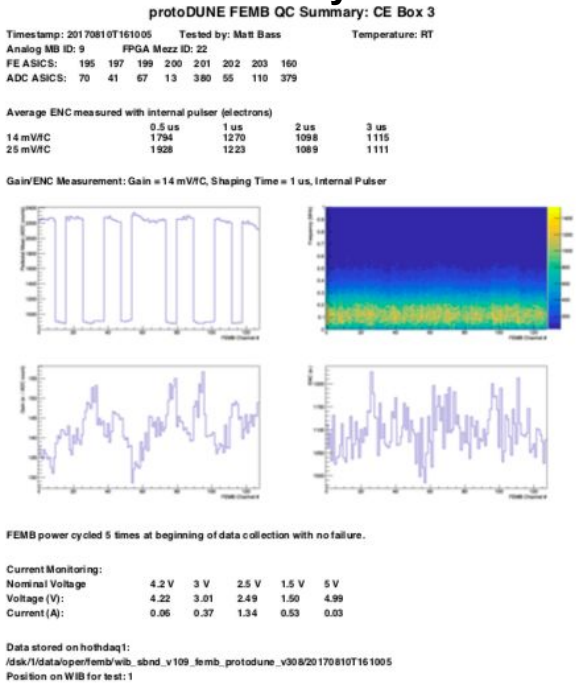
FEMB Test Setup

FEMB Tested in Automated Dewar



Cold LV and digital cables treated as part of the assembled FEMB

Generated Summary Document



protoDUNE FEMB QC Summary: CE Box 3

Timestamp: 20170810T161005 Tested by: Matt Bass Temperature: RT

Analog MB ID: 9 FPGA Mezz ID: 22

FE ASICS:	195	197	199	200	201	202	203	160
ADC ASICS:	70	41	67	13	380	55	110	379

Average ENC measured with internal pulser (electrons)

	0.5 us	1 us	2 us	3 us
14 mV/fC	1794	1270	1098	1115
25 mV/fC	1928	1223	1089	1111

Gain/ENC Measurement: Gain = 14 mV/fC, Shaping Time = 1 us, Internal Pulser

FEMB power cycled 5 times at beginning of data collection with no failure.

Current Monitoring:

Nominal Voltage	4.2 V	3 V	2.5 V	1.5 V	5 V
Voltage (V):	4.22	3.01	2.49	1.50	4.99
Current (A):	0.06	0.37	1.34	0.53	0.03

Data stored on hothdaq1:
/dsk/1/data/oper/femb/wib_sbnd_v109_femb_protodune_v308/20170810T161005
Position on WIB for test: 1

- FEMB test stand uses real DAQ board to evaluate fully assembled FEMB + cold cable performance, “final” check-out
- Tests measure gain+noise on various FE-ASIC settings, auto-summarizes results
- Evaluated automated dewar from MSU that controls cooldown and immersion in LN2

Quality Control: Production Test Results

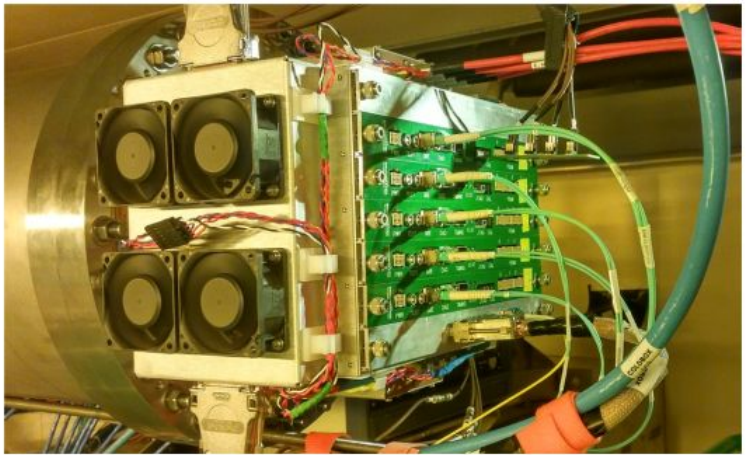
Component Type	# Tested	Rejection Rate
100 MHz Oscillators	700	35.7%
Flash Memory	860	77.9%
Pre-amplifier ASIC	1850	5.6%
ADC ASIC	3680	14.6%
Assembled FEMBs	139	2.8%

- Production testing effort largely successful, electronics delivered on time
  - Automation and component cryogenic pre-testing was crucial to minimize FEMB rejection rate
- Experience relevant for DUNE electronics production, requires >3000 FEMBs

protoDUNE-SP Cold Electronics Installation at CERN

- FEMBS delivered to CERN were tested on receipt and after installation on APAs in a dedicated cold box integration test facility
  - Cold box tests verified integrated electronics cryogenic performance, checked for issues
  - Problem with cable connectors (not tested in QC) that could have affected up to 15 FEMBs identified through these tests

Full Scale Warm Feedthrough for Cold Box Tests

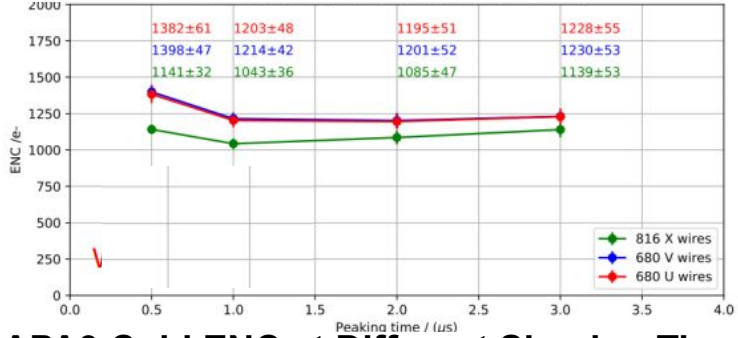


- FEMB and DAQ electronics allowed real-time studies of detector performance in integration tests and electronic noise debugging
- Using same DAQ electronics for QC as in real detector helped debugging tool development

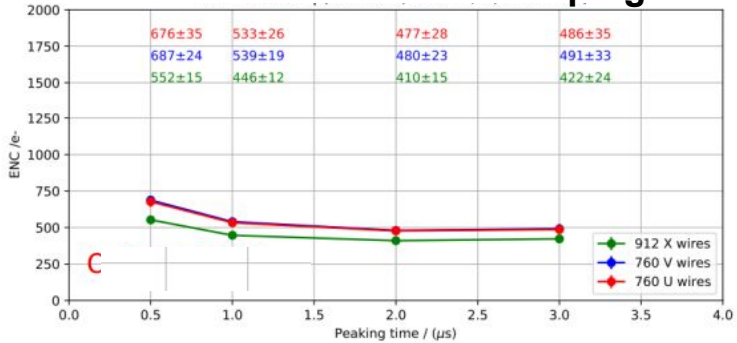
Integrated LArTPC Cold Electronics Performance

- Integrated LArTPC cold-electronics performed extremely well after cooldown
  - **99.96%** of electronic channels working (only 6 inactive channels after 9mo operation)
  - 99.73% connected to TPC wires (15318 out of 15360)
  - Excellent noise performance (<800e- ENC) on large majority of channels

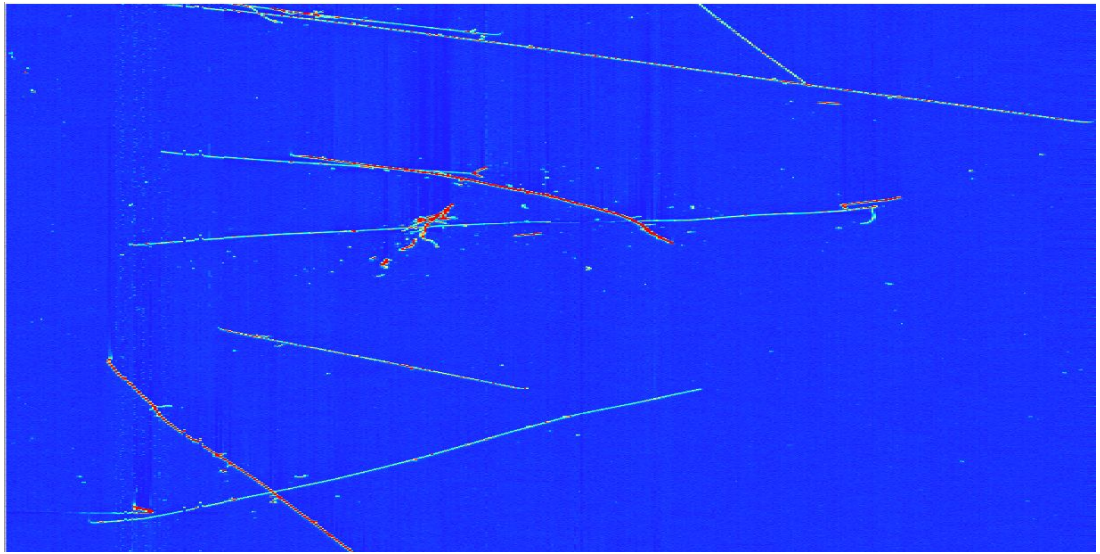
APA3 Warm ENC at Different Shaping Times



APA3 Cold ENC at Different Shaping Times



protoDUNE-SP Event Display



Quality control ensured excellent electronics performance, leading to successful detector operation

Summary

- protoDUNE-SP is a prototype of DUNE-style LArTPC cold electronics
  - Operated in successful beam test Oct 2 to Nov 13 2018, ongoing cosmic data-taking run
- Quality control effort used dedicated test-stands and automated software to validate protoDUNE-SP cold electronics
- Integration testing and commissioning effort yielded excellent electronics performance, 99.96% electronic channels working
- Many lessons learned that can be applied to DUNE and other future LArTPCs

Backup