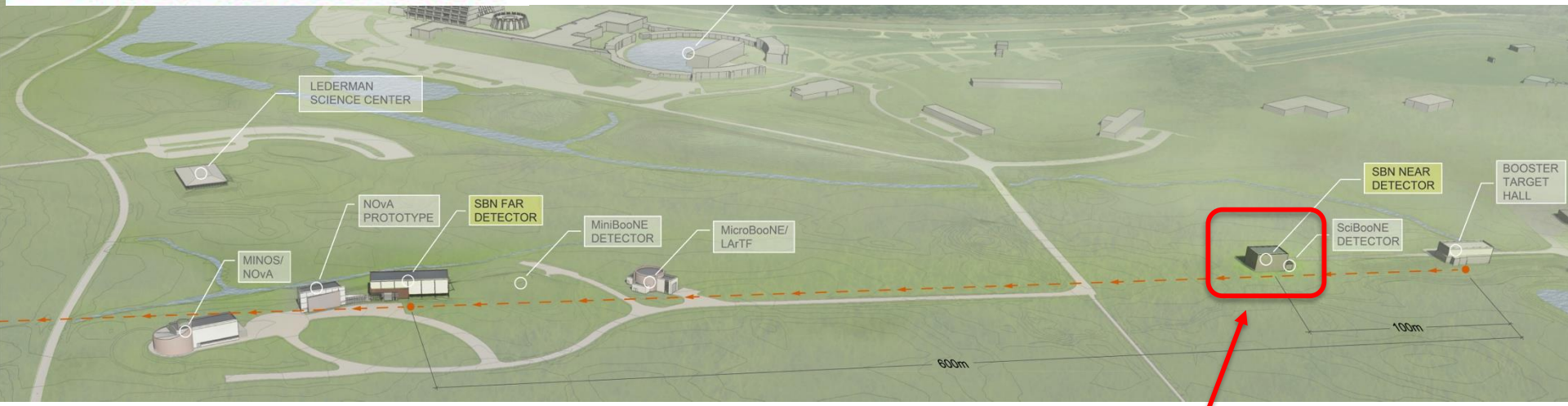
2019 DPF Northeastern

BROOKHAVEN NATIONAL LABORATORY | Fermilab | U.S. DEPARTMENT OF ENERGY | Office of Science

2019 Meeting of the Division of Particles & Fields of the American Physical Society



Low Noise Cold Electronics System for SBND LAr TPC

Shanshan Gao on behalf of the SBND collaboration

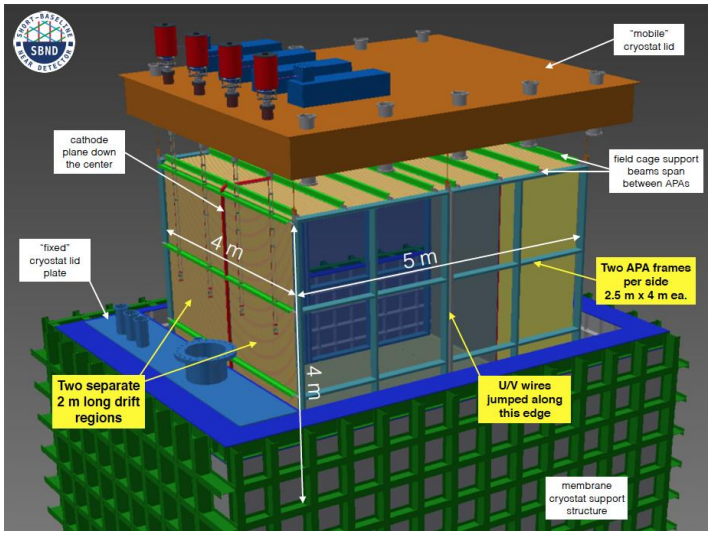
Brookhaven National Laboratory

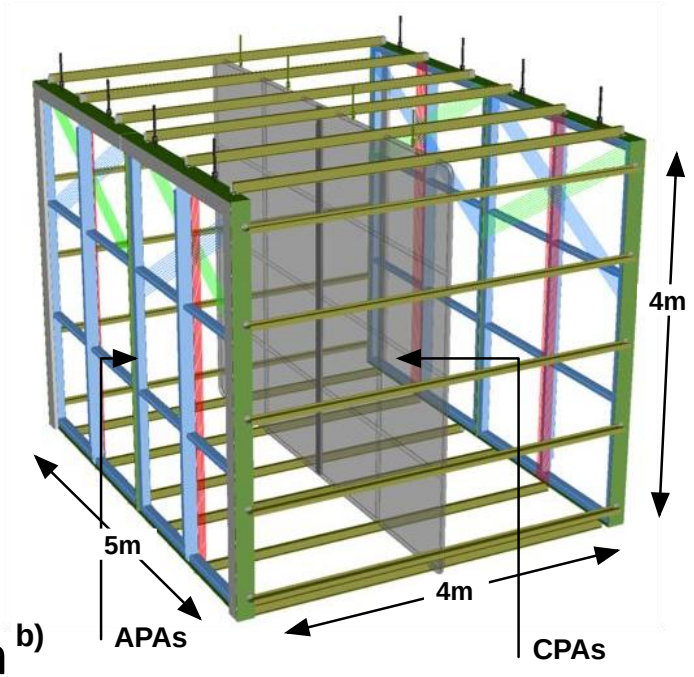
07/31/2019

Outline

- Overview of SBND Experiment
- SBND TPC Cold Electronics Development
- System Integration Test and ENC Projection
- QA/QC Procedure for Cold Electronics Production
- Summary

SBND Experiment



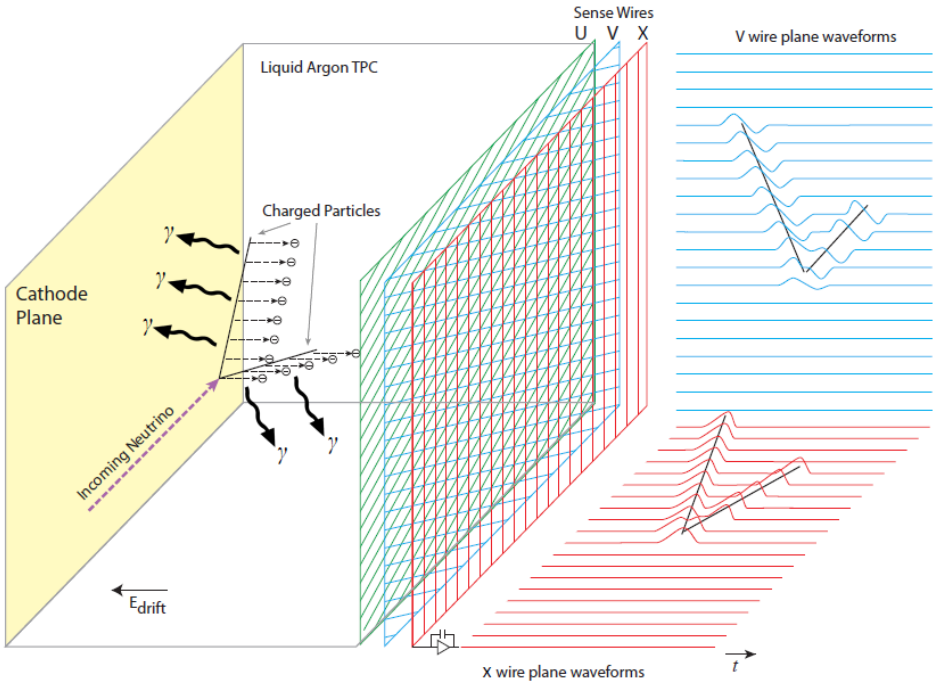


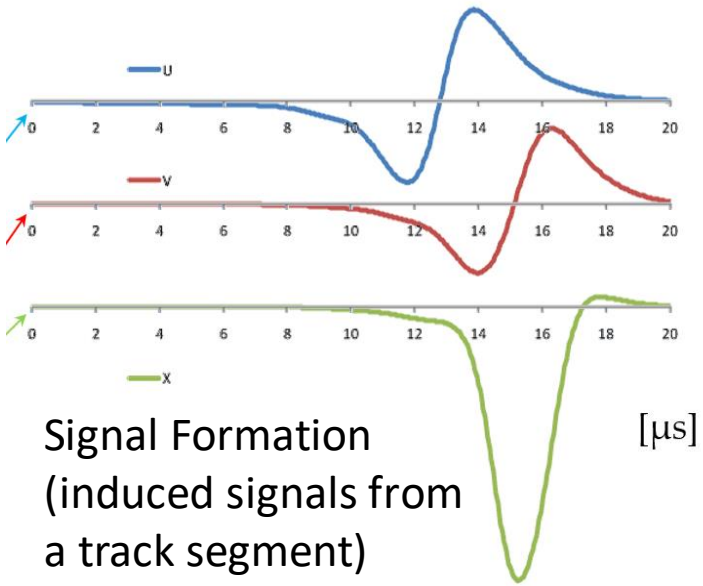
b)

- SBN (Short Baseline Neutrino) program
  - Use Booster Neutrino Beam for sterile neutrino search
  - 3 detectors: SBND, MicroBooNE and ICARUS
  - SBND is expected to be in operation in 2020
- SBND is a 260 ton LAr TPC as near detector in SBN program
  - Central cathode plane assembly (CPA), 2 anode plane assemblies (APA) on either side w/ 2m drift distance each
  - 11,264 sense wires to be read out
  - **Cold electronics enables an optimum balance** among various design and performance requirements for large LAr TPC detector

LAr TPC (Liquid Argon Time Projection Chamber)

Charged particles passing through detector ionize the argon atoms, and the ionization electrons drift in the electric field to the anode wall on a timescale of milliseconds. The anode consists of layers of active wires forming a grid.

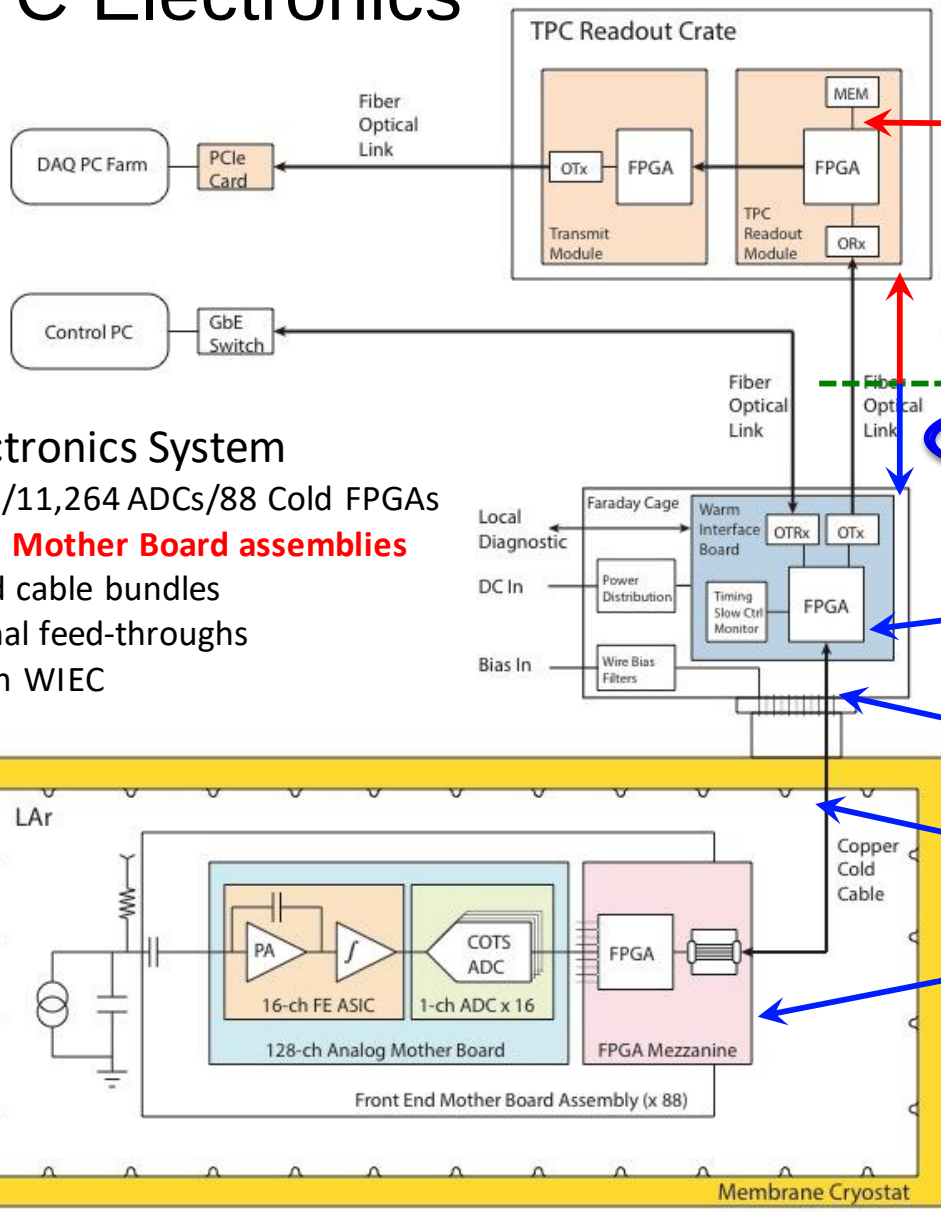




Signal Formation (induced signals from a track segment)

Time information: when ionization electrons arrive (drift distance)
Geometry information: which wires are fired (transverse position)
Charge information: how many ionization electrons (energy deposition)

SBND TPC Electronics



TPC Readout Electronics

Nevis

Back End Electronics

Front End Electronics

BNL

Warm Interface Electronics

Signal Feed-through

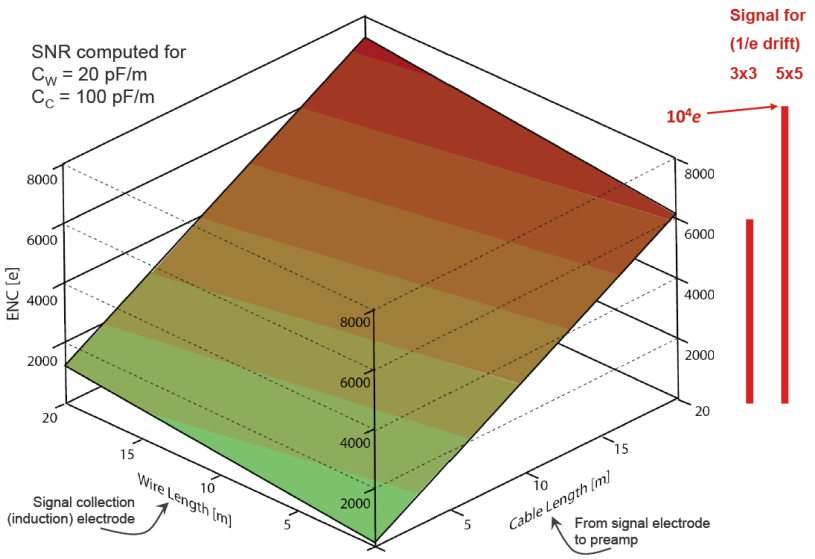
Cold Cable

Cold Electronics

- Front End Electronics System
  - 704 FE ASICs/11,264 ADCs/88 Cold FPGAs
  - **88 Front End Mother Board assemblies**
  - 4 sets of cold cable bundles
  - 4 sets of signal feed-throughs
  - ~28 boards in WIEC

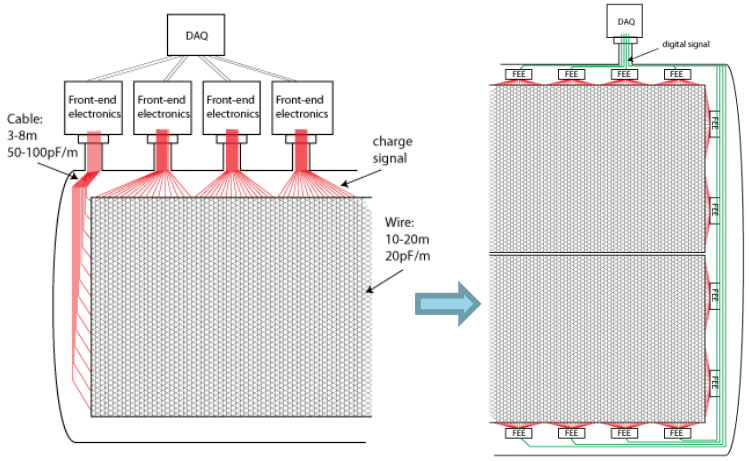
Motivation of Cold Electronics (CE) in Large LAr TPC

Much lower noise



- Integrated front-end electronics close to detector electrodes yields the best SNR
- CMOS in LAr has less than half the noise as that at room temperature

Much less cryostat penetrations

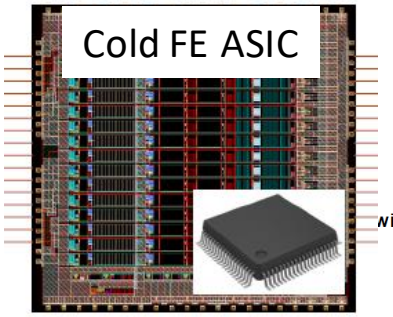


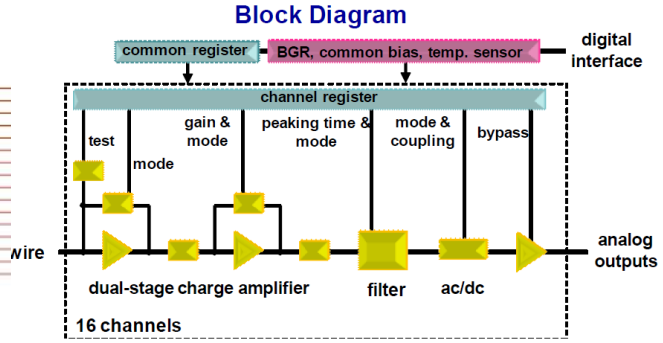
Warm Readout vs. Cold Readout

- Signal digitization and multiplexing to high-speed links inside the cryostat results in large reduction in cables and feed-through penetrations, and the freedom to choose the optimum configurations for both the TPC and the cryostat

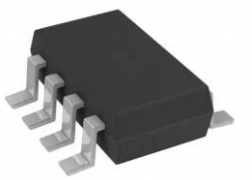
- BNL has started cold electronics study since 2008
  - Successful deployment of cold electronics system in MicroBooNE and ProtoDUNE-SP along the CE R&D with collaborators

CMOS Devices Qualified for Cryogenic Operation

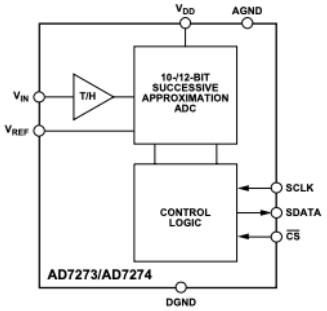




16 channels, programmable
Charge amplifier
Adjustable gain: 4.7, 7.8, 14, 25mV/fC
Adjustable filter time constant
Designed for 77K-300K operation
Designed for long lifetime
Tech. CMOS 180 nm, 1.8 V, 6M, MIM, SBRES



AD7274BUJZ (COTS)



FPGA (COTS)

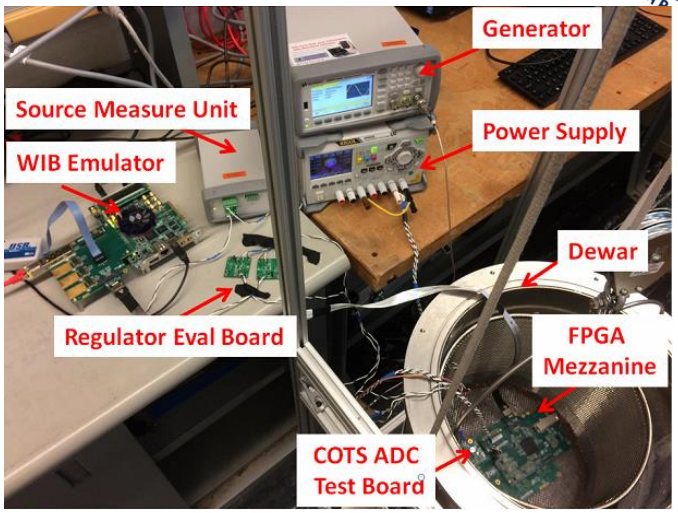
Voltage Regulator (COTS)
(< 100mV dropout)

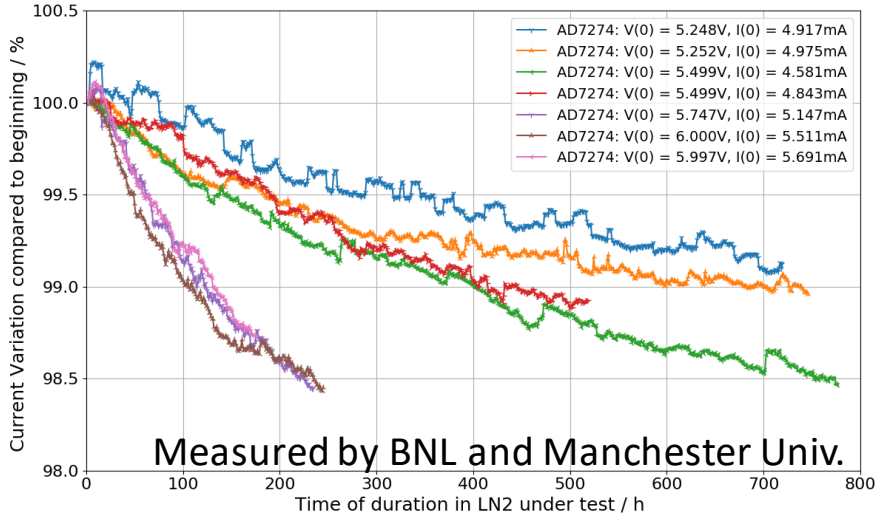
Commercial devices study

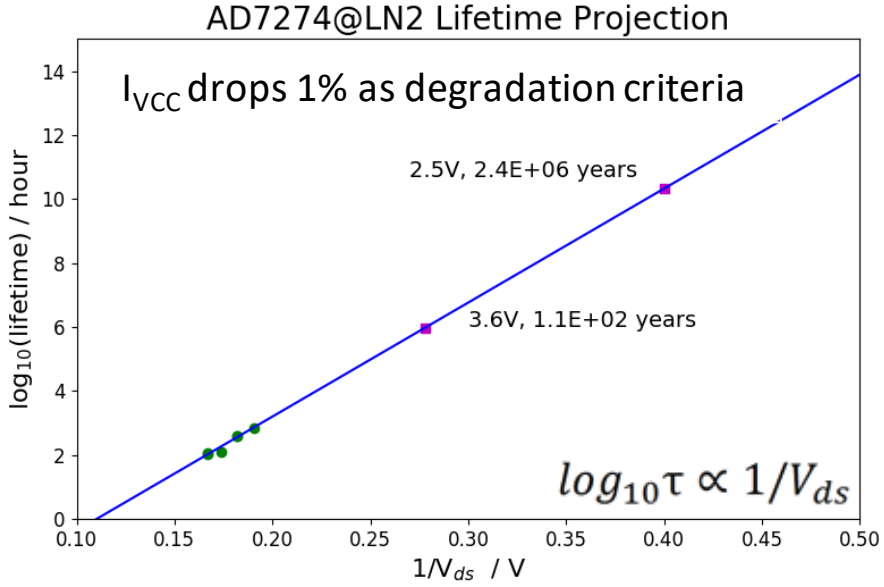
1. Screen various commercial devices to find survivors at LN2 temperature (77K)
   - **Single channel SAR ADC AD7274**
     12bit, 3MSPS, <5mW, ENOB 11.2bit
   - Cyclone IV GX FPGA
   - Low dropout voltage regulator
2. Lifetime study to determine qualified chips
   - Hot Carrier Effect (HCE) is the dominant degradation of CMOS at cryogenic temperature
   - Accelerated lifetime evaluation test
     CMOS circuit is placed under a severe electric field stress (large V_{DS}), to reduce the lifetime due to hot-electron degradation

SBND COTS ADC Cold Lifetime Study

- The COTS ADC work **benefits the future** program, which serves as a backup for DUNE far detector
- ***AD7274*** has gone through extensive lifetime study
  - 100% cold yield
  - 0.25 LSB scale DNL measurement
  - < 5 mW at 2MS/s







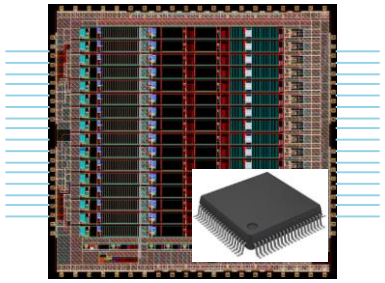
- The HCE is negligible for COTS ADC used in SBND, and **we'll be staying out of HCE during the detector operation**

SBND collaboration has made decision to use COTS ADC

A Complete Cold Front-end Readout Chain

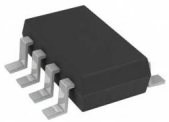
CMOS LDO

FE ASIC



COTS ADC

2 MS/s, 12 bit



16 x

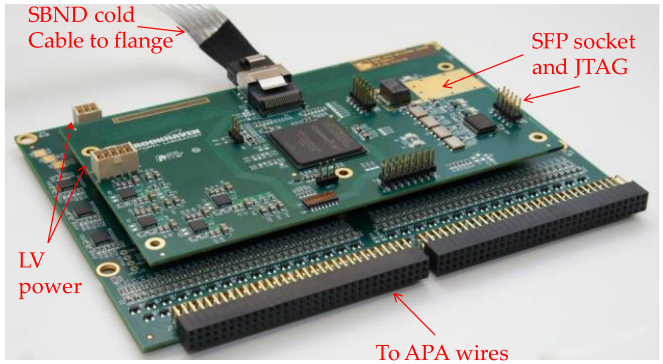
COTS FPGA

1 x

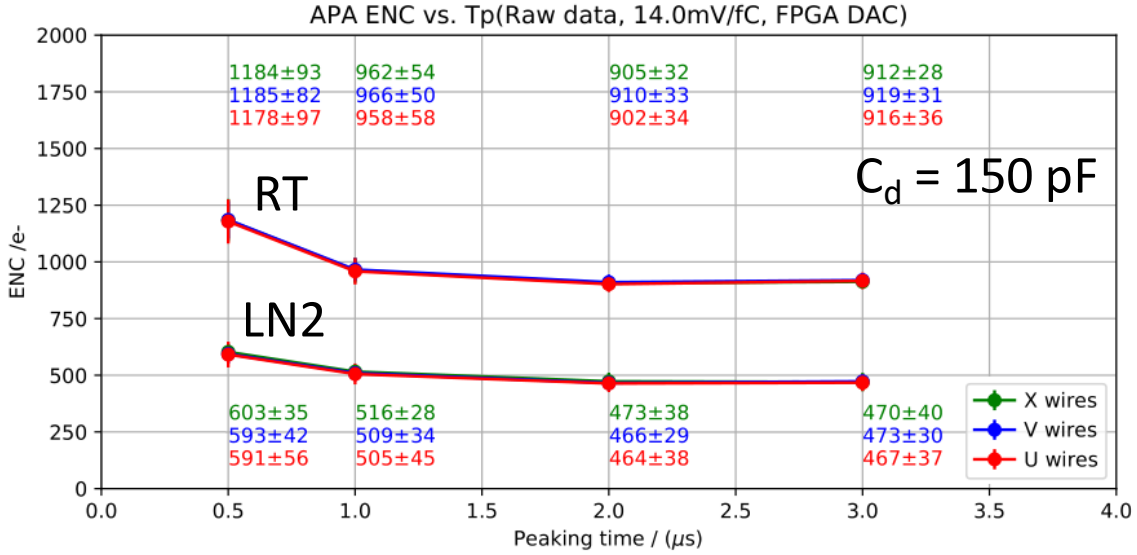
8 x

overall 128:4 multiplexing

128Ch Front End Motherboard Assembly (FEMB)



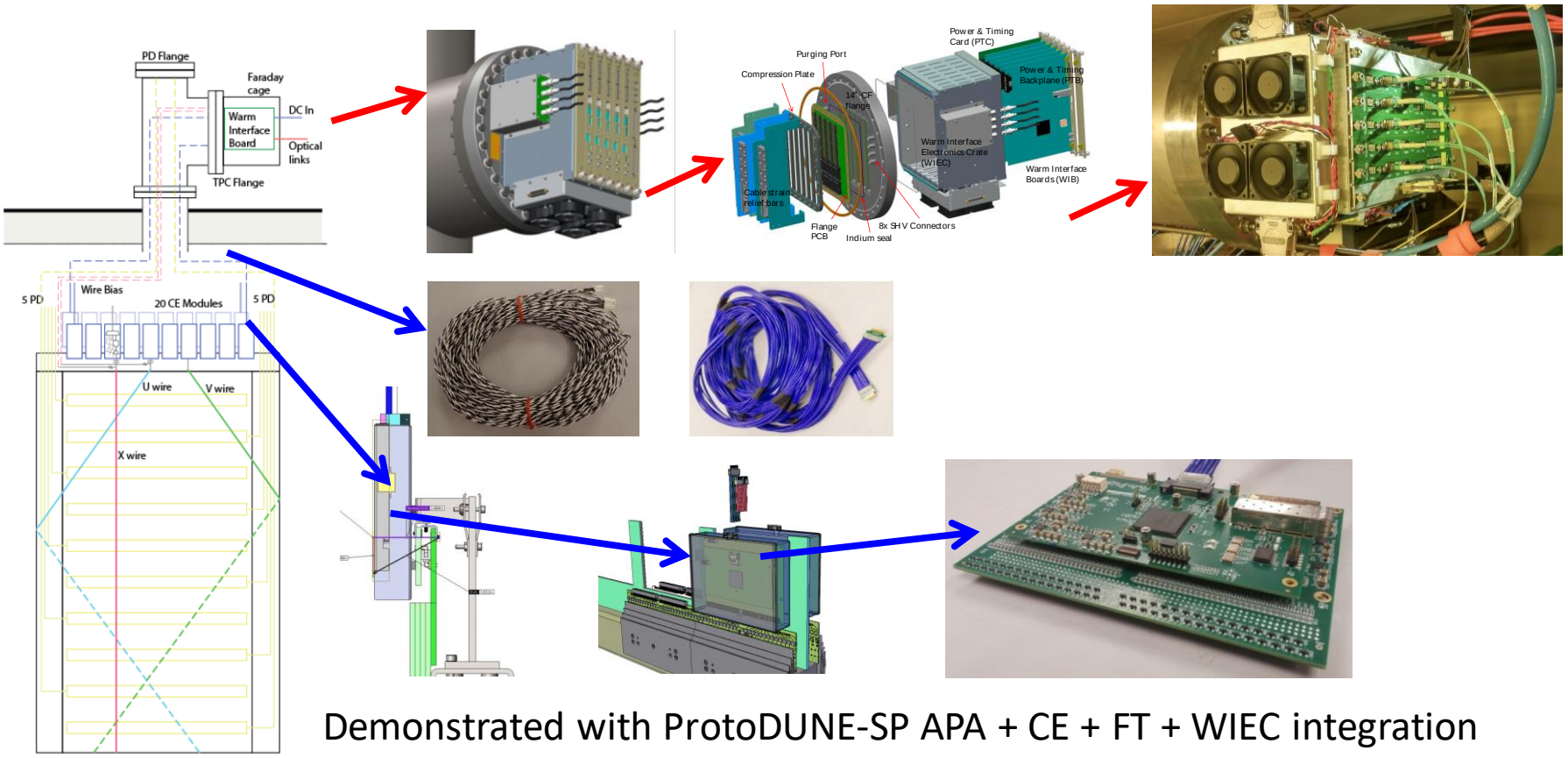
128 channels of digitized TPC wire readout with low noise



88 FEMB assemblies for 11, 265 sense wires in SBND TPC

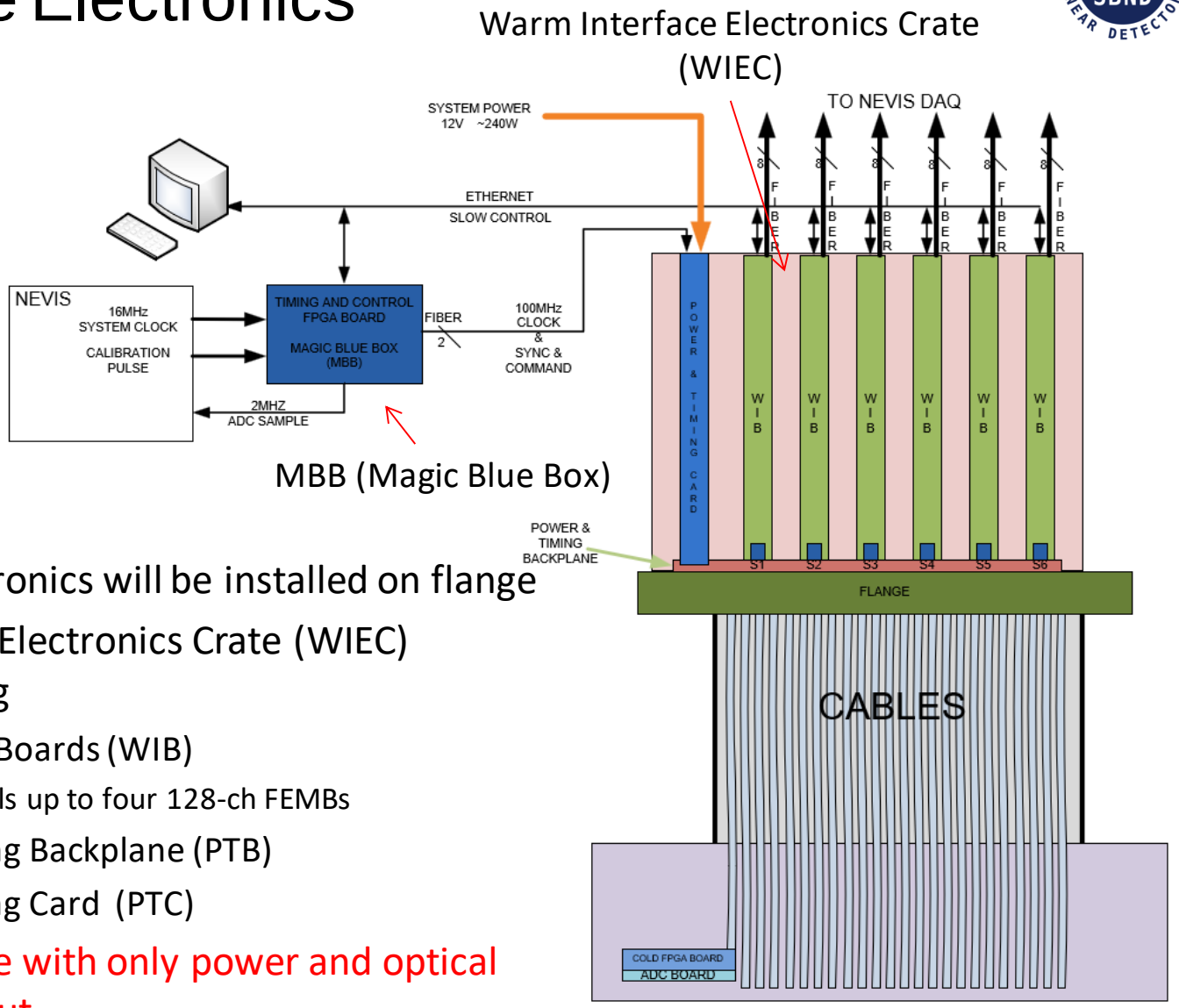
Integral APA and CE Concept

- A necessary (but not sufficient!) condition to achieve a good performance, the integral design concept of APA + CE + Feed-through, plus Warm Interface Electronics with local diagnostic and strict isolation and grounding rules will have to be followed



Demonstrated with ProtoDUNE-SP APA + CE + FT + WIEC integration

Warm Interface Electronics



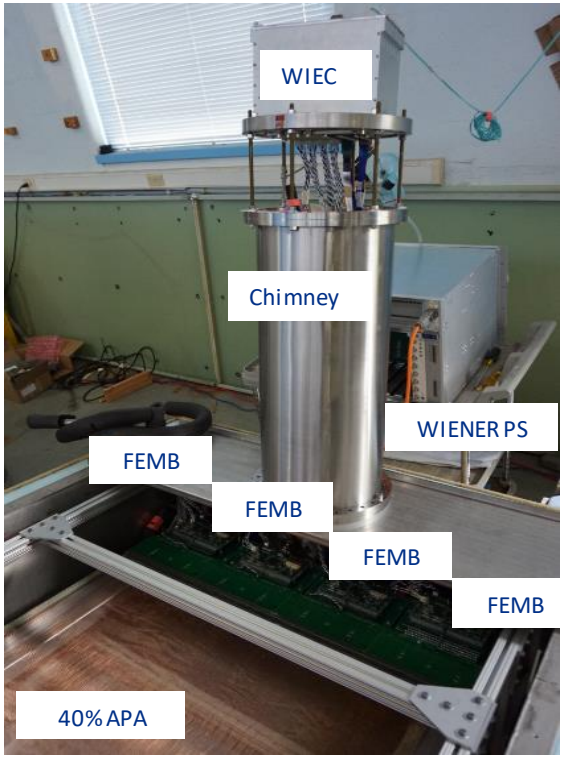
- Warm interface electronics will be installed on flange
- Each Warm Interface Electronics Crate (WIEC) contains the following
  - 6x Warm Interface Boards (WIB)
    - Each WIB controls up to four 128-ch FEMBs
  - 1x Power and Timing Backplane (PTB)
  - 1x Power and Timing Card (PTC)
- WIEC is a faraday cage with only power and optical signals going in and out

40% APA Integration Test Stand at BNL

4 layers: G, U, V, X
448 2.8m X wires
288 4.0m U wires
288 4.0m V wires

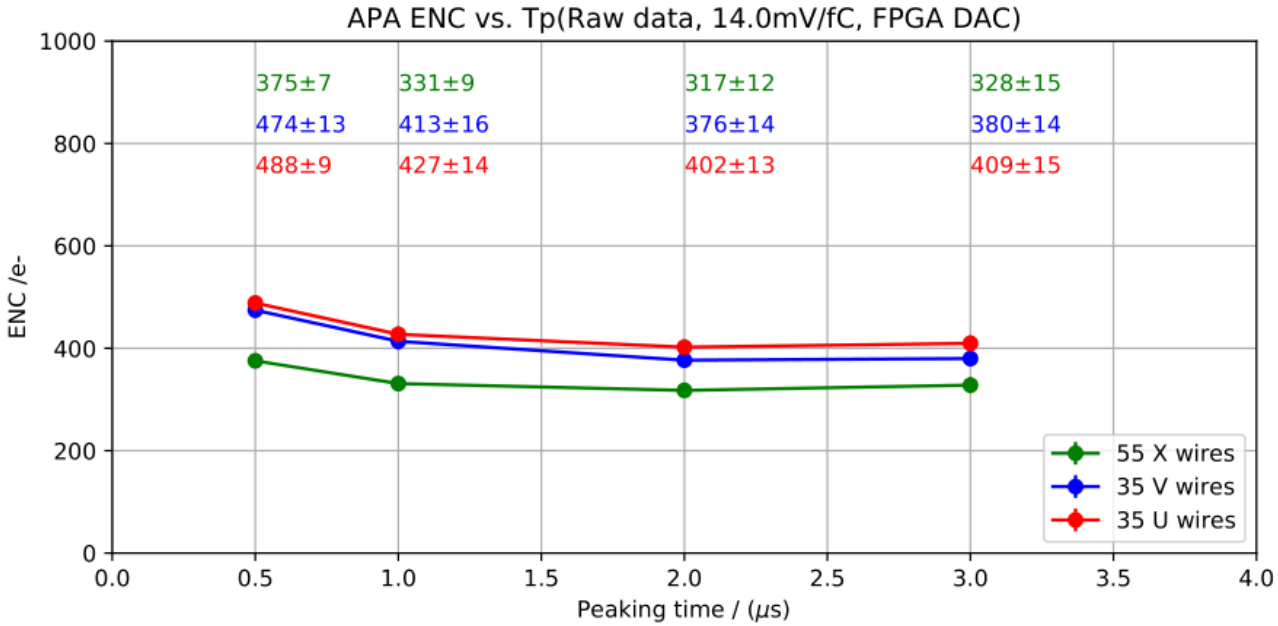
40% APA instrumented with SBND cold electronics components

CE + 40% APA fully submerged in LN2



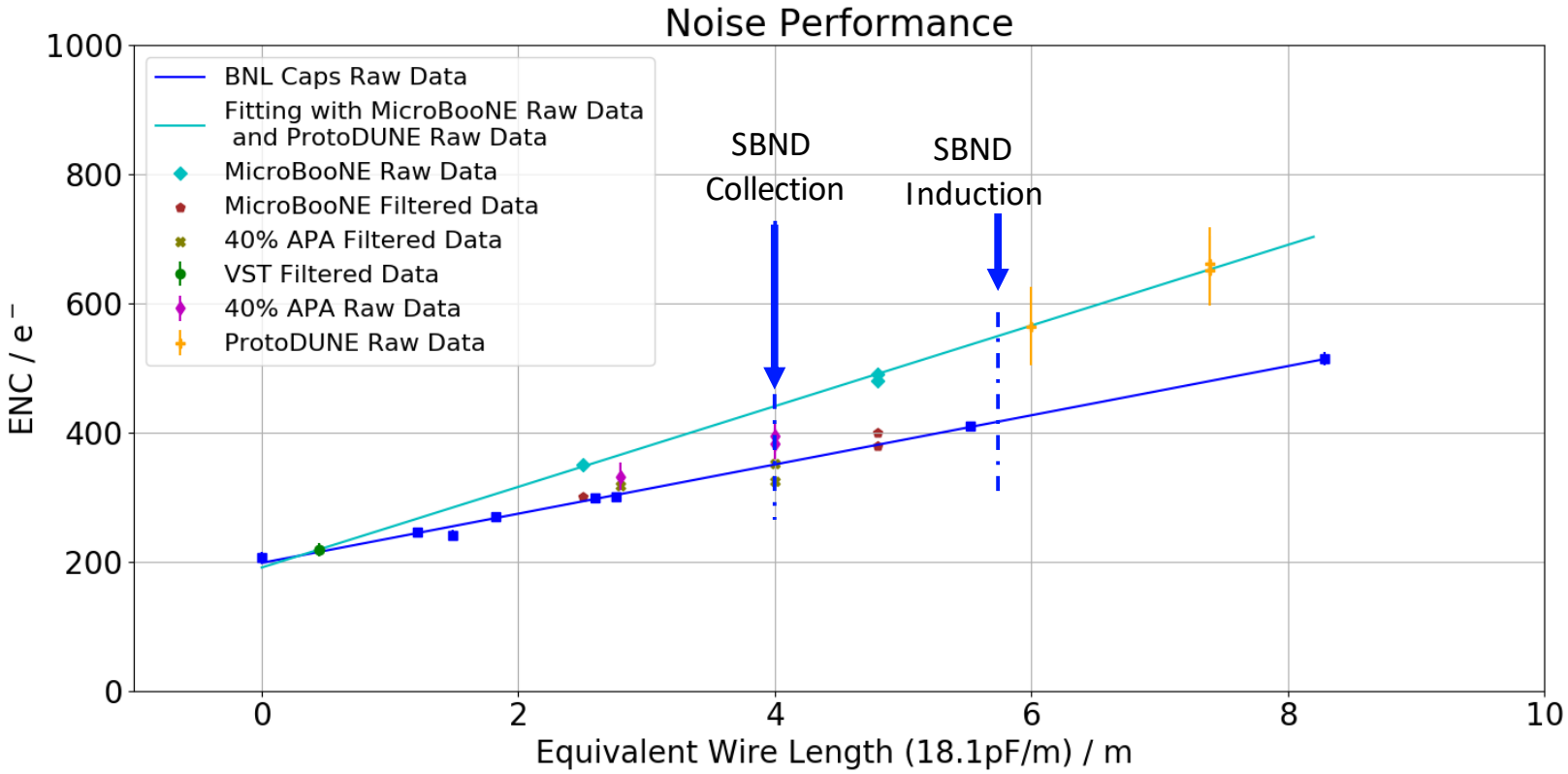
SBND Grounding and Isolation Rules

- SBND TPC uses extremely sensitive electronics to measure the charge from the TPC wires
- Principle
  - **The only electrical connection** between cryostat and detector common ground is through the signal feed-throughs
  - Avoid ground loop



40% APA and FEMBs Fully Submerged in LN2

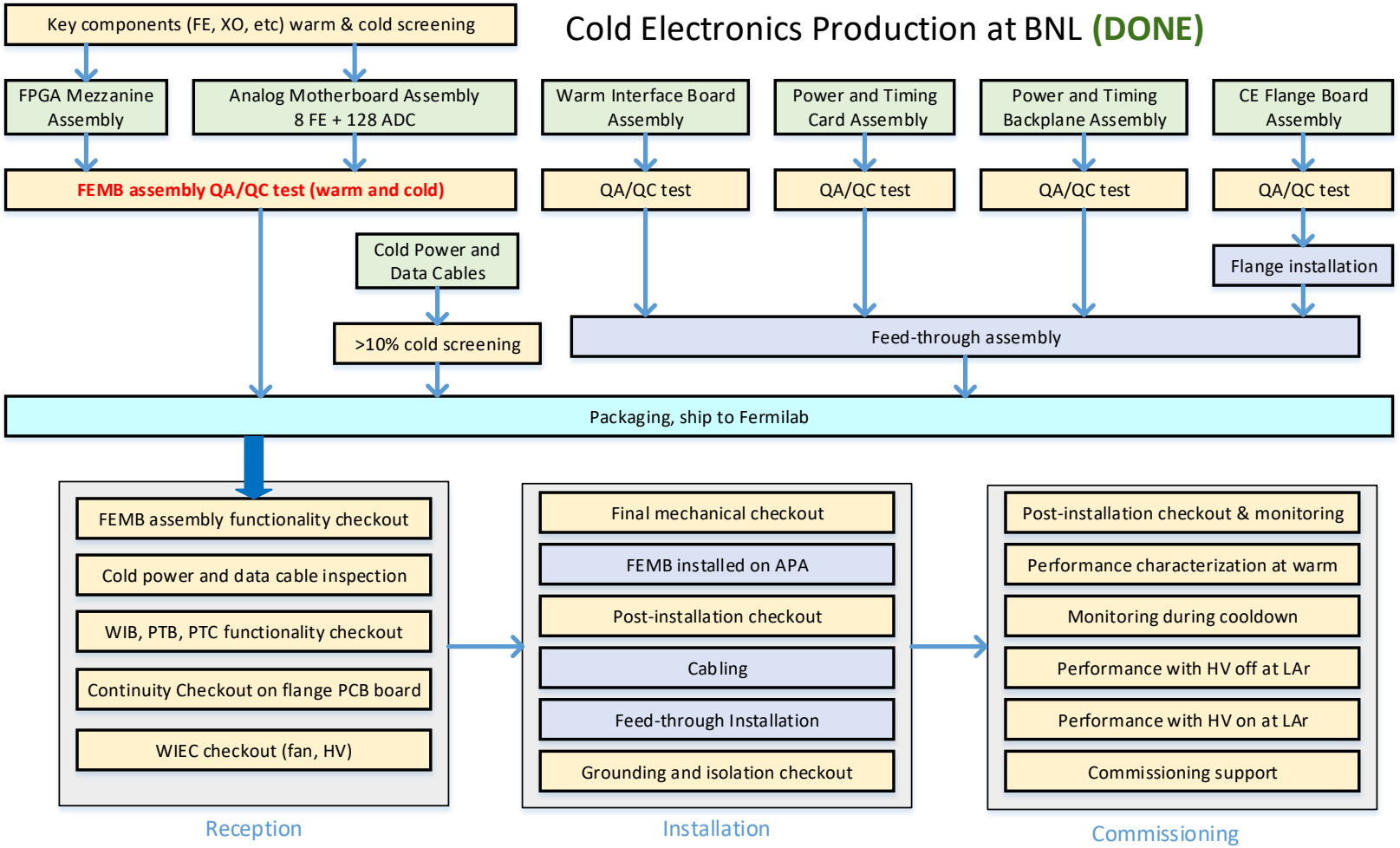
ENC Projection



1. Following correct grounding rules, both MicroBooNE and ProtoDUNE-SP have the required noise performance even before coherent noise filtering
2. Expected SBND noise performance **before offline filtering:**
   Induction plane (5.77m) < 600 e⁻, collection plane (4.0m) < 500 e⁻
3. Expected SBND noise performance after offline filtering and strictly followed grounding guidelines:
   Induction plane (5.77m) ~450 e⁻, collection plane (4.0m) ~350 e⁻

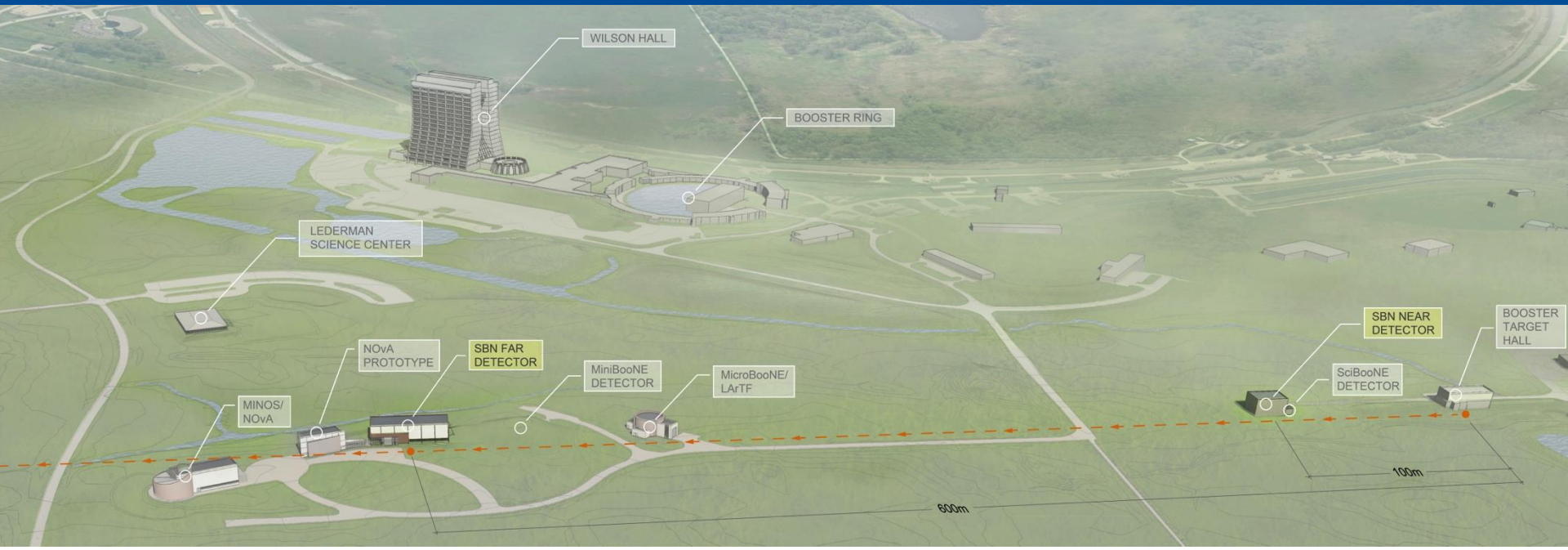
Production, Installation and Commissioning Procedure

B.Kirby's talk at 17:30: The ProtoDUNE-SP LArTPC Electronics Production, Commissioning and Performance



Summary

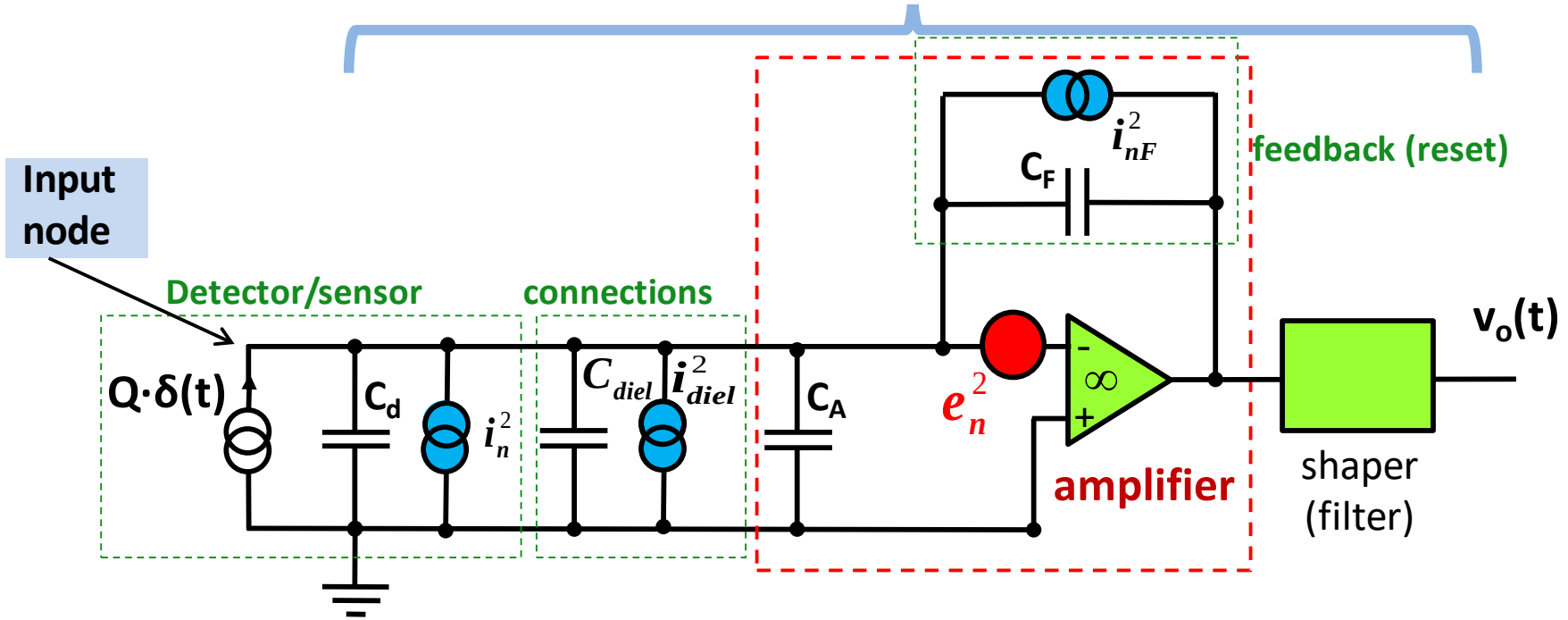
- Readout electronics developed for low temperatures (77K-89K) is an enabling technology for noble liquid detectors for neutrino experiments
  - Much lower noise and less cryostat penetrations
- SBND cold electronics development is progressing well
  - Benefit from ProtoDUNE-SP CE development
  - SBND collaboration has studied and made decision to use COTS ADC
  - An integral design concept of APA + CE + Feed-through, and Warm Interface Electronics with local diagnostics and strict isolation and grounding rules is crucial for the success of SBND experiment
    - Integration test of 40% APA at BNL shows satisfactory noise performance
    - **ENC projection shows cold electronics meets SBND requirement**
  - The QC plans, infrastructure, and experienced QC team are sufficient to deliver a high-quality, functional system
    - SBND CE production is completed as planed
    - Continuous effort for installation and commissioning


WILSON HALL
BOOSTER RING
LEDERMAN SCIENCE CENTER
NOvA PROTOTYPE
SBN FAR DETECTOR
MiniBooNE DETECTOR
MicroBooNE/ LArTF
MINOS/ NOvA
SBN NEAR DETECTOR
SciBooNE DETECTOR
BOOSTER TARGET HALL
100m
600m

Thank you!

Noise Sources in Detector-Amplifier

Overall system processing function: $h(t); w(t); H(j\omega)$



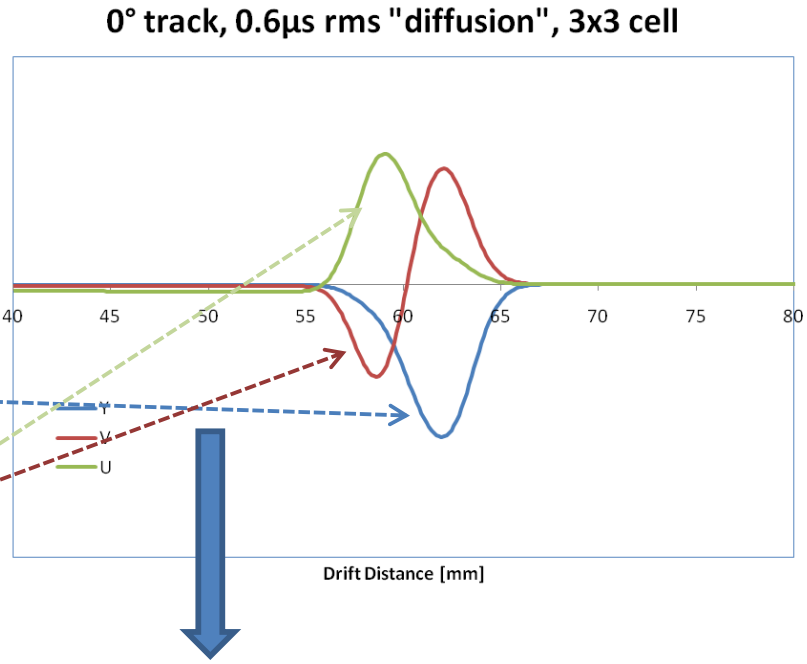
Dominant noise sources are from the components and circuits **directly connected to the input node**. Noise sources from the rest of the signal processing chain should be made negligible.

- i_n^2 arises in the sensor, e.g., from the leakage (dark) current; i_{nF}^2 may arise in feedback circuit
- i_{diel}^2 thermal fluctuations in dielectrics (dielectric loss noise)
- e_n^2 **noise associated with the input transistor:**
  MOSFET gain: "*series white noise*"
  trapping-detrapping: *1/f* eq. noise voltage generator in series

Signals in LAr TPC

- Charge signal
  - A 3mm MIP track should create 210keV/mm x 3mm /23.6eV/e = 4.3fC
  - After a 1/3 initial recombination loss: ~2.8fC
  - Assume the drift path to equal the charge life time, reducing the signal to 1/e≈0.368
  - The expected signal for 3mm wire spacing is then ≈1fC=6250 e, … and for 5mm, ≈10^4 e, for **the "collection signal"**
  - The induction signals are smaller
  - The time scale of TPC signals is determined by the **wire plane spacing** and **electron drift velocity**, (~1.5 mm/μs at 500 V/cm)

Induced Current Waveforms on 3 Sense Wire Planes



Sampling rate **≤ 2 Ms/s**

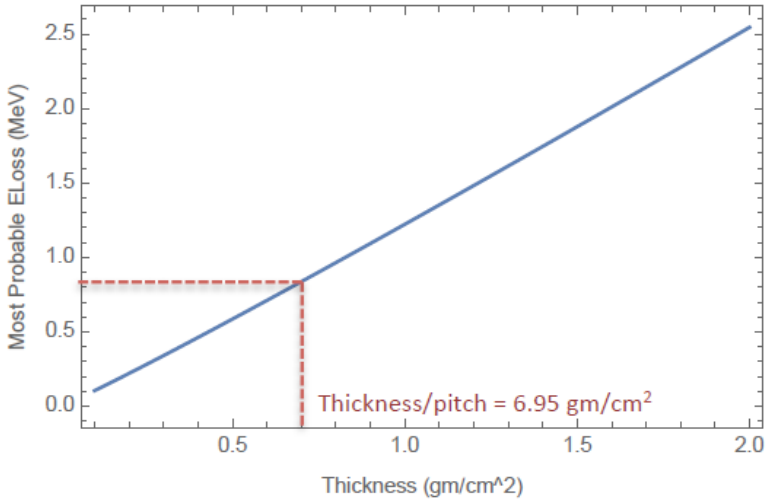
Signal to Noise

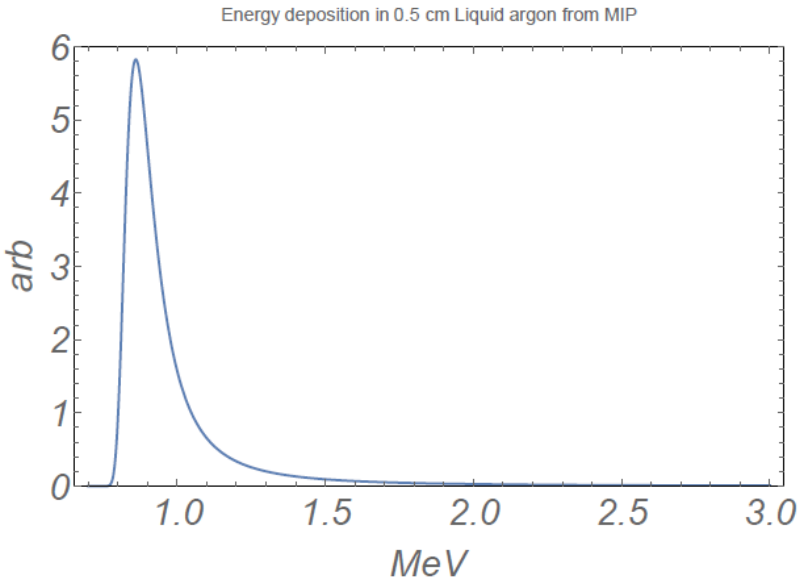
Total equivalent noise charge (ENC) shall be less than 1/9 of the expected worse case instantaneous charge arriving at the APA from a MIP.

- Driven by far detector S:N requirement to "distinguish a Minimum Ionizing Particle (MIP) track cleanly from electronic noise everywhere within the drift volume."
- Simple calculation of charge from a MIP track at the cathode parallel to the wire spacing:

$$\frac{E_{loss}\ (0.5\ cm)}{LAr\ E_{ee}} \times \text{Recombination (500 V/cm)} \times e^{-\frac{DL/velocity}{e^- \text{ lifetime}}} = \frac{0.83\ MeV}{23.6\ eV} \times 0.7 \times e^{-\frac{3.6m/1.6\ m/ms}{3\ ms}} = 11{,}629\ e^-$$

- Sets the collection wire noise parameter at ENC < 1300 e^-
- Equivalent charge on the induction wires is expected to be 0.5 x collection wire charge
- Induction wire noise parameter ENC < 650 e^-





Dynamic Range

The requirement to measure a MIP-size charge from the cathode with a precision of 1% in the collection plane determines the lower end of the dynamic range. The need to collect charge deposited at the vertex of a neutrino event (mainly by protons) without suffering satura0on sets the upper end.

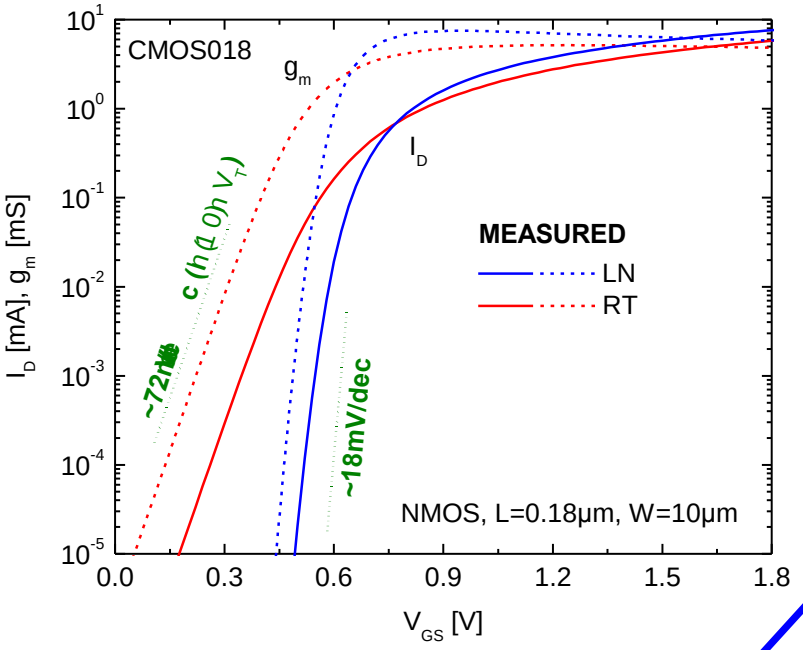
- Lower end calculation
  - To obtain 1% charge resolution requires 1% of 11.6k e^-: ~116 e^- per ADC count
- Upper end calculation
  - Proton energy distribution is isotropic in the range 10-100 MeV
  - Worst case assumption: all energy deposited in one 0.5cm voxel
  - Proton at wire plane: no drift losses, instantaneous deposition

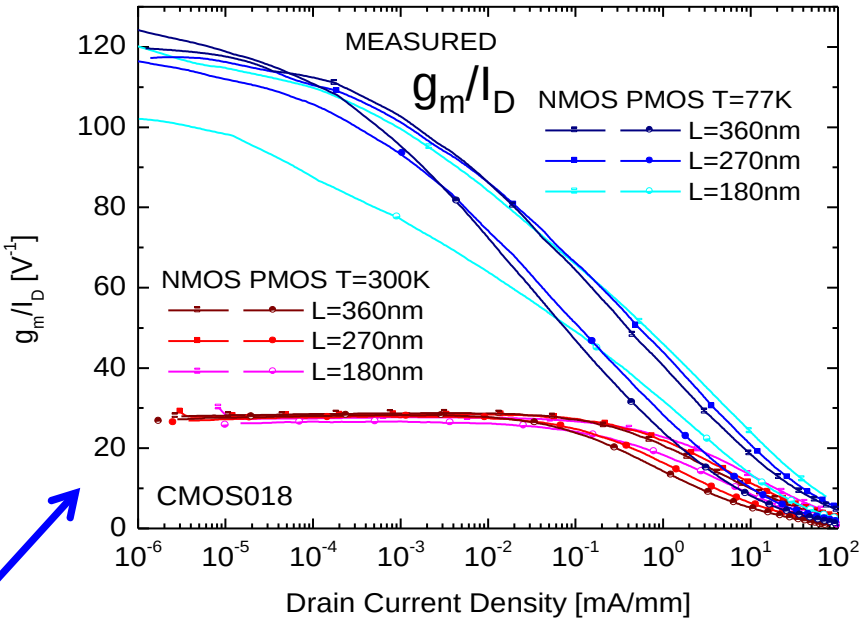
$$\frac{E_{loss}\ (0.5\ cm)}{LAr\ E_{ee}} \times \underset{(500\ V/cm)}{Recombination} = \frac{21\ MeV}{23.6\ eV} \times 0.25 = 222.5k\ e^-$$

  - For CC ν_e - Ar interactions assume a mean of 2 protons/vertex
  - 445k e^- maximum charge ÷ 116 e^- /count = 3,836 counts

12-bit ADC is sufficient for digitization

CMOS Characteristics in LAr





Transconductance/ drain current

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \ \ at \ \ T = 300K \\ \sim 116 \ \ at \ \ T = 77K \end{cases}$$

At 77-89K, charge carrier ***mobility*** in silicon *increases* and ***thermal fluctuations*** *decrease* with ***kT/e***, resulting in a ***higher gain***, ***higher*** g_m/I_D, ***higher speed*** and ***lower noise***.

- In parallel, studies of ***CMOS lifetime and reliability*** at 77 K have been conducted
  - *"LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Trans. on NSci, 60, No: 6, Part: 2, p4737(2013)*

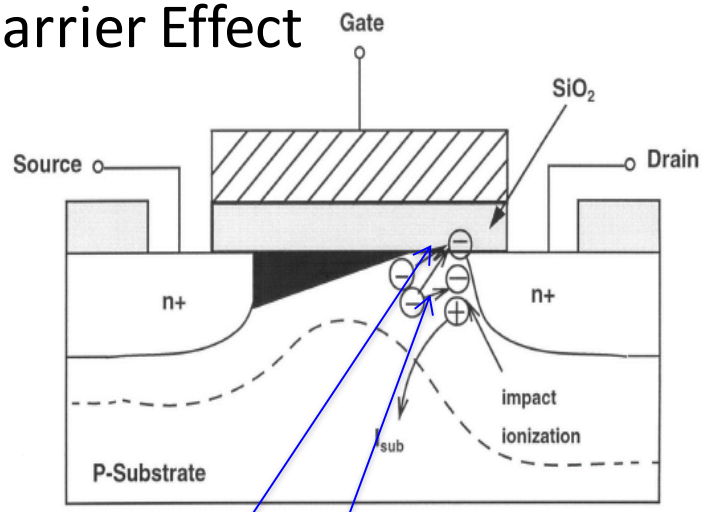
CMOS Lifetime Study – Principle Findings

- A study of hot-electron effects on the device lifetime has been performed for the TSMC NMOS 180nm technology node at 300K and 77K. Two different measurements were used: accelerated lifetime measurement under severe electric field stress by the drain-source voltage (V_{ds}), and a separate measurement of the substrate current (I_{sub}) as a function of $1/V_{ds}$. The former verifies the canonical very steep slope of the inverse relation between the lifetime and the substrate current, $\tau \propto I_{sub}^{-3}$, and the latter confirms that below a certain value of V_{ds} *a lifetime margin of several orders of magnitude can be achieved for the cold electronics TPC readout. The low power ASIC design for MicroBooNE and DUNE falls naturally into this domain, where hot-electron effects are negligible.*

- The slope of lifetime vs $1/V_{ds}$ is independent of the technology node (from 180, 130 to 65 nm) and of the foundry (TSMC, Global ...). For all three nodes the lifetime is extended by an order of magnitude if V_{dd} (V_{ds}) is reduced by **~6%**. This may be related also to the two basic underlying parameters, *electron energy* for *impact ionization* and for *creation of an interface state*, as well as *their ratio.*

Basic on HCE and ALT

Hot Carrier Effect



→Some hot electronics exceed the energy required to create an electron-hole pair, resulting in ***impact ionization***

→ A very small fraction of hot electrons exceeds the energy required to create an ***interface state*** at the Si-SiO2 interface

→ Due to the generation of interface states, negative charges will accumulate causing the degradation

→ More severe at cold than at RT

Accelerated Lifetime Test

CMOS in DC operation

→ ALT at any temperature (well-established by foundries) transistor is placed under a severe electric field stress (large V_{DS}), to reduce the lifetime due to hot-electron degradation to a practically observable range.

→ ALT is widely used by industry

→ Lifetime is projected by empirical equation $log_{10}\tau \propto 1/V_{ds}$

CMOS in AC operation

→ Lifetime of digital circuits (ac operation) is extended by the inverse duty factor $4/(f_{clock}*t_{rise})$ compared to dc operation. This factor is large (>100) for deep submicron technology and clock frequency needed for TPC

Basics on Hot-electron effects (HEC) and NMOS lifetime

- In deep submicron NMOS (L<0.25μm) electrons can become "hot" at any temperature, by attaining energy $E > kT$.

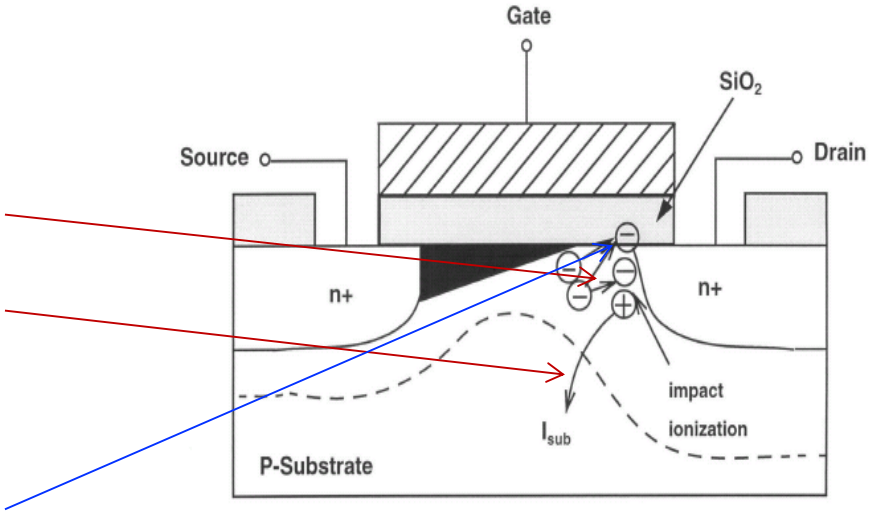
- Some hot electrons exceed the energy required to create an electron-hole pair, $\varphi_i \cong 1.3eV$ resulting in *impact ionization*. Electrons proceed to the drain. The *holes* drift to the substrate. The ***substrate current***,

$$I_{sub} = C_1 I_{ds} e^{-\varphi_i / q\lambda E_m} \qquad (1)$$

- A very small fraction of hot electrons exceeds the energy required to create an ***interface state*** (e.g., an acceptor-like trap), in the Si-SiO_2 interface, $\varphi_{it} \geq 3.7eV$ for electrons (~4.6eV for holes). This causes a change in the transistor characteristics (transconductance, threshold, intrinsic gain).

- The time required to change any important parameter (the changes in different parameters are correlated) by a specified amount (e.g., g_m by ~10%) is defined as the ***device lifetime***. It can be calculated as,

$$\tau = C_2 \frac{W}{I_{ds}} e^{\varphi_{it} / q\lambda E_m} \qquad (2)$$



q = electron charge

$\boldsymbol{\lambda}$ = electron mean free path

E_m = *electric field*

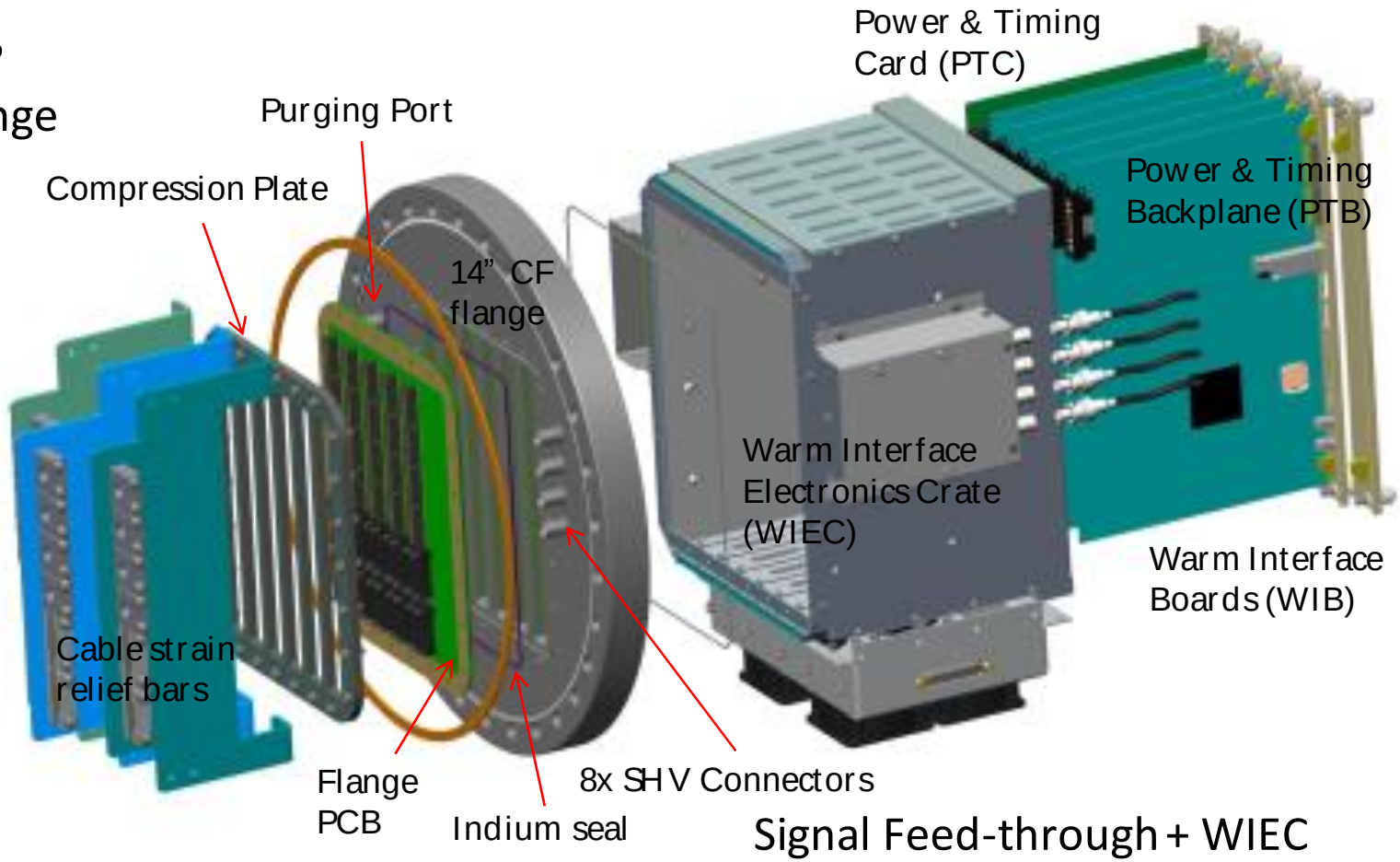
I_{ds}= drain-source current

W= channel width

C_1, C_2 - constants

Warm Interface Electronics

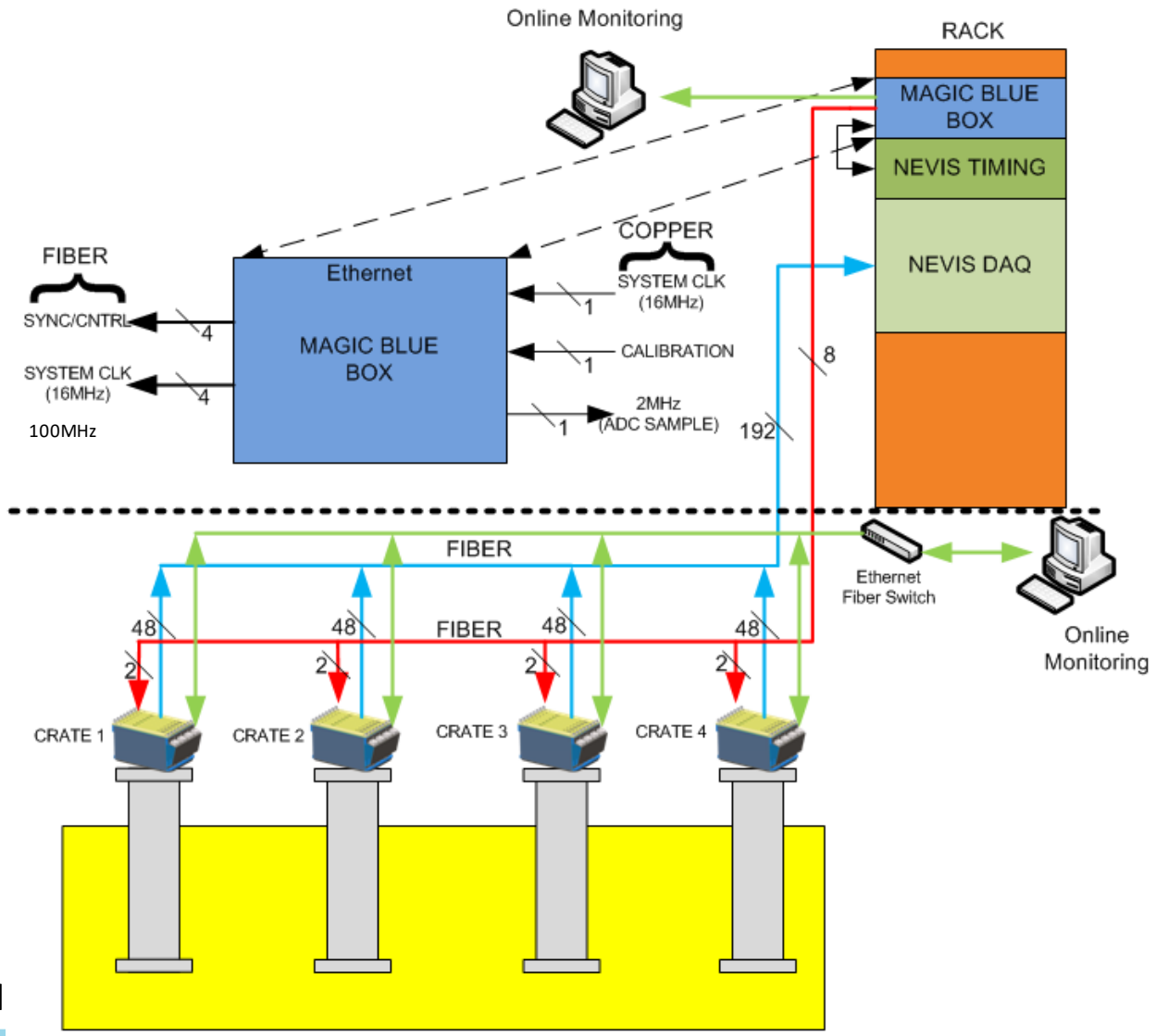
- 6x SBND Warm Interface Boards (WIB)
- 1x SBND PTC
- 1x PTB
- 1x Flange



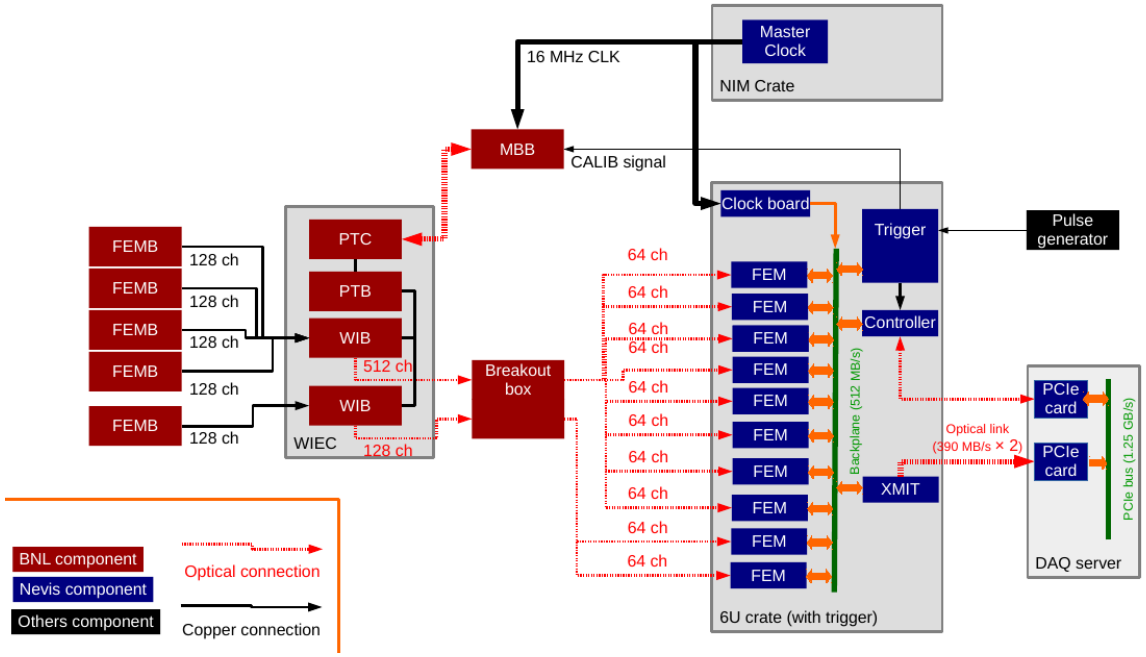
Signal Feed-through + WIEC

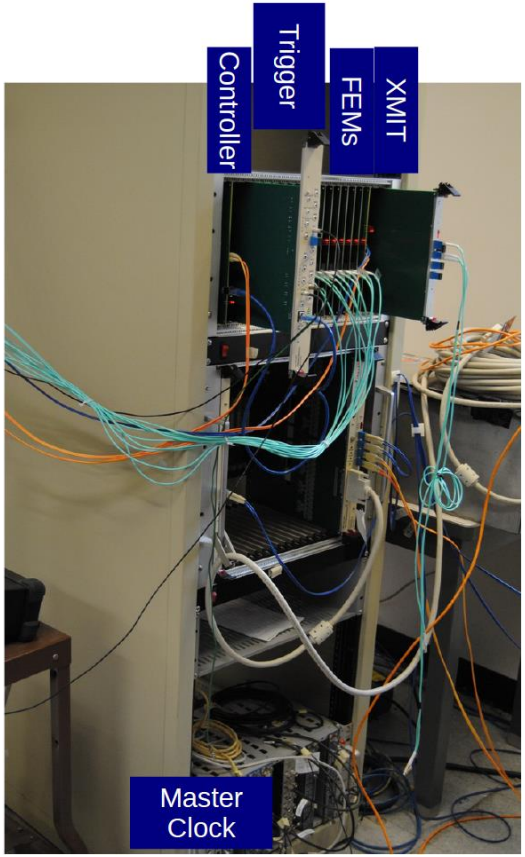
SBND TPC Data, Clock & Calibration Signals

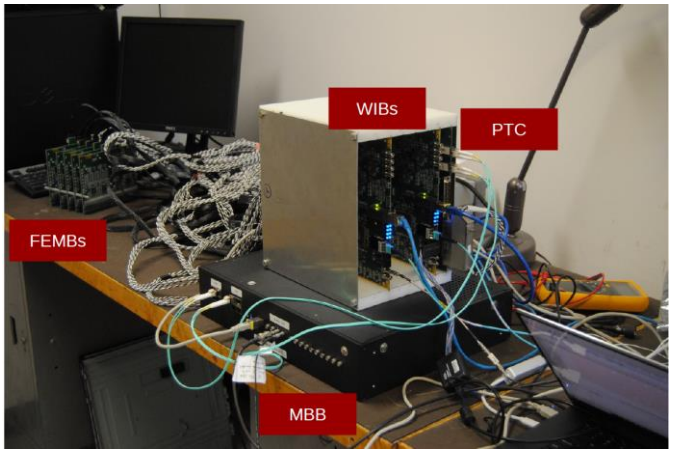
- DAQ
  - WIB → Nevis DAQ RACK
    - 192 Fibers
- System Clock
  - Nevis timing to MBB
    - Copper
  - $MBB_{(DAQ\,RACK)}$ → PTC
    - Four Fibers
- Sync/Cntrl
  - $MBB_{(DAQ\,RACK)}$ → PTC
    - Four fibers
- GbE Ethernet
  - To online monitoring
  - Six per WEC 24 total
    - WIB ←→ switch
    - Fiber
  - One MBB
    - Fiber or copper
- Calibration
  - Nevis timing to MBB
    - Copper
  - MBB (DAQ RACK) → PTC
    - Encoded on Sync/Cmd



BNL-Nevis Integration Test







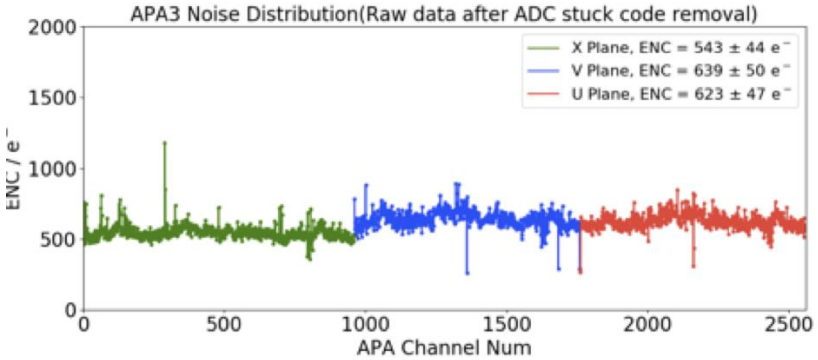
Successful joint BNL-Nevis integration test

- Full readout chain from FEMBs to Nevis FEMs established
- Successful trigger readout stream data acquisition with artdaq
- Successful clock distribution from Nevis Clock Fanout (NIM) to BNL's MBB and subsequent distribution to WIBs

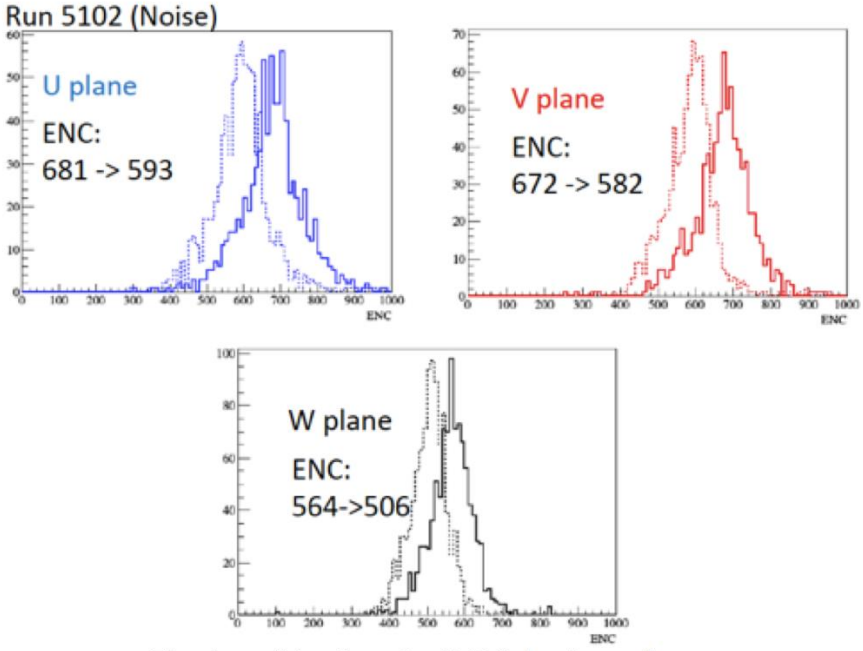
ProtoDUNE-SP

Cold Electronics Performance

- 99.74% (15320 of 15360) TPC channels are active
  - → 31 are missing or disconnected wire candidates
  - → 3 channels are missing in several runs
  - → just 6 inactive cold electronics channels in 9 months of operation
- 92.83% (14259 of 15360) TPC channels are working with excellent noise performance (ENC < 800 e^-)
  - → the abnormally high RMS of the remaining 7% is probably due to the TPC instrumentation
  - → more detailed noise performance study is now ongoing

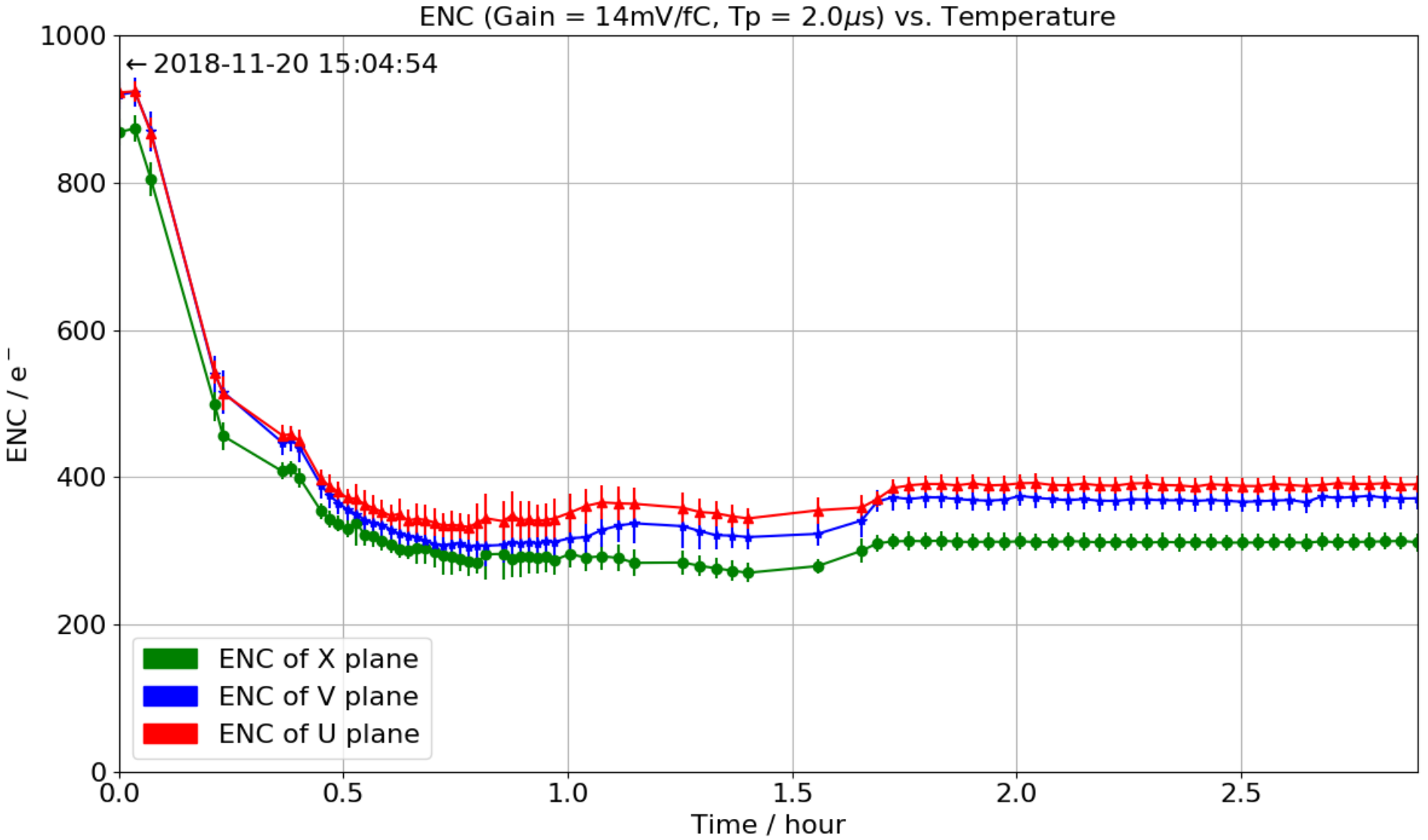


Thanks to Shanshan Gao @ BNL for this plot



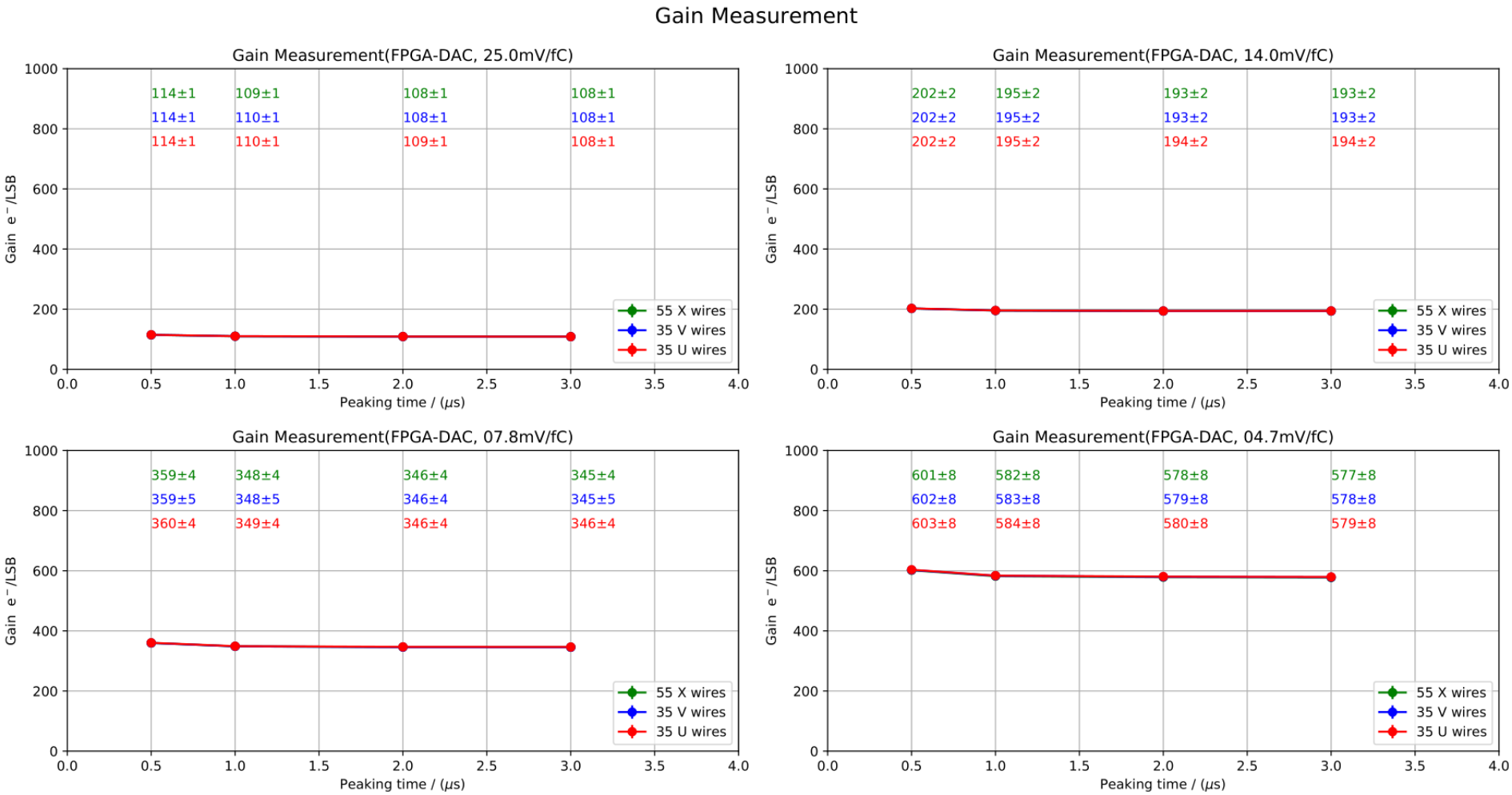
Thanks to Wenqiang Gu @ BNL for these plots

40% APA Cooldown



40% APA and FEMBs Fully Submerged in LN2

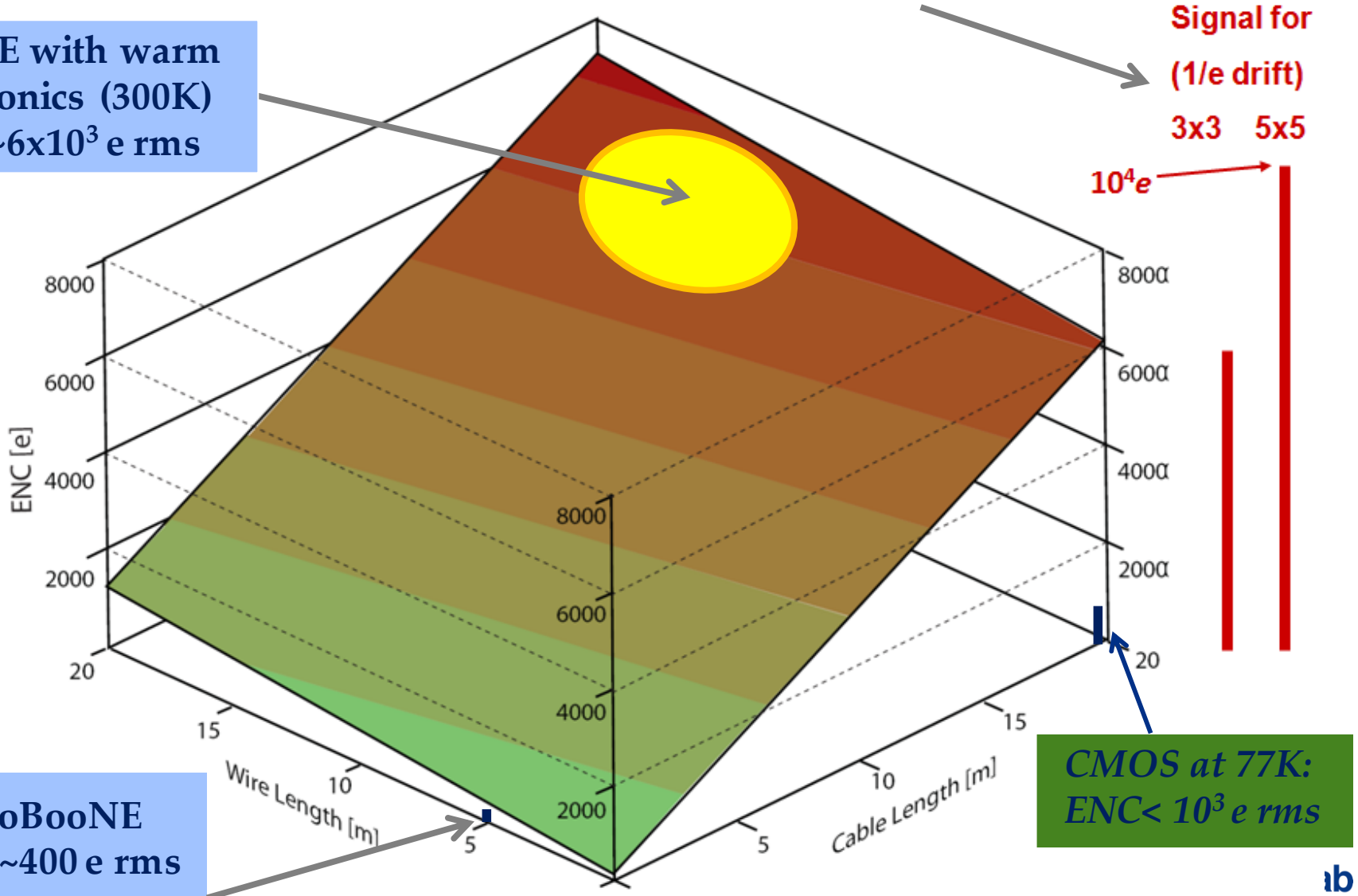
- FEMB2 (SBND-Production Side FEMB) – **Gain Measurement**



Noise (ENC) *vs* TPC Sense Wire and Signal Cable Length for CMOS at 300K and 89K

MIP Signal for 3x3 and 5x5 mm Sense Wire Spacing

DUNE with warm electronics (300K) ENC~6x10^3 e rms



MicroBooNE ENC~400 e rms

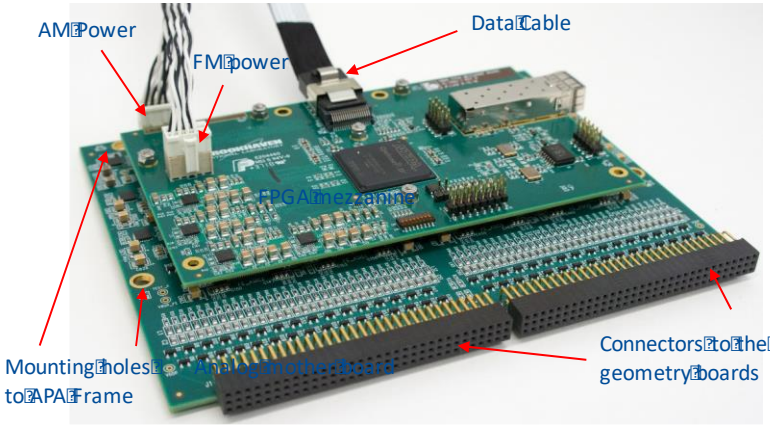
CMOS at 77K: ENC< 10^3 e rms

32

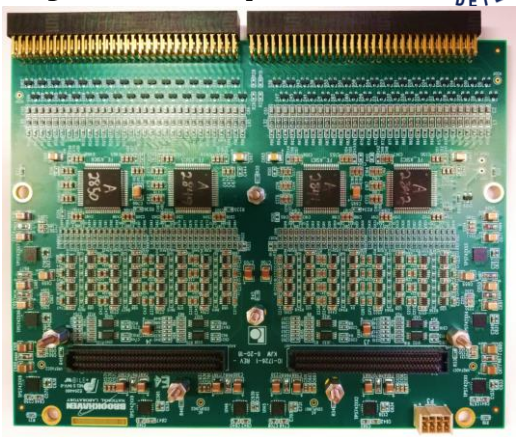
BNL Front End Electronics (Inside the Cryostat)

8m Samtec Power Cable

8m Mini-SAS data cable with isolation wrap



128CH FEMB Assembly

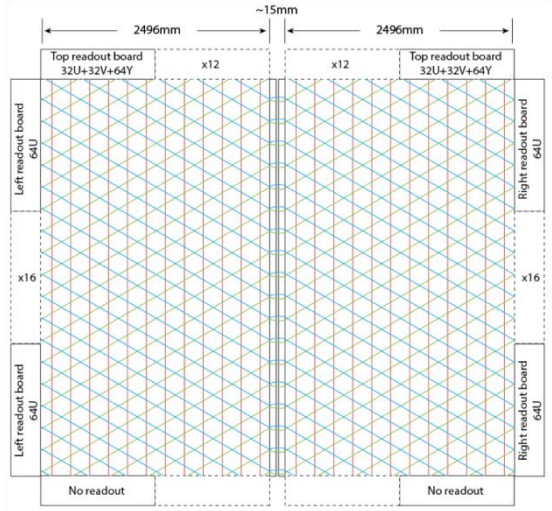


Top AM

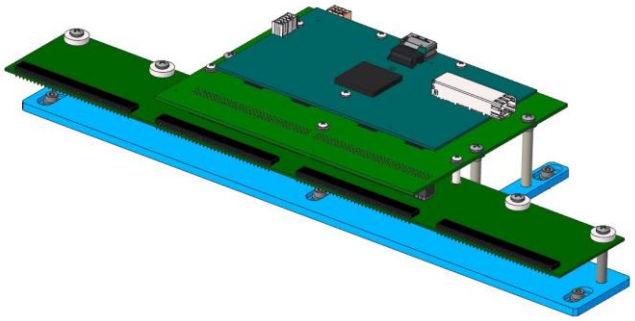
26X Top FEMBs

Side AM

9X Side FEMBs



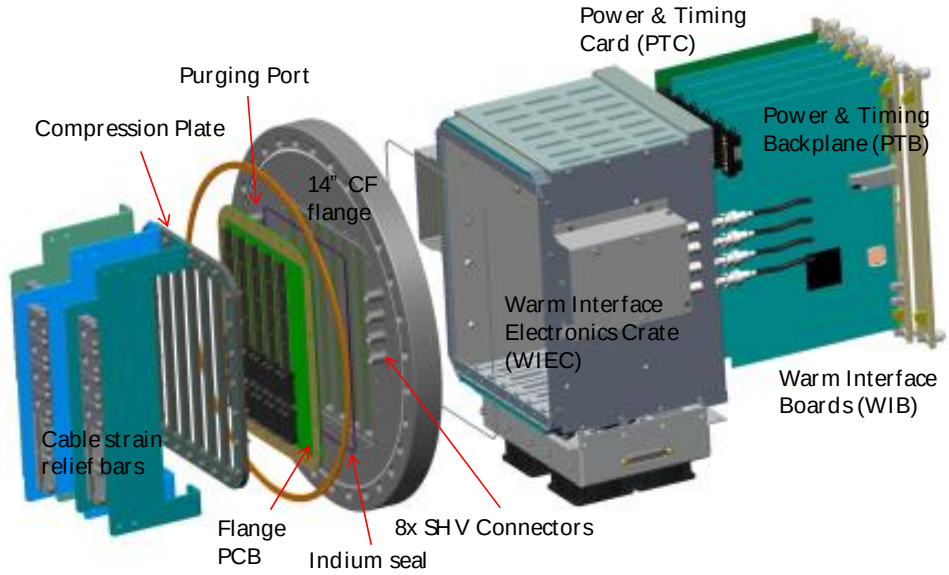
9X Side FEMBs

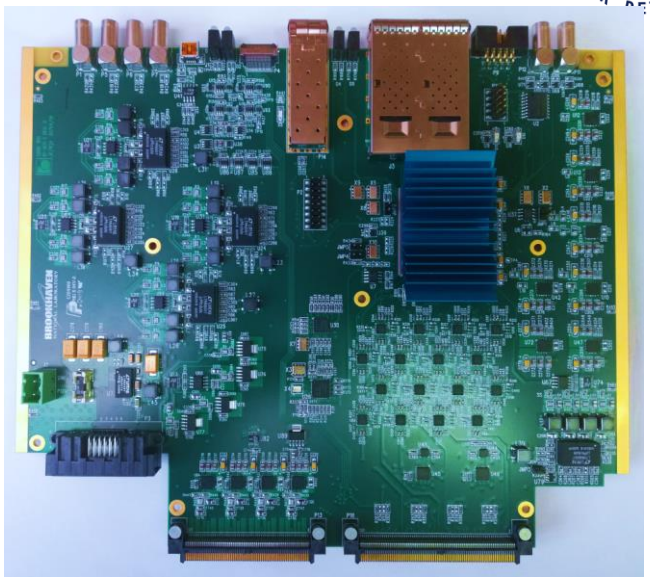


Side FEMB Adapter Board

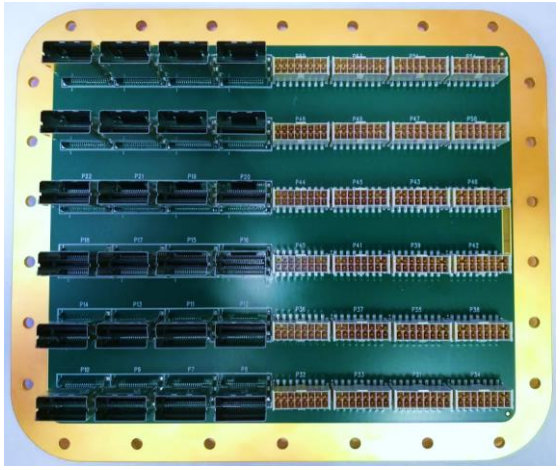
2X APAs

BNL Front End Electronics (Feedthrough)

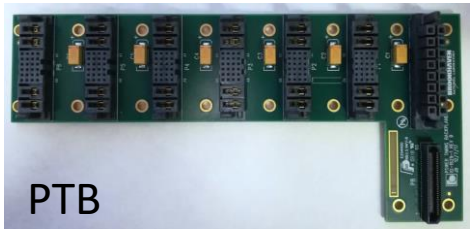




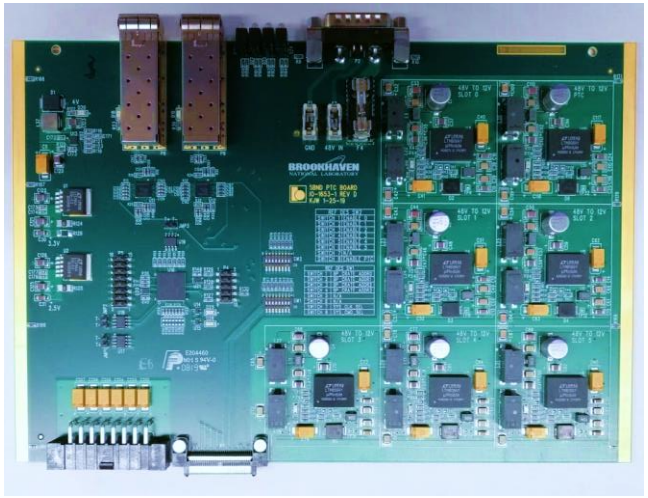
WIB with Dual-QSFP



Flange

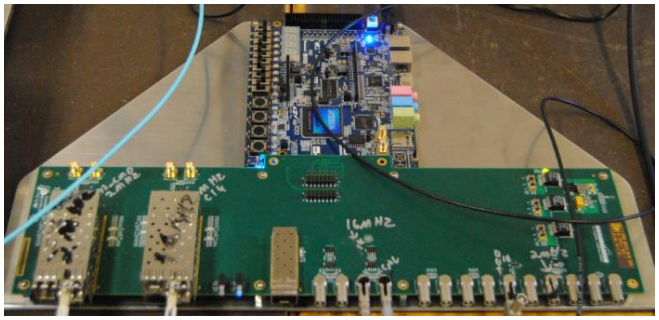


PTB



PTC

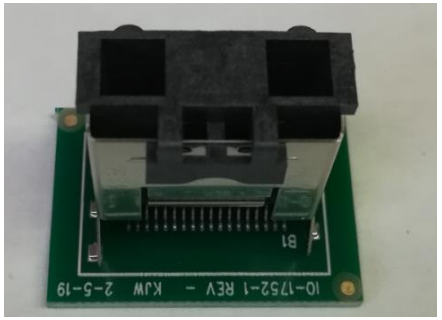
BNL Front End Electronics (MBB and Accessories)



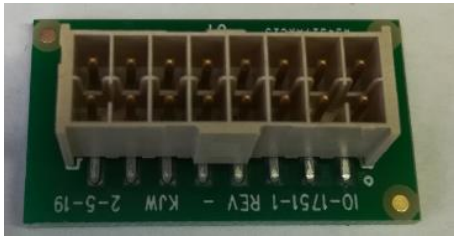
MBB (Magic Blue Box) for timing

MBB is placed in DAQ rack

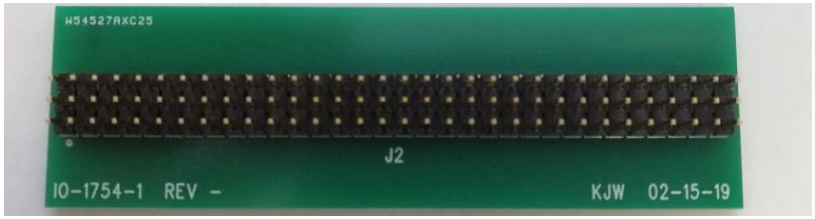
Accessories assure QA during CE installation



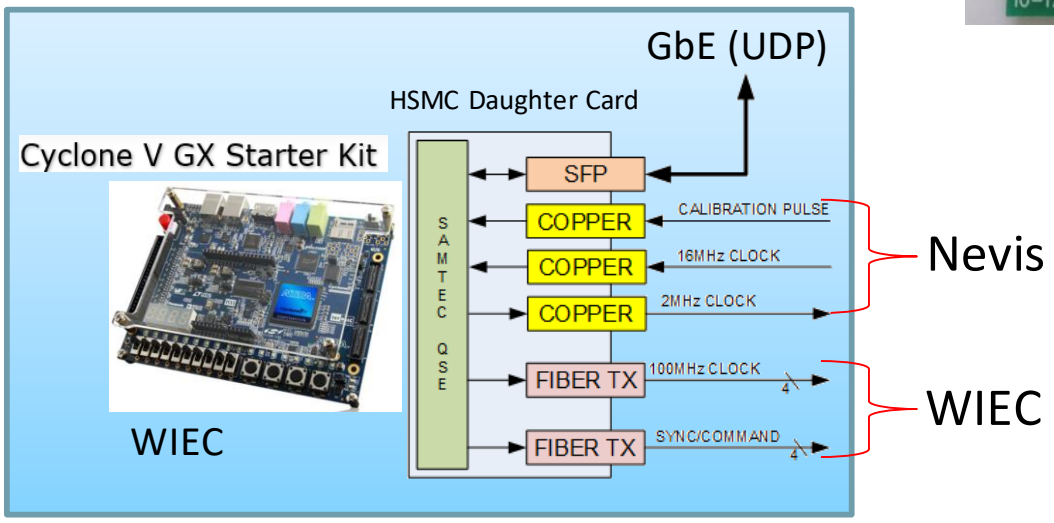
Data Cable Short Board

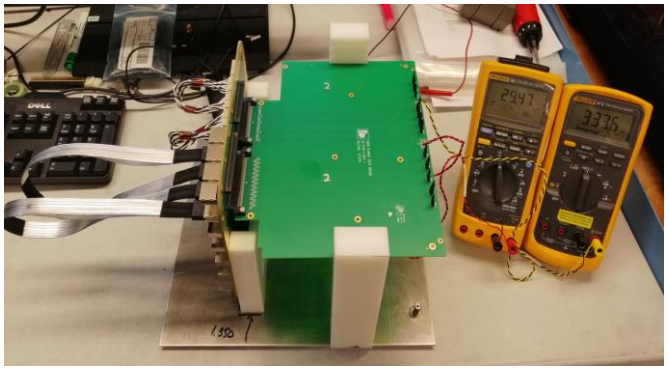


Power Cable Short Board



FE input short board





Flange daisy-chain test board

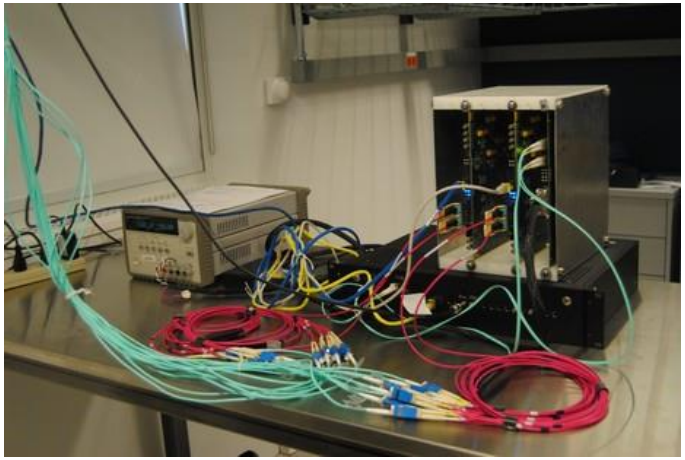
Test Stands for CE Production QA/QC

FEMB QC

3 MSU CTS for FE and FEMB cold screening

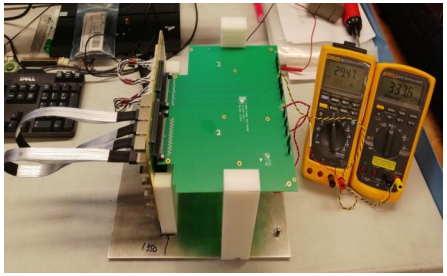
Quad-Socket FE test board

XO and Flash cold screening



Nevis-BNL Integration Test Stand
(Support Back-End Electronics QA/QC)

WIB, PTC, and PTB
Joint Test Stand



Flange Daisy-chain Test Stand