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Low Noise Front-End Cold Electronics System R&D for SBND LAr TPC

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The Short Baseline Near Detector (SBND) is one of three liquid argon (LAr) neutrino detectors sitting in the Booster Neutrino Beam (BNB) at Fermilab as part of the Short Baseline Neutrino (SBN) program. The detector is in a cryostat holding 260-ton of LAr and consists of four 2.5 m (L) × 4 m (W) Anode Plane Assembles (APAs) and two Cathode Plane Assemblies (CPAs), which leads to 11,264 Time Projection Chamber (TPC) readout channels and two separate 2 m long drift regions. As an enabling technology, Cold Electronics (CE) developed for cryogenic temperature operation makes possible an optimum balance among various design and performance requirements for such large sized detectors. There are two main advantages of CE. First, large detectors used for neutrino experiments require very low noise performance to meet their physics goals. CE decouples the electrode and cryostat design from the readout design. With the integration of electronics and detector electrodes, the capacitance of the input signal path is negligible, which results in the noise being independent of the fiducial volume. Meanwhile, the noise of the CMOS front end (FE) ASIC significantly decreases at cold temperature, benefiting from increased charge carrier mobility in silicon and decreased thermal fluctuations in accordance with kT/e. Second, signal digitization and multiplexing to high speed links inside the cryostat result in a large reduction in the quantity of cables (less outgassing) and number of feed-through penetrations, giving the designers of both the TPC and the cryostat the freedom to optimize the detector configurations.
Brookhaven National Laboratory (BNL) has been leading the R&D and implementation of the entire front-end CE system for LAr TPC readout in collaboration with other SBND institutes. The front-end readout electronics system will be presented. This includes the cold front-end electronics placed close to the wire electrodes, which detects and digitizes the charge signal in LAr, as well as the warm interface electronics placed on the signal feed-through flange outside of the cryostat, which further organizes and transmits the digitized signal to the DAQ system. An extensive study of electronics suitable for 77K – 300K, including the custom designed front-end ASIC and commercial components, e.g. ADC and FPGA, has been made to meet requirements such as low noise, low power consumption, high reliability and long lifetime. Furthermore, an integral design concept of APA, CE, feed-through, warm interface electronics with local diagnostics, grounding and isolation rules has been practiced with vertical slice test stands to project the CE performance in the SBND detector. A detailed QA/QC procedure has been developed and is currently being carried out for CE production, which is ongoing to support successful installation and commissioning of the SBND TPC readout electronics system in coming months.

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