Development and Testing of the ATLAS ITk HCCStar ASIC

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Penn
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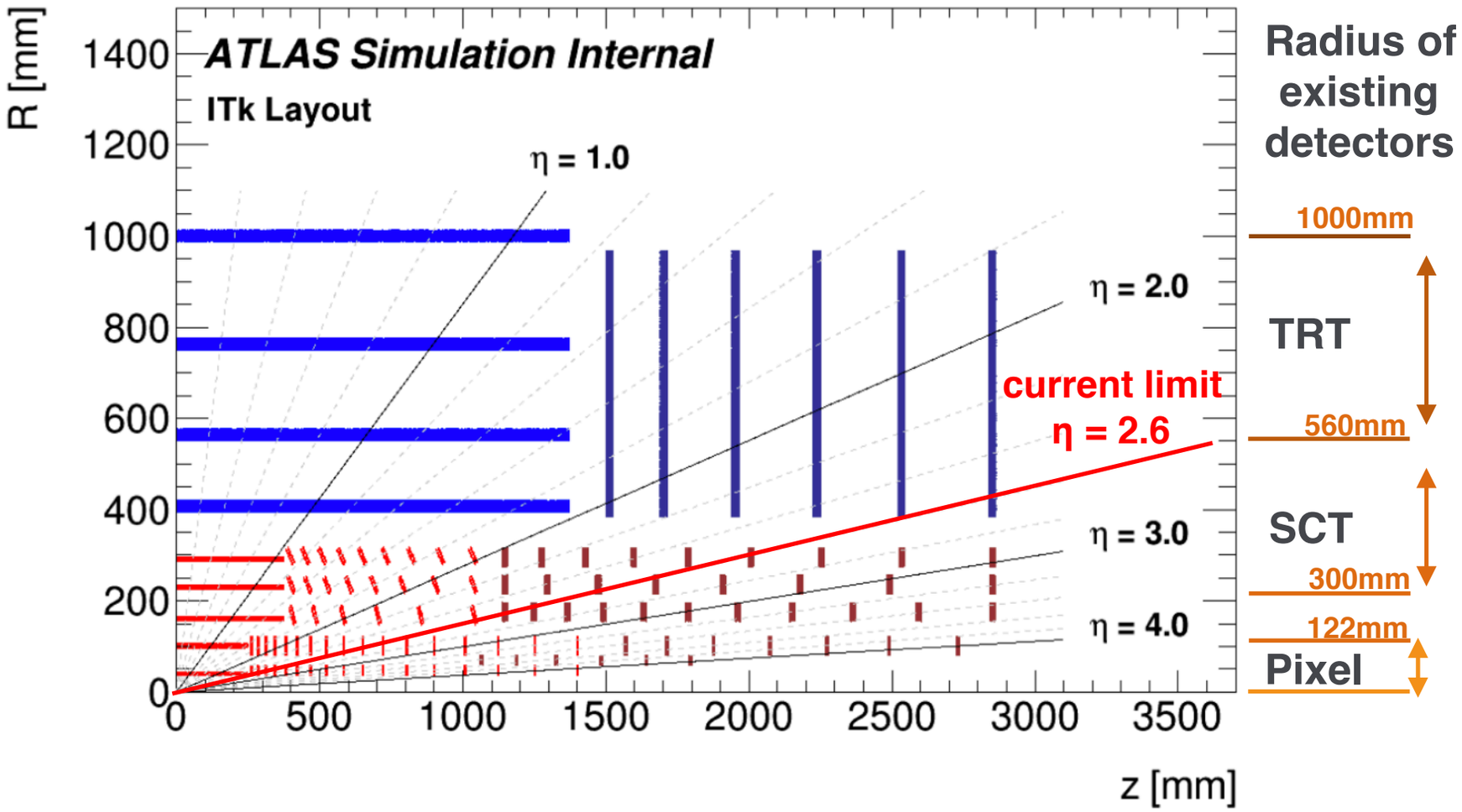
ATLAS EXPERIMENT

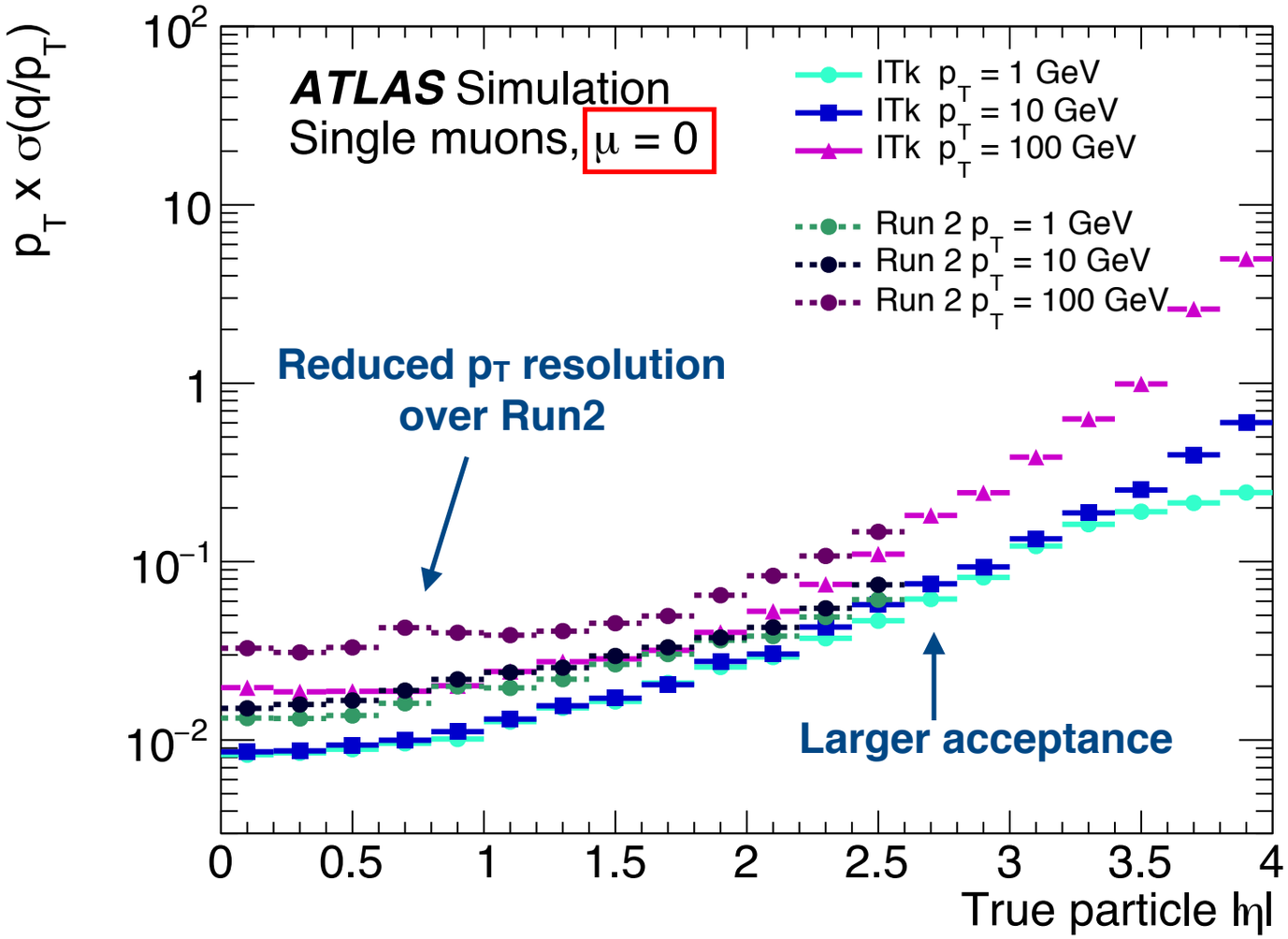
ATLAS Inner Tracker for HL-LHC

- ITk is the replacement Inner Detector for ATLAS during HL-LHC (beginning in 2026)
  - Must operate over **10 years**, collecting **4000 fb^{-1}** of data from **~200 collisions** per bunch crossing
- **Radiation Tolerant:** Pixel / Strips subject to **1000 / 50 MRad** (10x increase)
- Improved performance:
  - **All-silicon detectors**, increased active area (from 61m^2 to 165 m^2)
  - **Larger radius**
  - **Finer segmentation**
  - Track coverage increased to **η = 4**
  - Reduced material footprint



Inner Tracker for HL-LHC

All these detector improvements lead to better tracking efficiency & momentum resolution

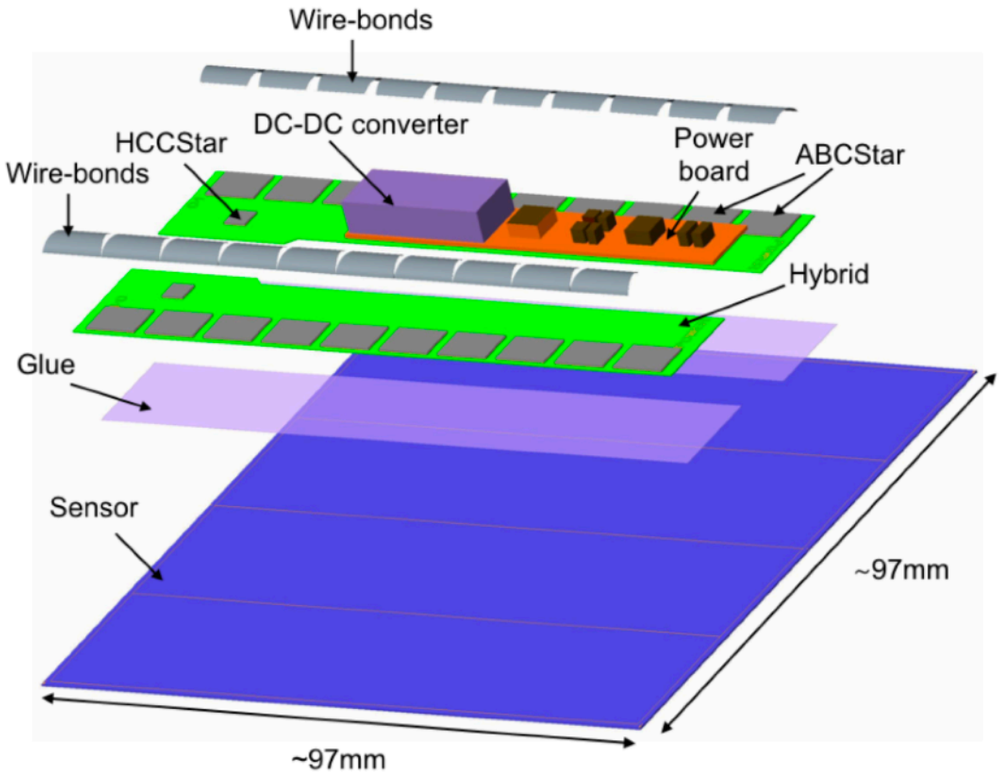


- Big gains for **tracking at trigger-level**
  - Operation can be either a **single level trigger** (L0 @ 1MHz) or **a two level trigger** (L0 @ 4MHz, L1 @ 600 kHz)
  - **Regional readout request** after L0 for ROI tracking discrimination in L1 (R3 @ 400 kHz)

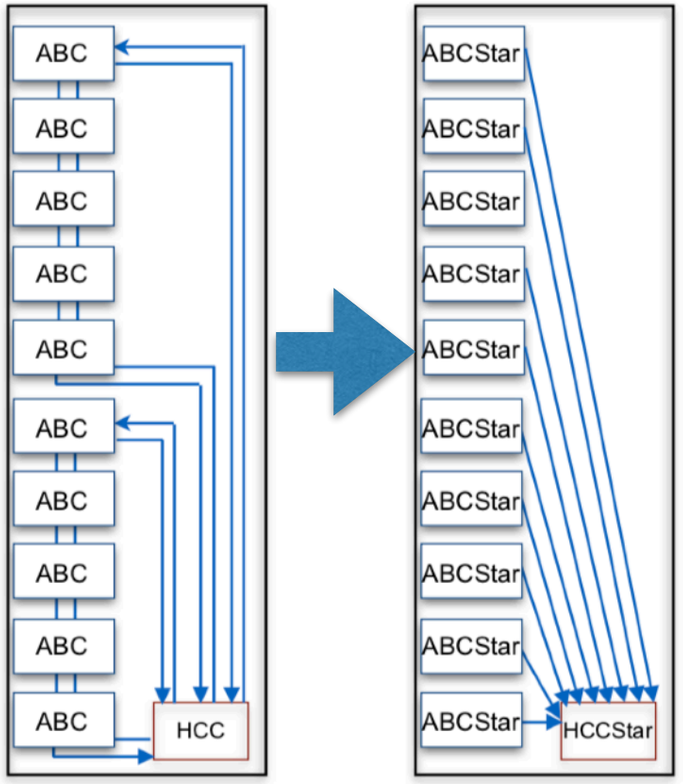
ITk Strip ASICs

- Sheet of **silicon sensor** segmented into long strips
- **ABCStar** (ATLAS Binary Chip) **glued to 256 sensors, digitize** & **compress data** into clusters
- **HCCStar** (Hybrid Controller Chip) **serializes data** of up to 11 ABCStars, **transmits commands**, **buffers triggers**
- **AMAC** (Autonomous Monitoring And Control) - **monitors** voltage/current/temperatures, **system interrupts**
- **New Star design** w/ point-to-point communication, accommodating 2x increase to trigger rate

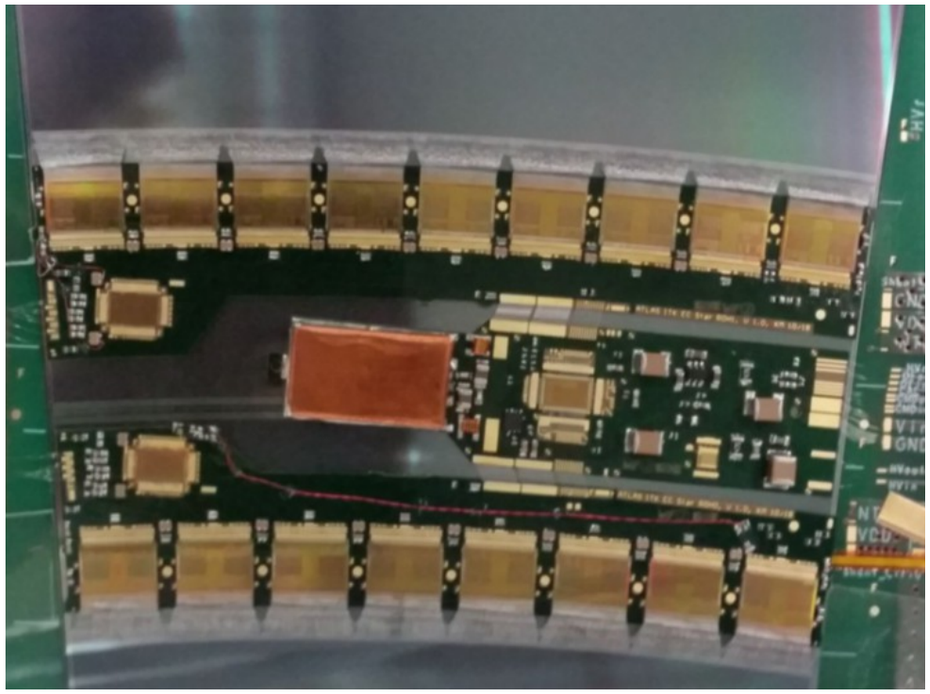
Exploded view of a module's components



Daisy-chain design

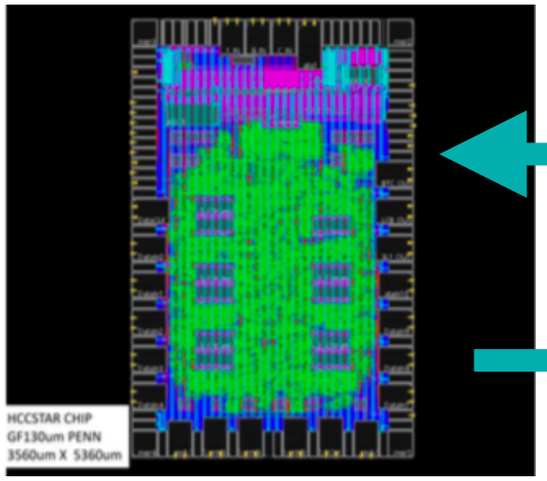


Star chip design



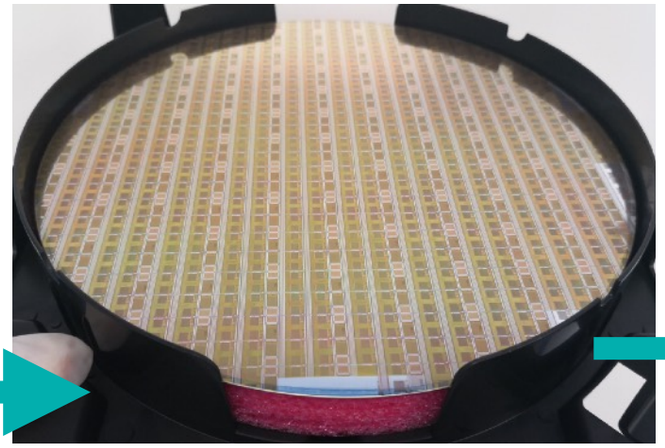
Development Cycle

CAD Design

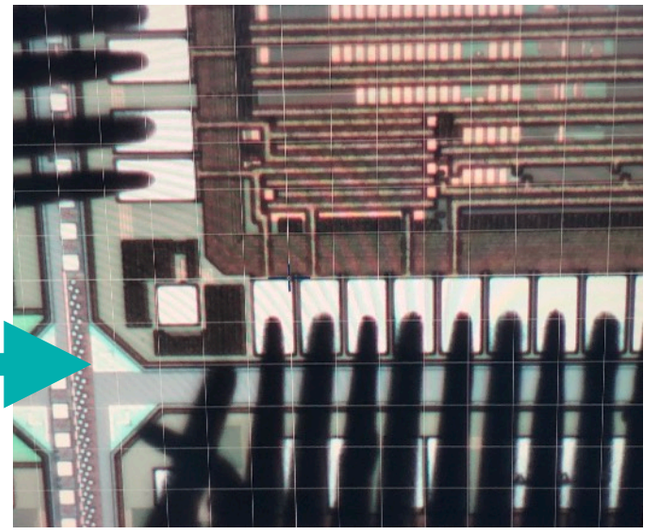


Simulation

Vendor Fabrication

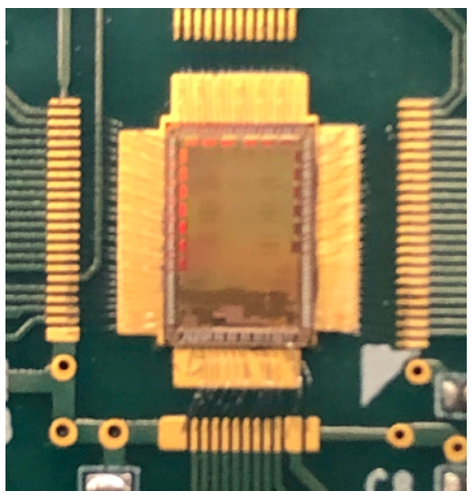


Wafer Probing



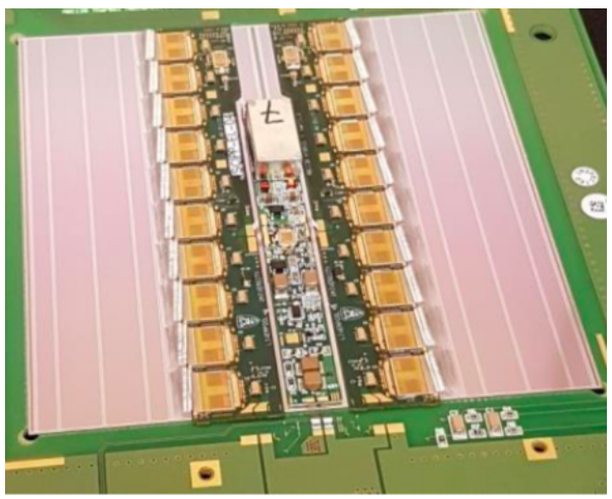
Wafer Probing

Single-chip Tests



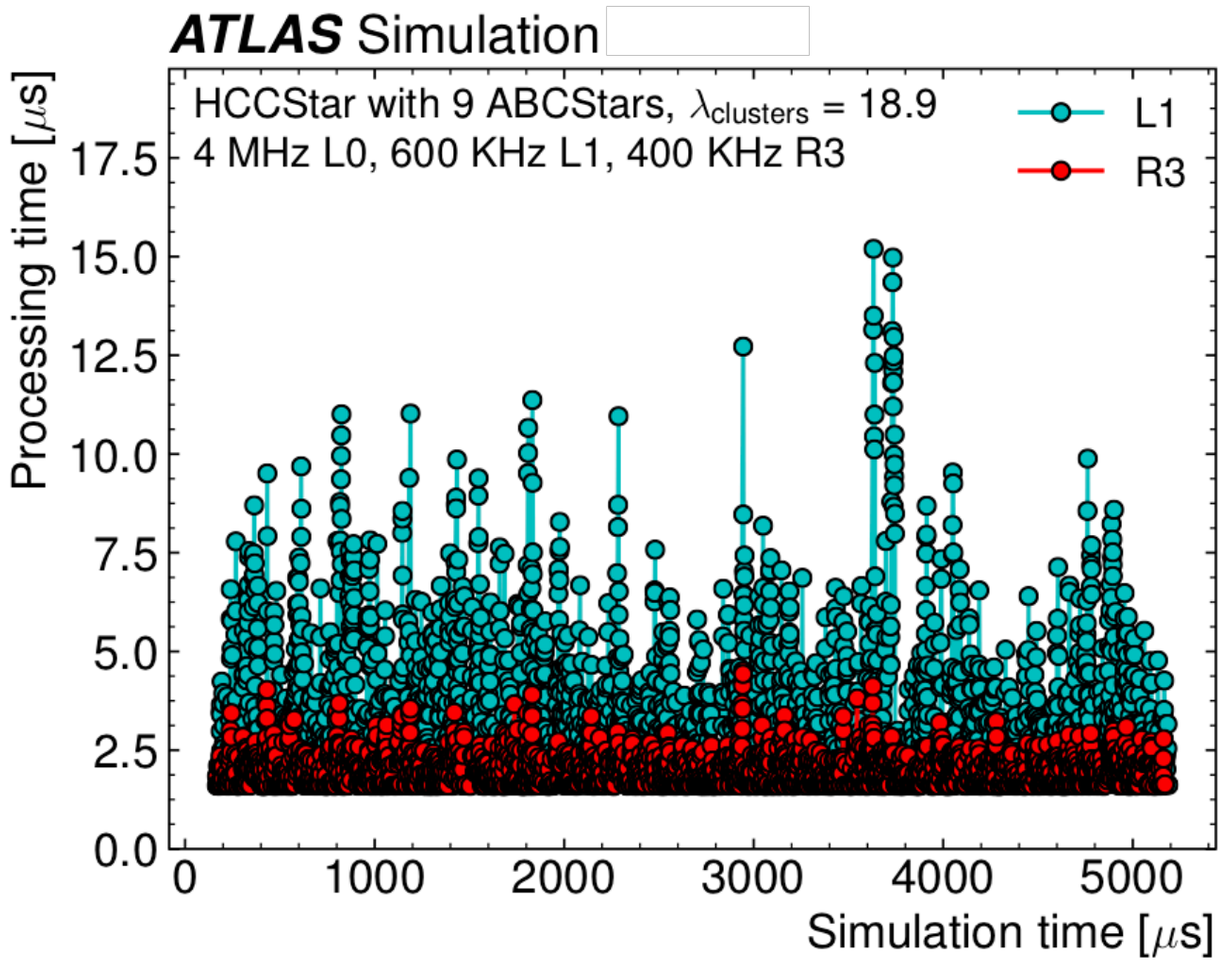
Radiation Tests

System Tests



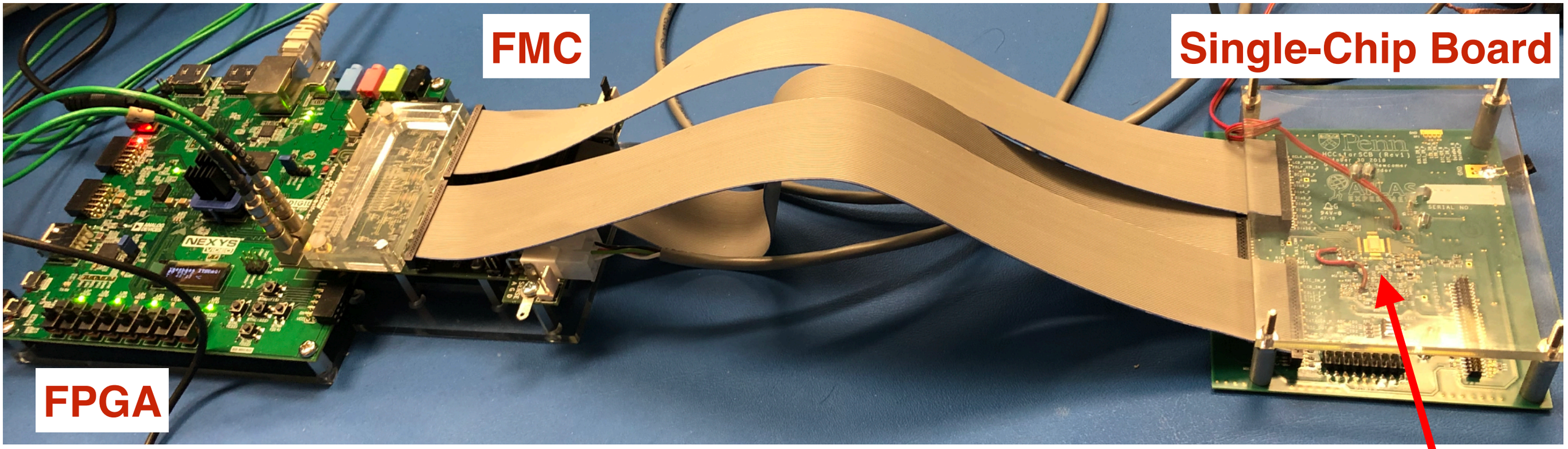
Simulation of Design

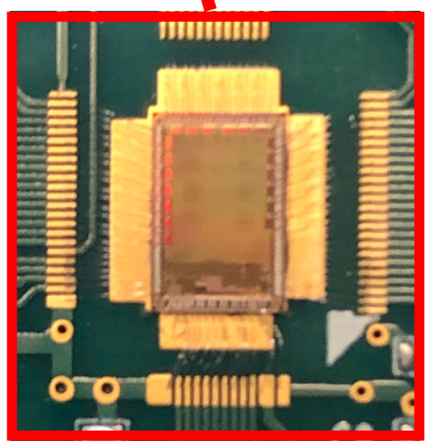
- Verified RTL design in using **python-based cocotb**
  - Easy to pick up, powerful, full control
- Hundreds of **unit tests** run daily to probe all logic and simulate unique situations
- Advanced **trigger tests** w/ both HCCStar & ABCStar
  - Realistic data placed on 256 inputs, using **predicted cluster occupancy** for various scenarios
  - **L1 & R3 trigger processing times** below latency requirements (25 & 6 μs)
  - Good recovery from data errors & buffer overflows, even at high trigger rates
- See Ben Rosser's poster for more info!



Visualization of L1 & R3 processing time for highest-occupancy scenario

Single-Chip Testbench



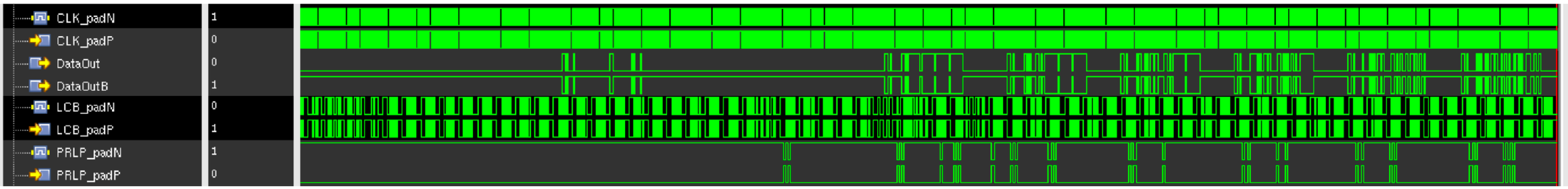


- Test infrastructure for real Star chips consists of
  - **Single-chip board**, wire-bonded to a single Star chip
  - Nexys Video **FPGA** loaded with bitstream vectors for all HCCStar input lines
  - Custom **FPGA Mezzanine Card** to drive input lines and monitor voltages/currents/temperature

Single-Chip Testing

- **Basic functionality** and many **edge cases** tested
  - **Simulate ABCStar clusters** for authentic trigger tests
  - HCCStar **output checked against expectation** in real time
- **Simulation waveforms converted to bitstreams**, allowing existing tests to be played on real system

Simulation waveforms

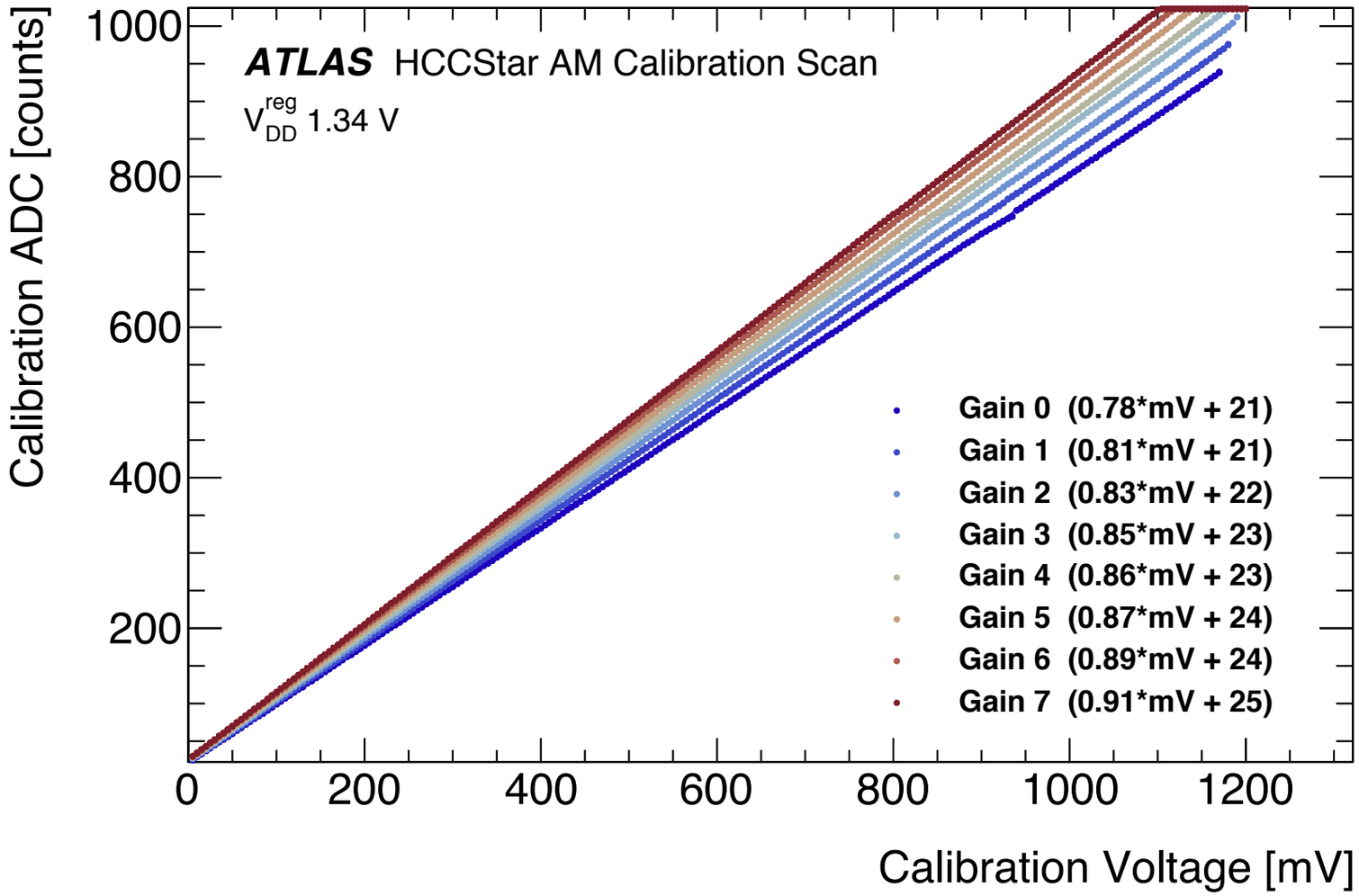



```
0ff 00f 087 008 078 00d 055 00d 0ff 017 087 010 078 015 055 015 0ff
01f 087 018 078 01d 055 01d 0ff 027 087 020 078 025 055 025 0ff 02f
087 028 078 02d 055 02d 0ff 037 087 030 078 035 055 035 0ff 03f 087
038 078 03d 055 03d 0ff 04f 087 048 078 04d 055 04d 0ff 057 087 050
```

Bitstream input to real HCCStar

Analog Monitor Testing

- HCCStar includes a basic **Analog Monitor** (AM) of voltages and current
- **Calibration Scan** derives gain (counts / mV) for 8 settings



Good linearity seen in response, even down to zero

Probe Station

Custom probe cards for each Starchip

Easy swapout of probe card & Single-chip board

96 HCCStar chips per wafer

Single-Chip Board

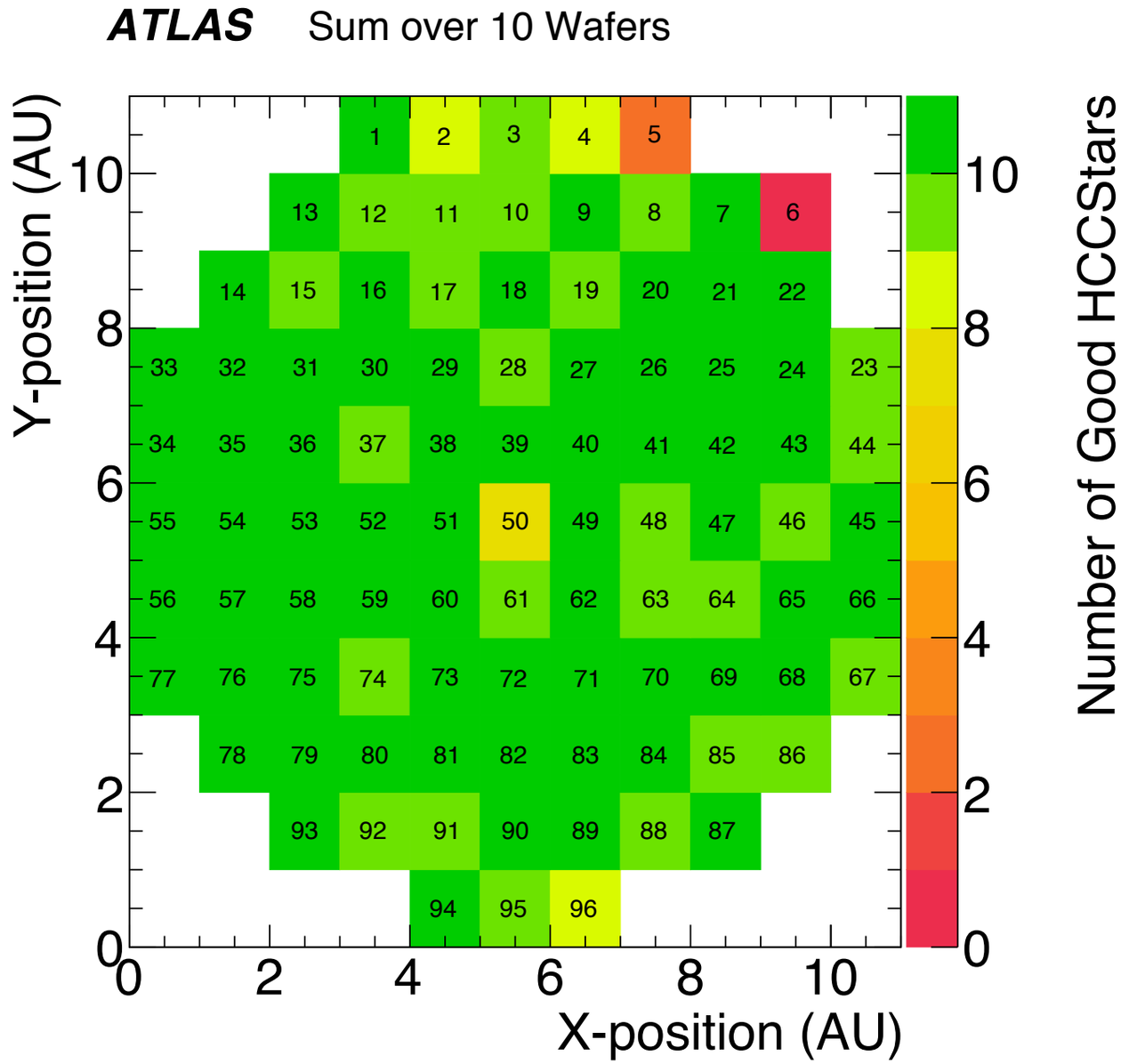
Probe Card

FPGA+FMC Testbench

Star Chip Wafer

HCCStar Probe Tests

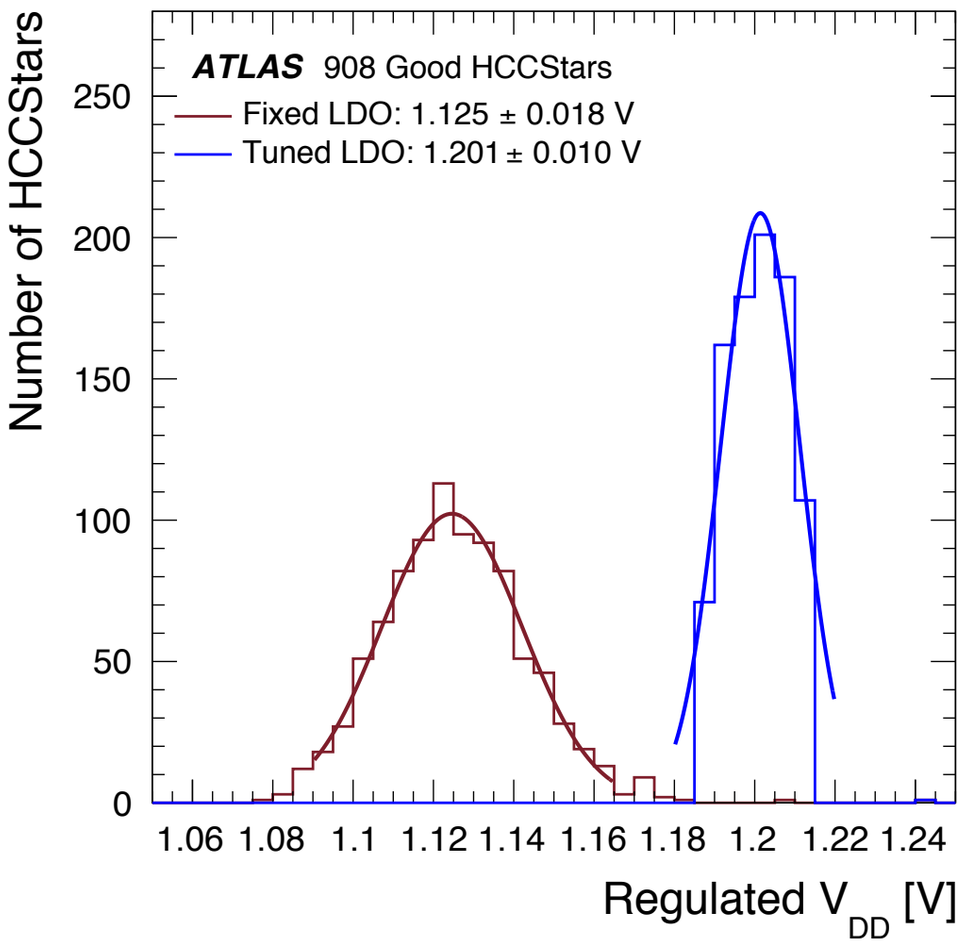
- Comprehensive suite of tests identify bad chips due to process variation
  - **Unresponsive** to configuration (2%)
  - Voltages and currents outside of **validity ranges** (0.5%)
  - **Analog tests** including calibration scan, requiring reasonable gain ranges (1%)
  - **Communication** & **digital trigger** (3%)
    - Edge cases (i.e. force all packet errors)
    - Check for stuck bits in packet buffers
    - Very intensive trigger rates
- **95% yield of good chips (960 total)**



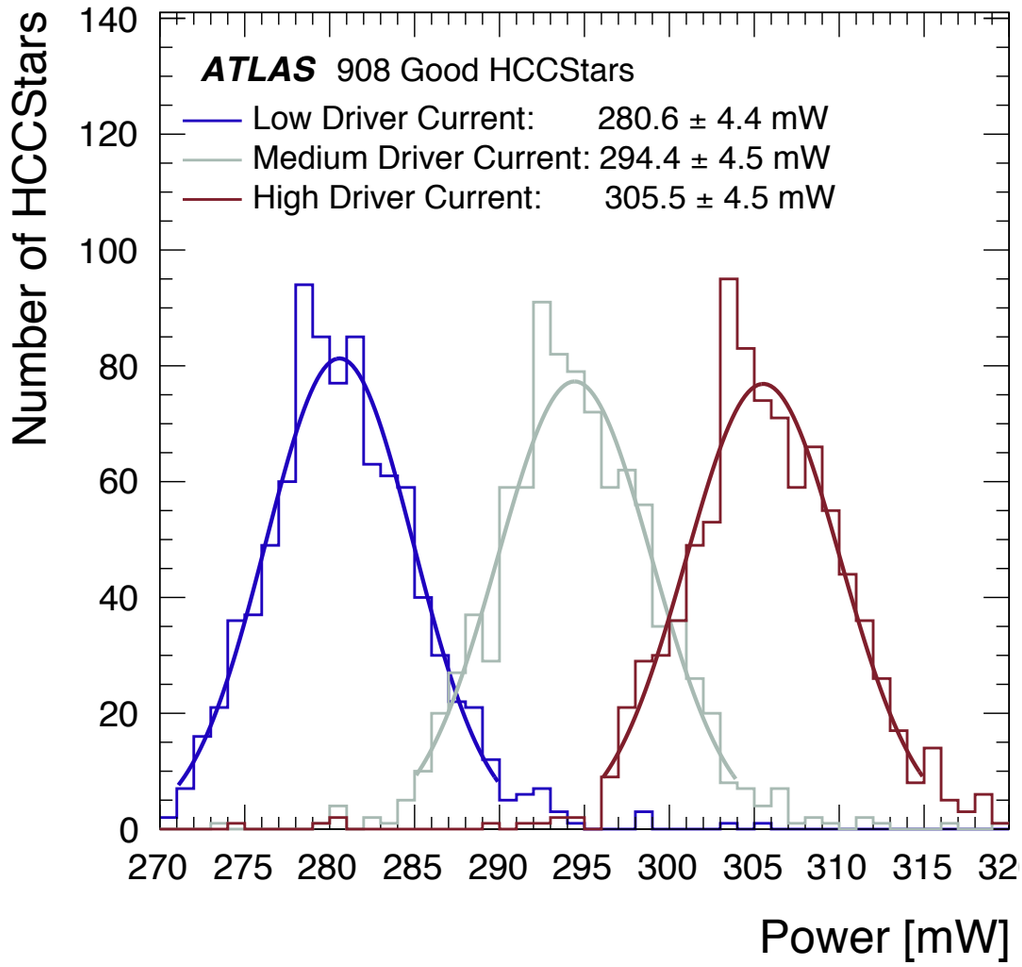
HCCStar yield per position across 10 wafers

Example HCCStar Diagnostics

Voltage vs. LDO setting



- Internal voltage must be **regulated at 1.2V** using CERN-designed low drop-out regulators (LDO)
- **Uncalibrated voltage** consistent within ±0.02V
- By **tuning LDO setting**, all chips able to achieve 1.20±0.01 V



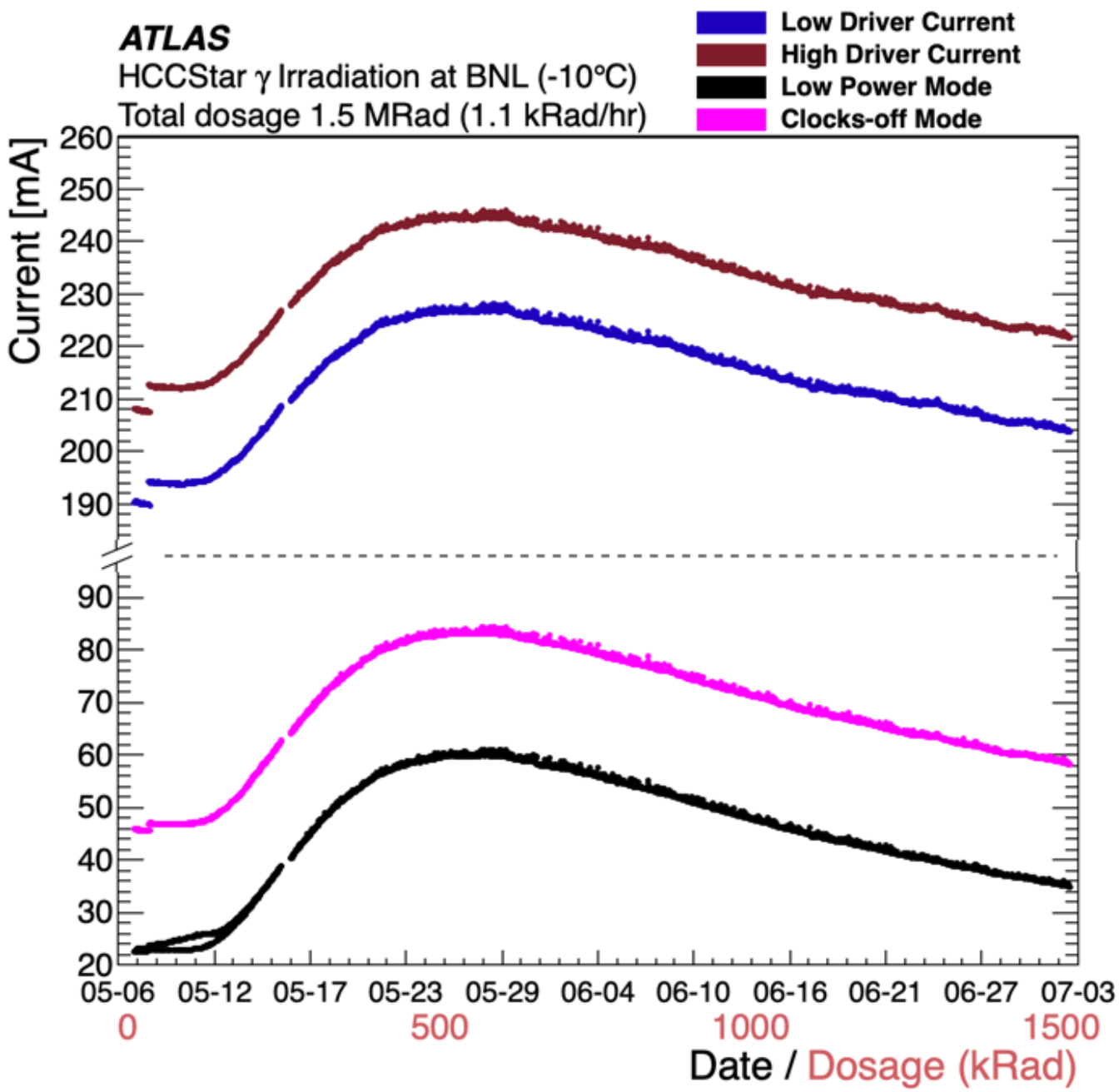
Power consumption of 906 HCCStars

- **Power consumption** follows Gaussian distribution
  - Nominally between **281** & **306** mW, is reduced to 69 and 34 mW in clocks-off and low-power mode
- All diagnostics show HCCStar behavior within specifications

TID Gamma Irradiation

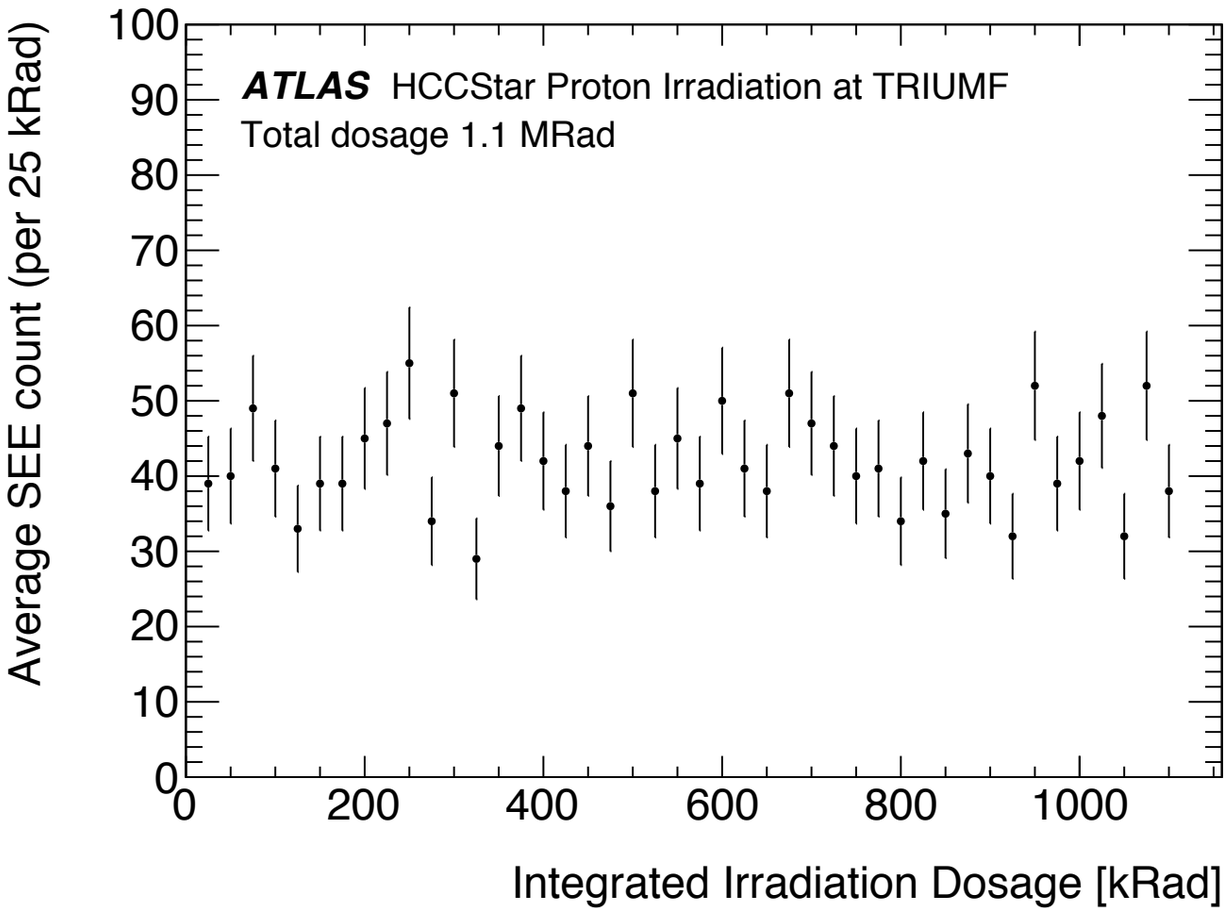
- Expect total ionization dose (TID) around 50 MRad over HL-LHC lifetime
  - NMOS transistors known to have a **TID-dependent current increase**
- Measured using **1 MeV γ-radiation** from a Co-60 source, targeting HL-LHC rates
  - Tests all 3 Star chips and various temperatures / irradiation rates
  - Full suite of trigger & analog tests during irradiation for realism
- Pre-irradiation shown to remove TID bump, studies ongoing on permanence

Chip	Rate (kRad/hr)	Temp. (°C)	Current Increase
HCCStar	1.1	-10	15%
AMAC	1.1	-10	25%
ABCStar	0.6	0	30%
ABCStar	0.6	-10	60%
ABCStar	1.1	-10	90%
ABCStar	2.5	-10	140%



SEE Irradiation

- Star chips will be subject to both temporary & destructive Single-Event Effects (SEE)
  - Minimize disruption through **register triplication** (auto-correcting) and **Hamming encoding** of finite-state logic
- Recent SEE tests at TRIUMF using **480 MeV proton beam**
  - Heavy Ion testing at end of August



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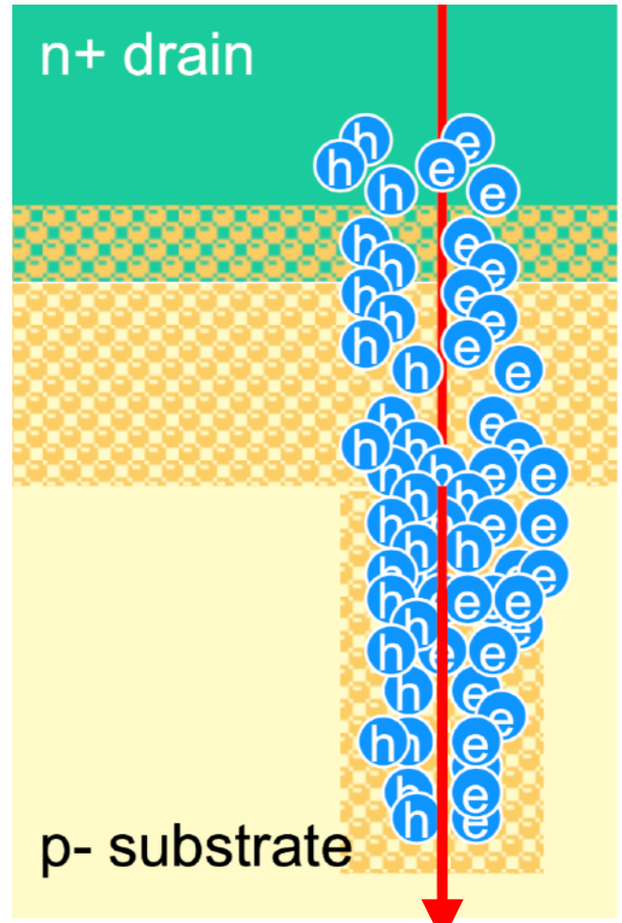
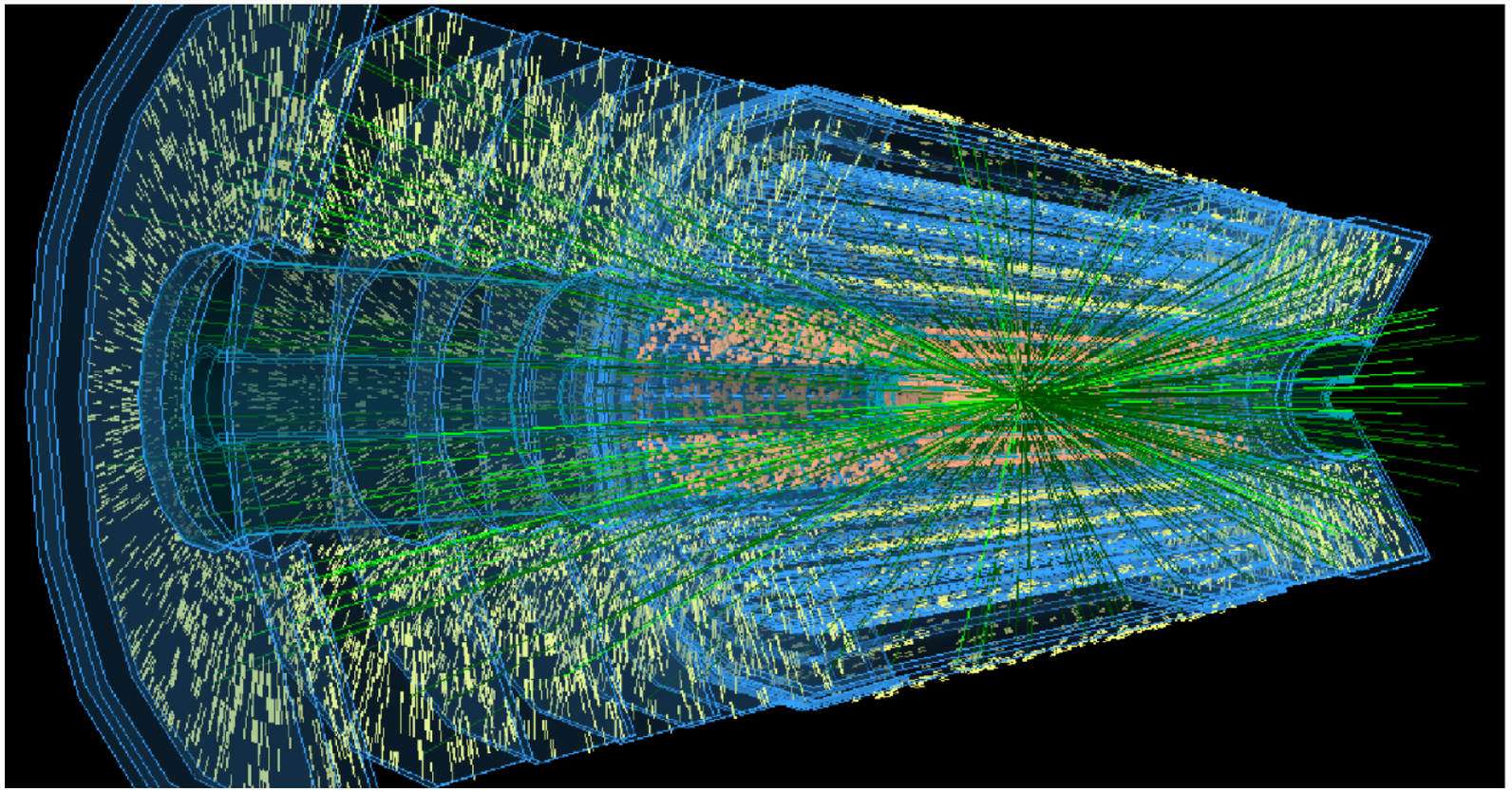


- At 1kRad/hr during HL-LHC, HCCStar will experience about **40 corrected bitflips** each day
  - Expect significantly fewer uncorrectable SEEs (2+ bitflips)

Outlook



- HCCStar design well validated at all stages: simulation, single-chip testing, and large-scale probing
  - Have a good handle on consequences of high-radiation environment (TID current increase, SEEs)
- Final design reviews proceeding smoothly, pre-production scheduled to begin within a year
- ITk detector will need ~18k AMAC, 26k HCCStar, and 234k ABCStar ASICs
- Early & thorough testing is the key to success!