Upgrade of the CMS electromagnetic calorimeter barrel readout electronics for the High-Luminosity LHC
The CMS EM Barrel Calorimeter

Lead Tungstate Crystals

Assemblies of modules and supermodule

Installation of 36 supermodules w/in CMS 3.8T Solenoid

(61,200 Crystals)

Essential for standard model, precision measurements, and new physics search programs
High Luminosity LHC

×10 larger data set for physics (wrt Run 3)

<table>
<thead>
<tr>
<th>LHC</th>
<th>HL-LHC</th>
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<tbody>
<tr>
<td>E</td>
<td>7–14</td>
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<tr>
<td>$\mathcal{E}_{\text{peak}}$</td>
<td>2</td>
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<tr>
<td>$\mathcal{P}_{\text{peak}}$</td>
<td>40–60</td>
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<tr>
<td>$\int \mathcal{E}$</td>
<td>≥ 50</td>
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<tr>
<td>$\int \mathcal{P}$</td>
<td>300–500</td>
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<td>14 TeV $\cdot 10^{34}$ cm$^{-2}$ s$^{-1}$</td>
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<td>5–7.5</td>
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<td>150–200</td>
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<td>250–320</td>
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<td>3000–4000</td>
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<td>fb$^{-1}$/year</td>
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<td>fb$^{-1}$ total</td>
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A challenging environment for physics and detector components

Numerous preparations underway for running in 2026 and beyond
Physics with ECAL at HL-LHC

LHC => HL-LHC

- Determine Higgs couplings $\lesssim 10\%$ level, differential meas.
- Higgs self-coupling
- New physics via EW channels, Jets/MET, …

Precision energy measurement / resolution required

However, high luminosity running results in many interaction vertices (pileup).

Choosing an incorrect vertex reduces resolution for event reconstruction

Precision timing can be used to reduce pileup effects at high lumi, eg:
- ECAL timing for photon pointing
- “4D” tracking to improve vertex localization in time and space (see talk by Si Xie)
Performance of detector components at HL-LHC

- Crystal transparency affected by radiation damage
  - Transparency loss in barrel < 50% over HL-LHC running => no need for replacement*

- APD dark current will increase with integrated luminosity and become a dominant contribution to $\sigma_E$
  - x10 more noise after 3000/fb

- Dark current depends on temperature
  - Mitigate by cooling the calorimeter to 9°C (currently at 18°C)
  - Will also enhance the light yield of PbWO$_4$ by ≈20% ($\Delta S/S = -2%/\degree C$)

- Further suppressed by reducing amplifier shaping time

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*ECAL (+ HCAL) endcaps need complete replacement. See high granularity, silicon/scintillator based, sampling calorimeter talk by Maral Alyari
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- Dark current depends on temperature
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  - Will also enhance the light yield of PbWO$_4$ by $\approx 20\%$ ($\Delta S/S = -2\%/^\circ C$)
- Further suppressed by reducing amplifier shaping time

- Will need improved discrimination of direct ionization signals (spikes), associated with particles striking the APDs and rarely interacting to produce secondaries
Upgrades for HL-LHC

- **Major requirement:** larger trigger rates and latencies to exploit higher luminosity
  - Level 1 rate 750 kHz, 12.5 μs latency (currently 100 kHz, 4 μs)
  - spike mitigation mandatory for L1 rate
  - Front-end and off-detector electronics need replacement
  - Requires removal, refurbishment, re-installation, re-commissioning of 36 EB supermodules

- **Opportunity to maintain and enhance performance goals w.r.t. Phase 1:**
  - same excellent energy resolution
  - fast response for pileup mitigation and noise reduction
  - timing resolution and improved granularity at trigger

Complete replacement of front end (on detector) and off detector electronics
2 new custom (radiation hard) ASICs for the VFE upgrade

- **CATIA ASIC**: analog ASIC
  - Trans-Impedance Amplifier (TIA) architecture,
  - 2x bandwidth of current MGPA
  - Energy signals dynamic range: 50 MeV → 2 TeV
  - 2 outputs, gain values: (x1, x10), with (50, 500) MeV LSB

- **LiTE-DTU ASIC**: digital signal processing ASIC
  - ADC: resolution: 12-bit, sampling frequency: 160 MS/s
  - Lossless data compression and transmission unit

- Also low-voltage regulator card (LVR): 1.2, 2.5 V
  - Point-of-load FEAST DC/DC converters
Front End Upgrade

Front End (FE) cars

- FE: fast optical links to stream all crystal data off-detector at 40 MHz
  - lpGBT/VL+ components (4×10.24 Gb/s data links, 1×2.56 Gb/s control link)
  - eLink serial interface to ADC, clock and i2C interface
  - ~ 25x increase in bandwidth from legacy system

- **Sufficient bandwidth to move all data processing off detector:**
  noise suppression, pulse reconstruction, trigger primitives generation, data buffering, etc moved to powerful FPGAs off detector)
Tests of first VFE prototypes

- Staged approach: discrete components first, minimal prototype with TIA only, full prototype (TIA + i2C + test pulse), full prototype in final package
- Commercial ADC for 1st tests, data transmission units via custom adapter card

- First characterization in lab with laser light + crystal + APDs
- Extensive tests performed at the CERN H4/H2 beam line on a 5×5 crystal matrix
  - H4: very pure electron beam, $\Delta p/p = 0.5\%$ with $20 < p < 250$ GeV
  - H2: pion beam for APD direct ionization
- Plastic fiber hodoscopes for position measurement
- 2 Micro Channel Plate devices (1.2 cm diameter, $< 1 X_0$) for time reference
Tests of first VFE prototypes

- **2016:** discrete component TIA + DRS4 readout at 5 GS/s
  - different sampling rates emulated offline
  - 160 MHz optimal, at lower frequencies dependence on the phase between APD signal and ADC clock

- **2018:** first prototype ASIC TIA chip + commercial ADC at 160 MHz
  - Realistic noise performance
  - Energy resolution matches legacy electronics
  - Time resolution matches target (<30 ps @ 50 GeV)

Results shown for 18°C (Data also taken at 9°C)
Impact of upgrade on trigger

- Target for spike discrimination: 1 kHz L1 rate for $E_T > 5$ GeV
- With faster shaping and 160 MHz sampling frequency => strong pulse shape discrimination for spikes and scintillation signals

- Single crystal level available at L1 (×25 better granularity than legacy system)
  - More sophisticated trigger algorithms
  - Improve resolution, PU/background rejection
  - Pulse shape method can be combined with topology for spike suppression
Off detector electronics

- Barrel Calorimeter Processor
  - ATCA form factor
  - Main processing by two powerful Xilinx Kintex FPGAs
  - Embedded LINUX and real time OS systems for board monitoring, configuration, and control

- BCP functions
  - Concentrate detector raw data
  - Pulse reconstruction and noise suppression, build trigger primitives and transmit them to L1 Trigger
  - Receive the LHC clock and distribute with high precision to the on detector electronics.
  - Buffer and send event data to DAQ upon L1 Accept
  - Handle slow-control of on-detector electronics via lpGBT interfaces

108 boards for ECAL Barrel
Clock distribution

- The limiting factor in timing resolution with the current ECAL electronics (optimized for energy resolution only!)
- A well implemented back-end and FE capable of precision clock distribution should deliver ≈10 ps RMS (random) jitter
- Dedicated studies on the currently available GBTx serial link
  - Preliminary results indicate better performance with prototype of new lpGBT
- Alternate clock distribution schemes under evaluation also capable of satisfying jitter requirements
Summary

• The HL-LHC phase will bring exciting and challenging opportunities for precision measurements and new physics searches

• Motivated by trigger and physics requirements, redesigned BCAL electronics will provide:
  • equivalent energy resolution to Phase 1/legacy system
  • precise timing for electrons and photons
  • mitigation of pileup effects
  • mitigation of increased APD noise
  • anomalous signal filtering at L1 trigger
  • 25x higher granularity at L1 trigger

• With these upgrades, the CMS ECAL barrel will continue its excellent performance throughout HL-LHC