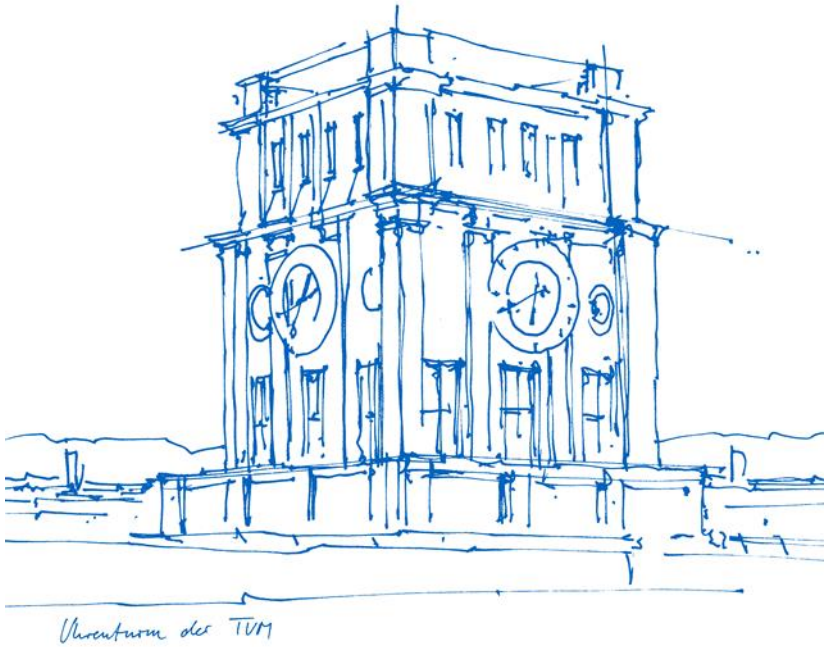
Integration of a Crosspoint switch in the COMPASS DAQ in 2018

D. Steffen



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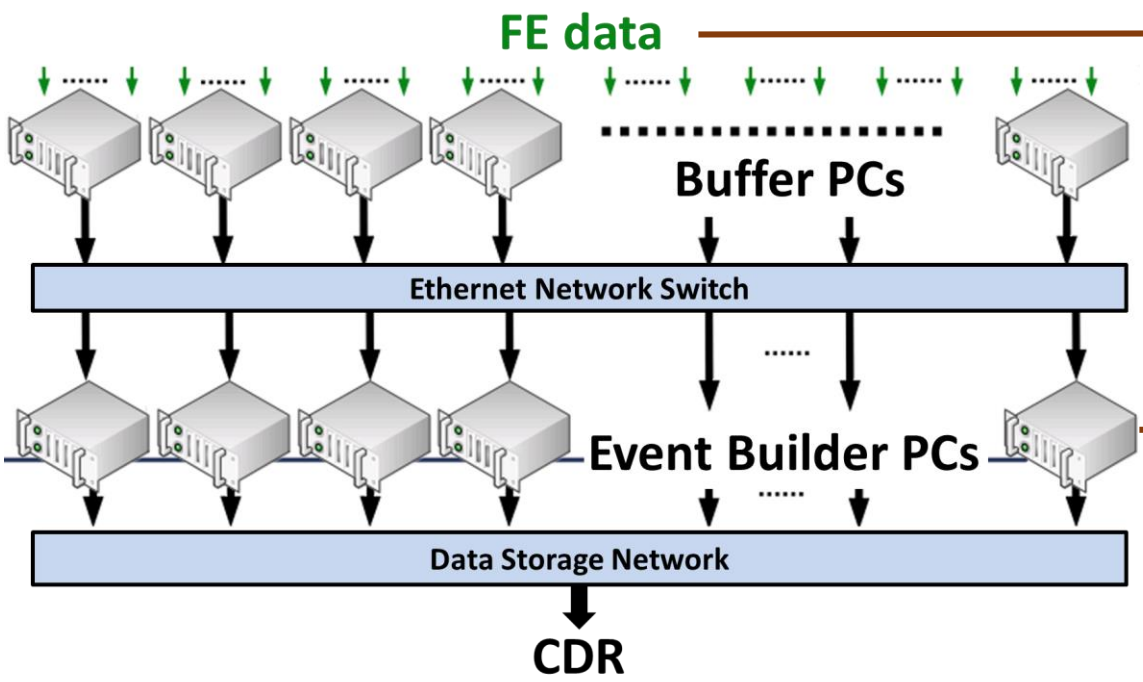
Traditional Event Building

Event Building(EB): combination of logically connected, but physically split data fragments



1st Level Trigger

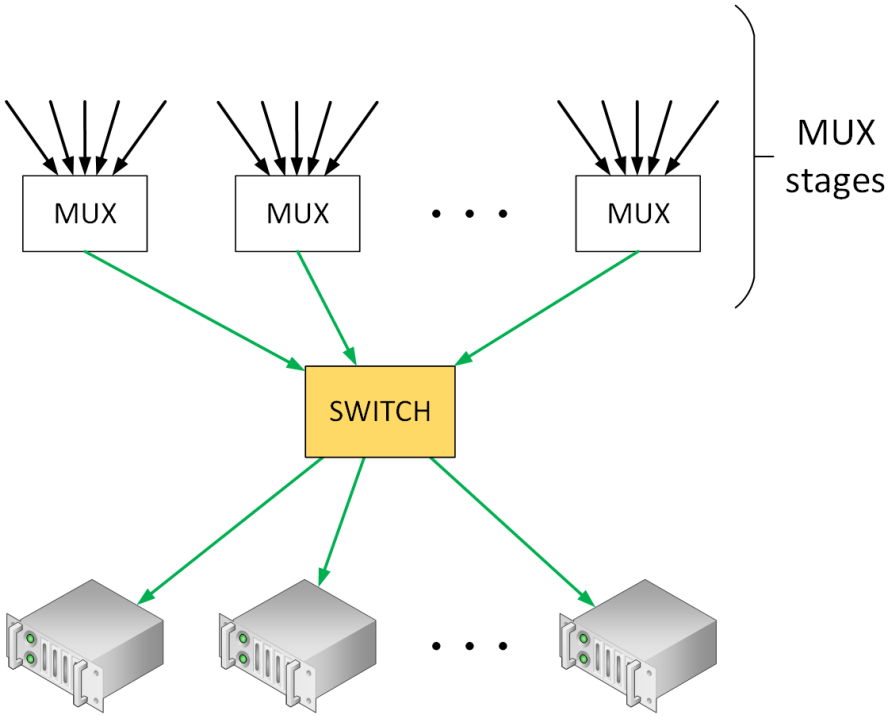
- Buffers data until receiving control msg to forward to specific builder unit
- Replicated over number of computers to fit performance needs and application scenario

High-Level Trigger

- Collects event fragments and combines them into complete event
- Replicated over number of computers to fit throughput requirements

Sophisticated traffic shaping to optimize throughput of EB-network switch (buffer utilization and data rate) and load on EB computers

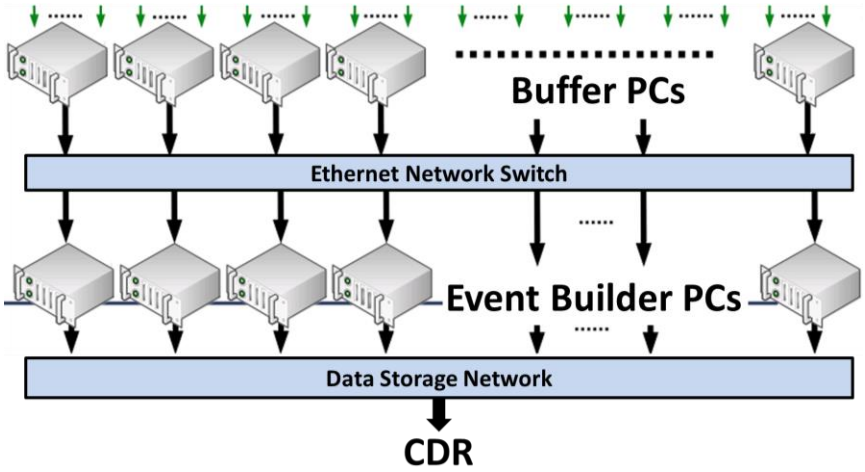
Hardware Event Building



- Usage of FPGAs and exploiting its properties:
  - Parallel processing
  - Pipeline architectures
- Continuation of the pipeline architecture in FEE
- Collecting of all data in one FPGA-module
- Optional multiplexing stages to reduce number of incoming links
- Distribution of fully assembled events to different computer nodes

Traditional vs Hardware EB

Traditional EB (Ethernet)



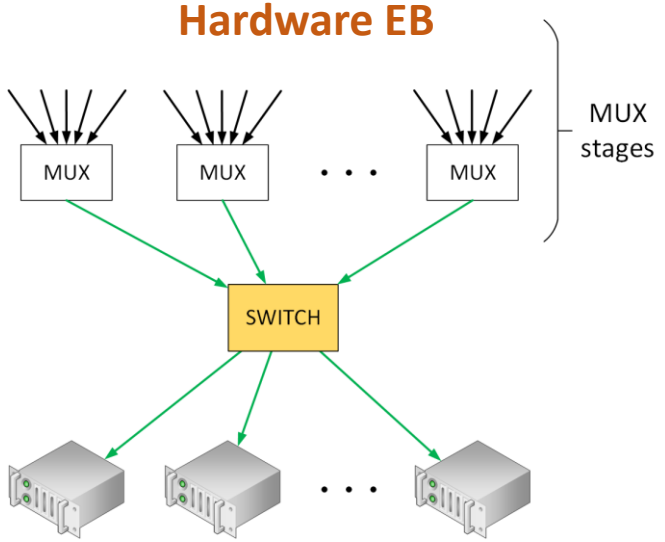
Advantages

- Easy integration of redundancy elements (traffic shaping according to load on nodes)
- Usage of mass-produced components and standards

Disadvantages:

- Throughput limited by EB-network switch
- Inefficient usage of max. bandwith due to:
  - Improper comm. pattern (N senders -> 1 receiver) => network congestion
  - Data overhead due to addressing etc.

Hardware EB



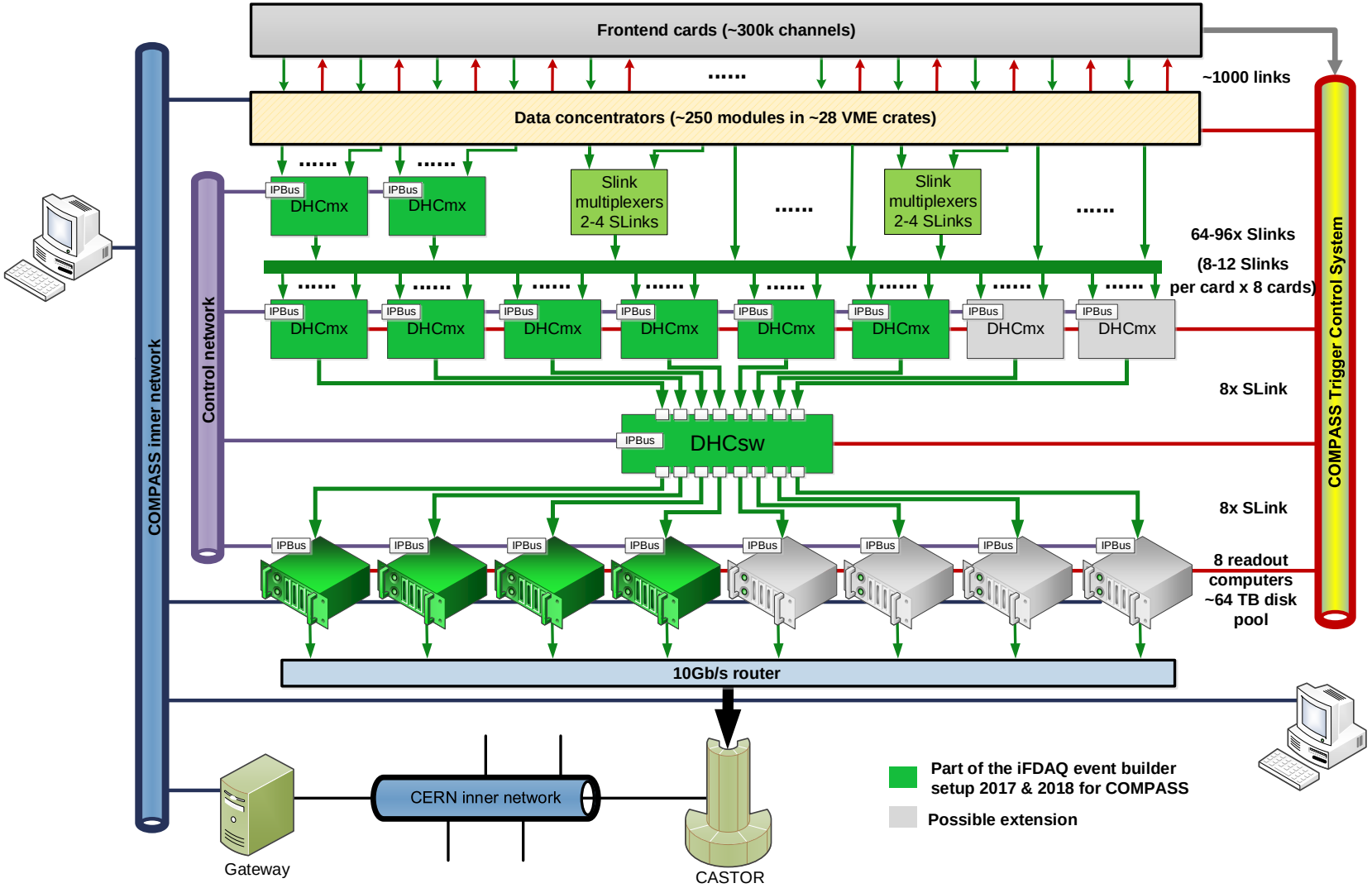
Advantages:

- Independence of network switch
- Efficient usage of link bandwidth (no addressing etc.)
- High reliability

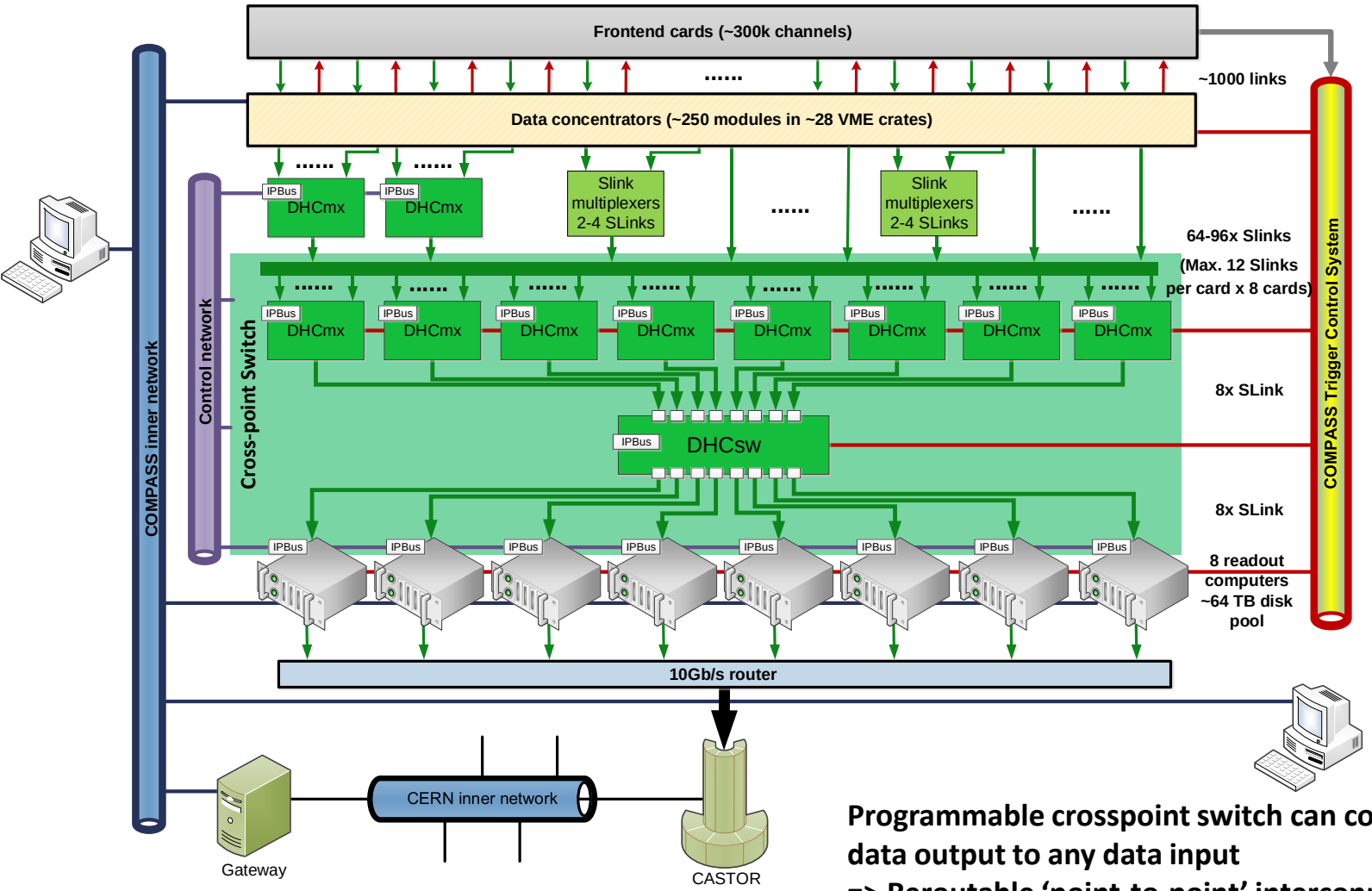
Disadvantages:

- Strong dependence on reliability of network nodes (no rerouting possibility in case of hardware failure)
- No possibility for dynamic network optimization (e.g. load balancing)

iFDAQ setup in 2018 DY



Switching Network Topology



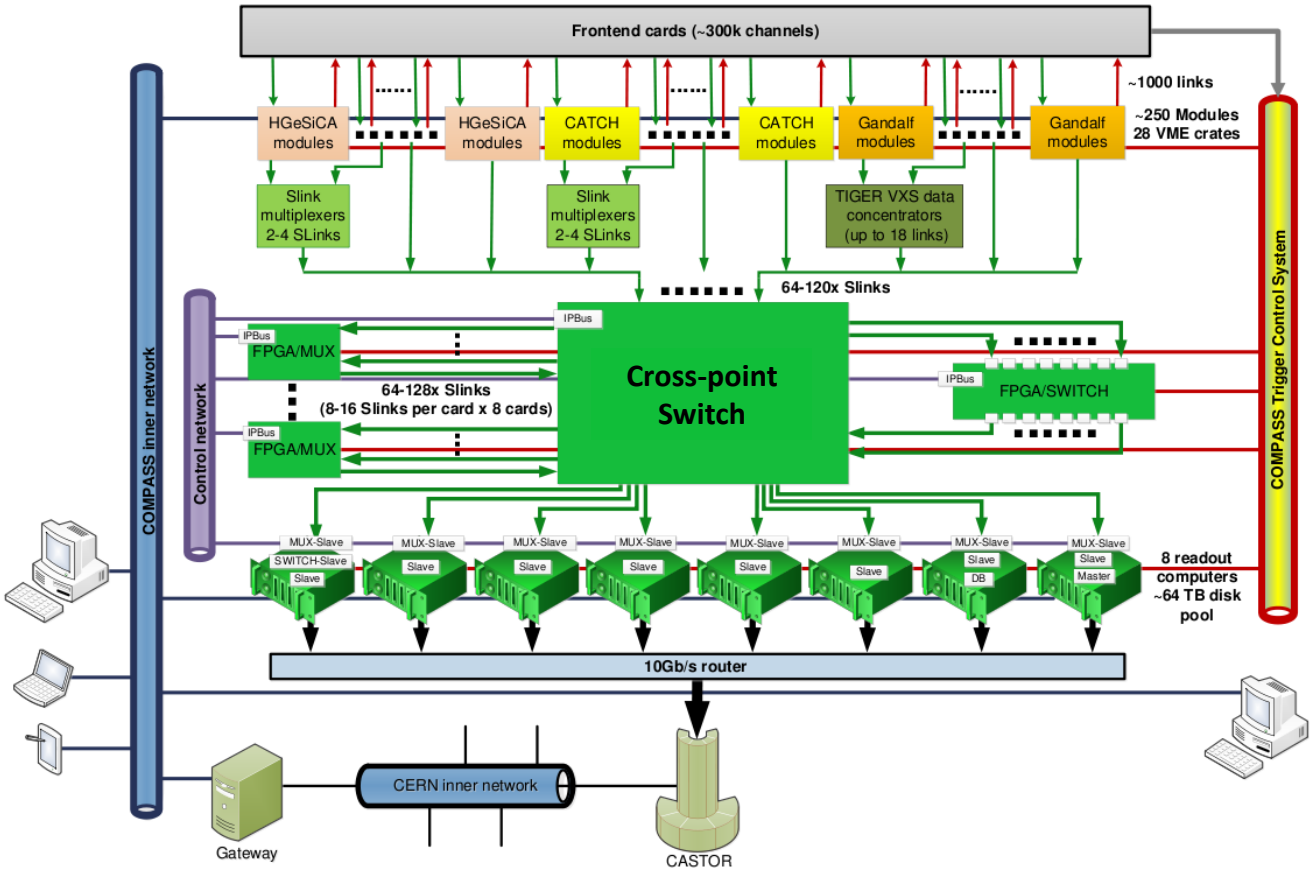
Programmable crosspoint switch can connect each data output to any data input
=> Reroutable 'point-to-point' interconnections between nodes of EB

Crosspoint Switch - Integration

Cross-point Switch

- connects:
  - FE electronics
  - DHCmx modules
  - DHCsw module
  - Spillbuffers
- purpose:
  - Ease of load balancing
  - System redundancy to compensate hardware failures

⇒ provides fully customizable network topology



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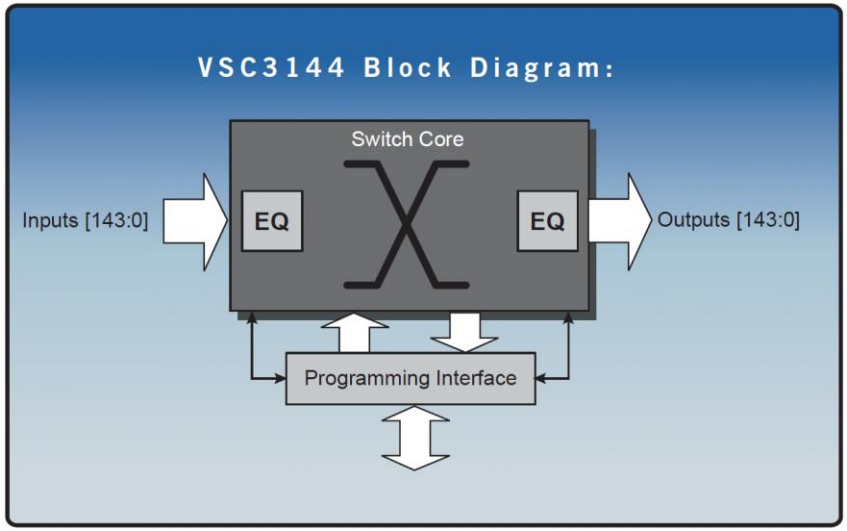
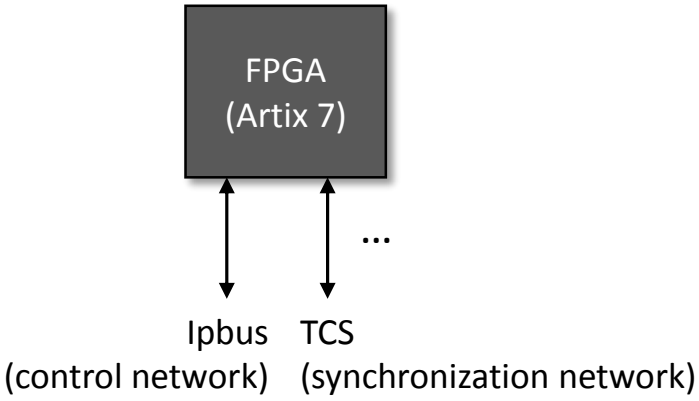
1. Motivation and Concept of the Switching Network Topology
2. **Hardware Design and Implementation of the Crosspoint Switch**
   - **Hardware Layout**
   - **Software Developments**
3. Performance in 2018 DY run and Outlook

Hardware: Vitesse VSC3144

- 144 x 144 strictly non-blocking cross-point switch
- Up to 6.5 Gbps bandwidth per port
- No registers used in data path i.e. asynchronous data path => no restrictions on the phase, frequency, or signal pattern of any input (protocol independent)
- 45mm x 45mm 1072-pin BGA package
- Core programming on port-by-port basis OR simultaneous issuing of multiple queued assignments (low latency: ns)





MPO connectors

- High density fiber technology necessary
  → Multi-fiber Push-On technology
- Easy installation due intuitive push-pull latching sleeve mechanism
- MPO harness cable to interface with LC-standard used so far in iFDAQ

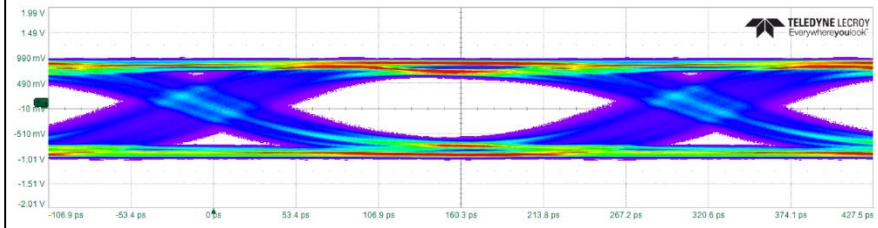
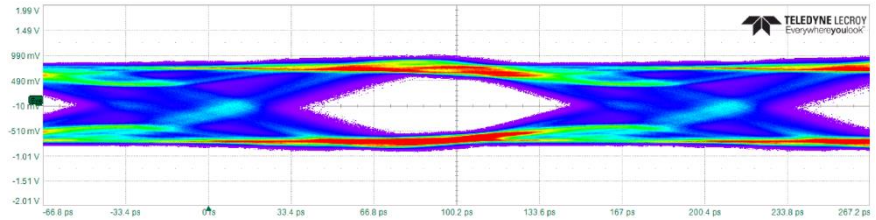
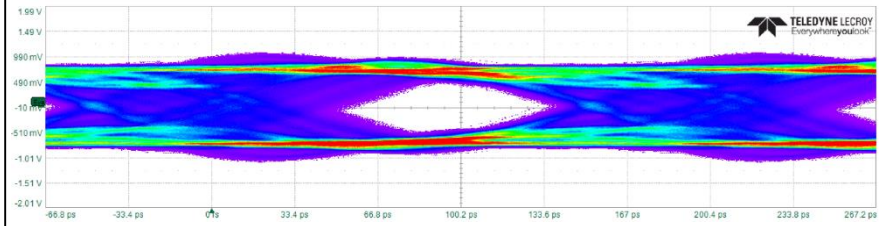
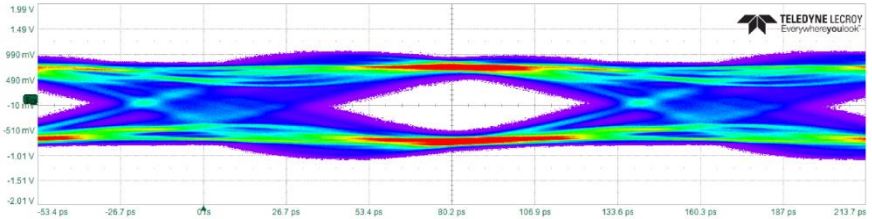
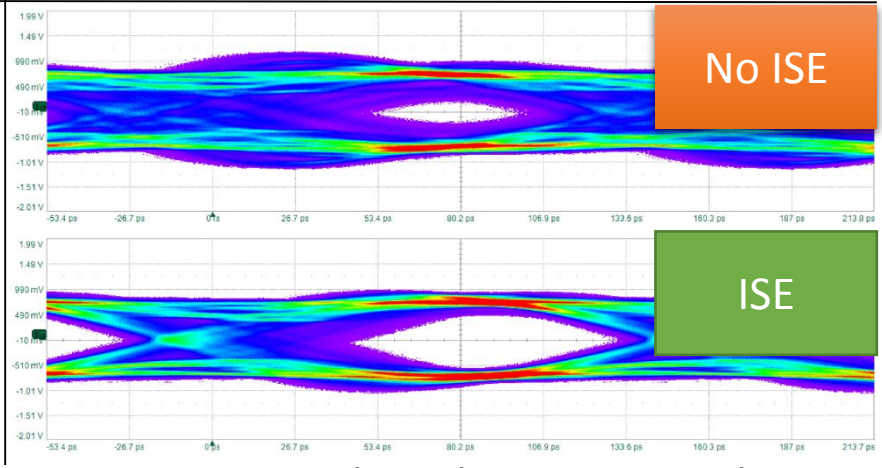
Crosspoint Switch – Hardware Design

Crosspoint Switch Components

- **interfaces:**
  - 12 x 12 channel CXP transceiver (MPO fiber connectors)
  - Ethernet for IPbus
  - JTAG
  - TCS (Trigger Control System) receiver
- **Switching and Control:**
  - **Vitesse VSC3144-02** – fully configurable 144x144, asynchronous, 6.5 Gbps crosspoint switch
  - **Xilinx Artix-7 FPGA** for switch control and monitoring

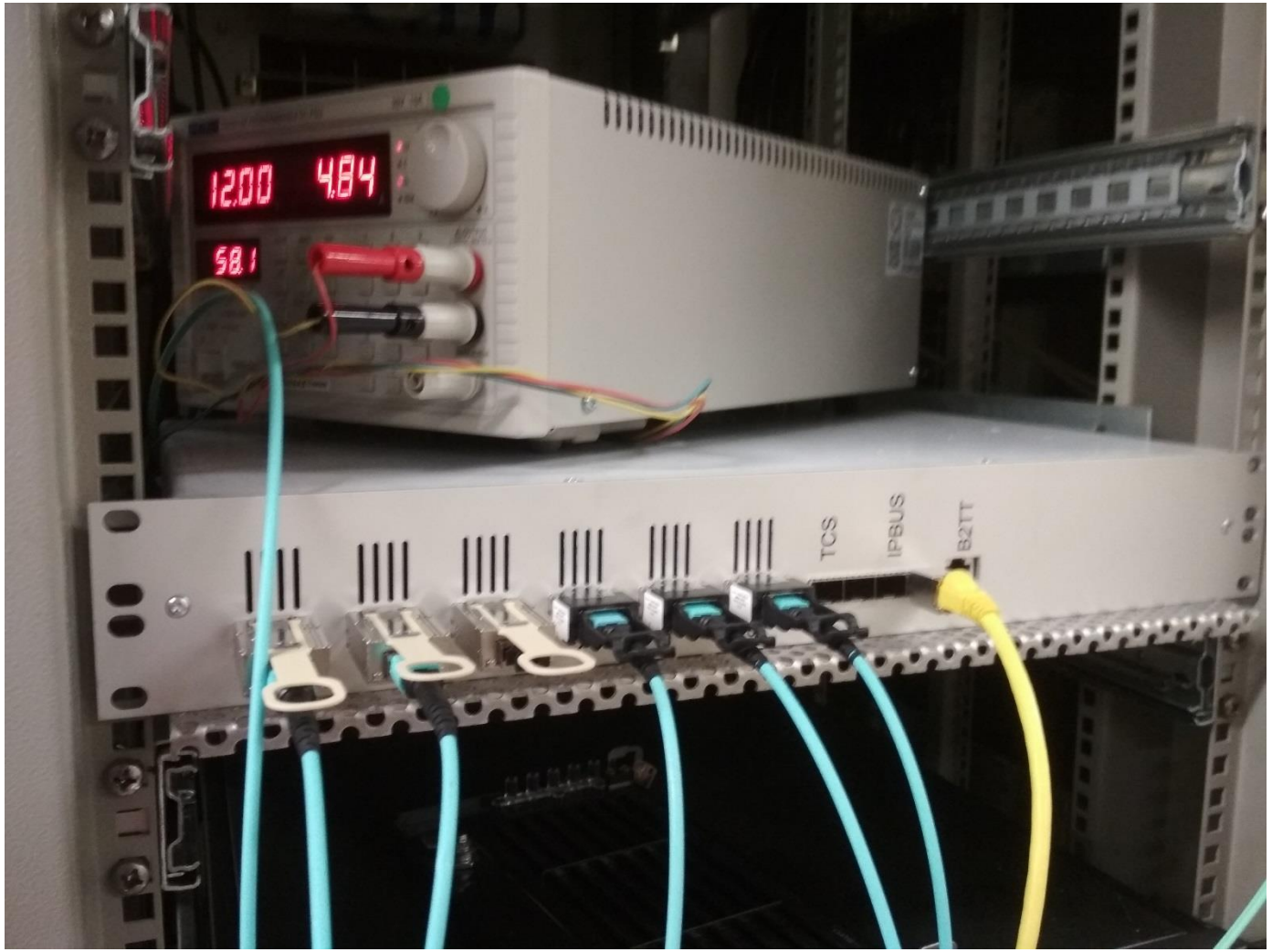
- **Interface FPGA – Crosswitch:**
  - 90 MHz, 11-bit parallel data bus
  - Multiple program assignments can be queued and issued simultaneously ⇒ fast programming (<< 1us)

Crosspoint Switch – Signal Distortion

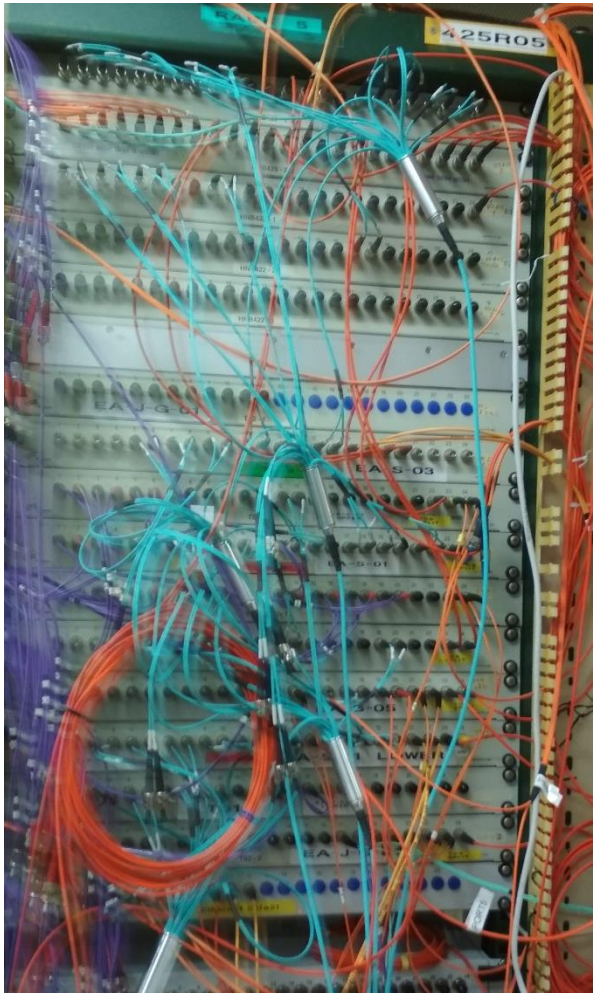
Line rate	Signal BEFORE switch	Signal AFTER switch
3.13		
5.00		
6.25		

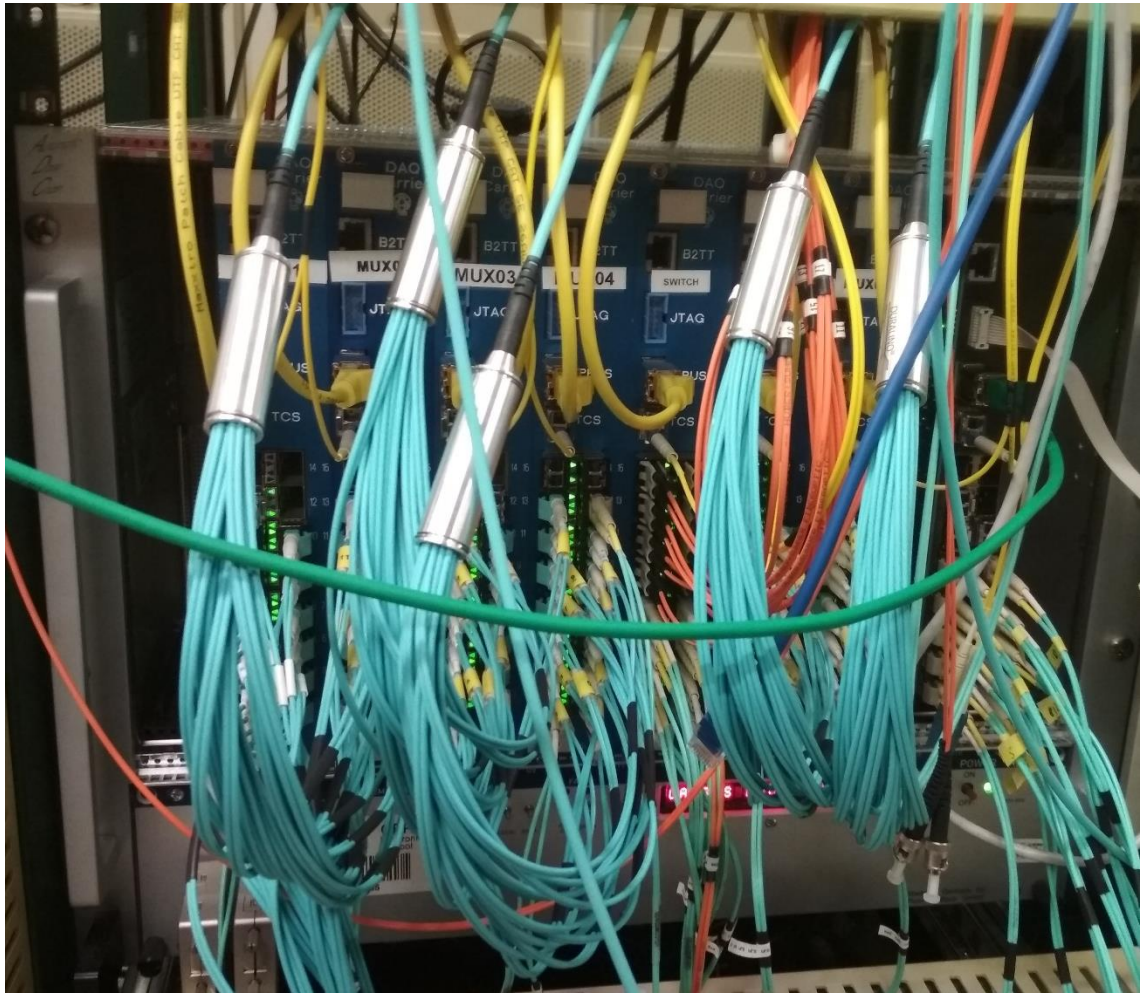
Input Signal Equalization on Switch

Crosspoint Switch in COMPASS DAQ



Crosspoint Switch in COMPASS DAQ

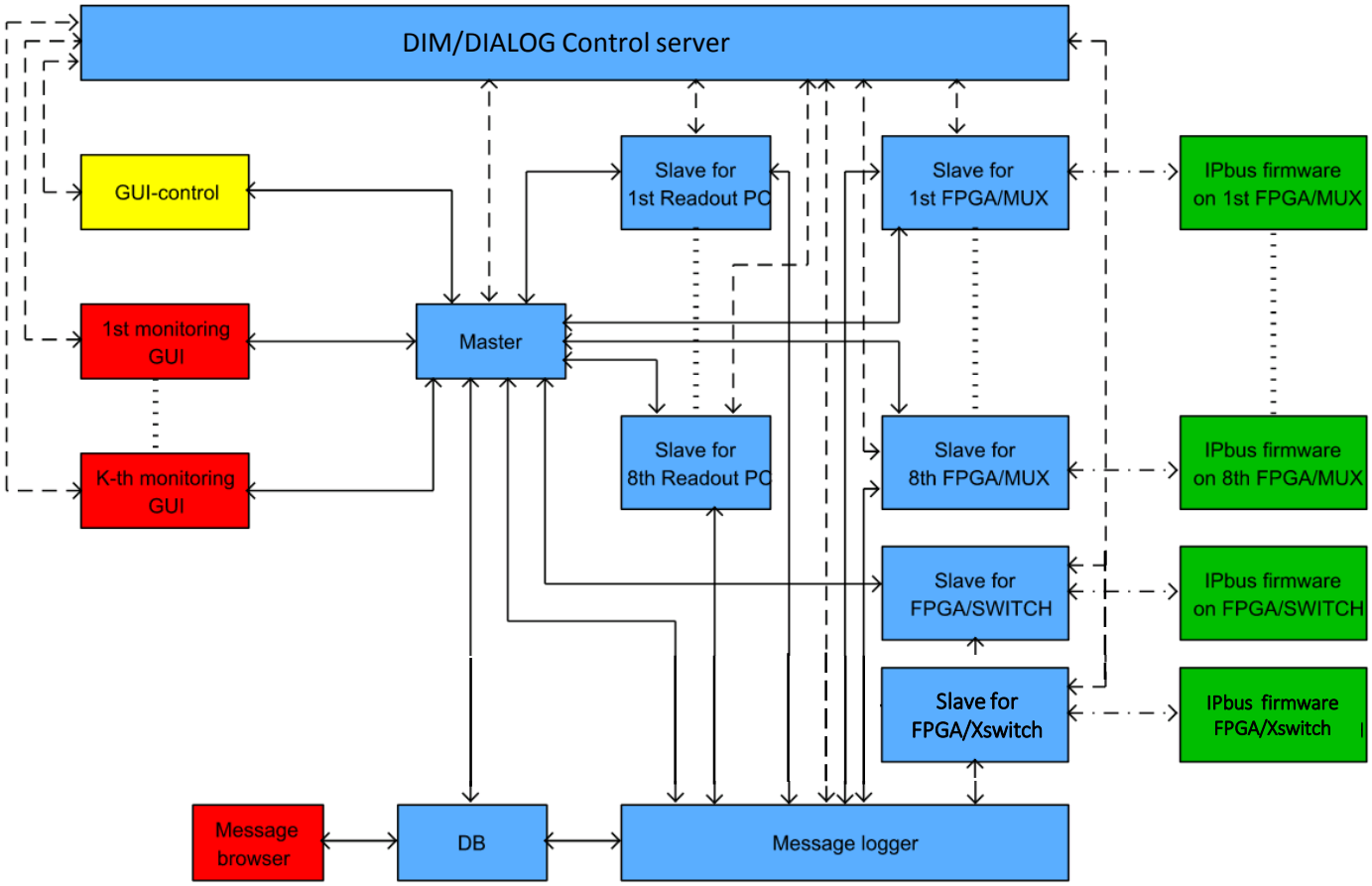




Software Development

Multilayer System:

- Master is the main control process
- **Slave-control monitors and controls the DHCs (hardware nodes)**
- Slave-readout: readout, verification, and transformation of the data
- Runcontrol GUI is a graphical user interface
- MessageLogger stores informative and error messages into the database
- MessageBrowser provides an intuitive access to messages stored in the database

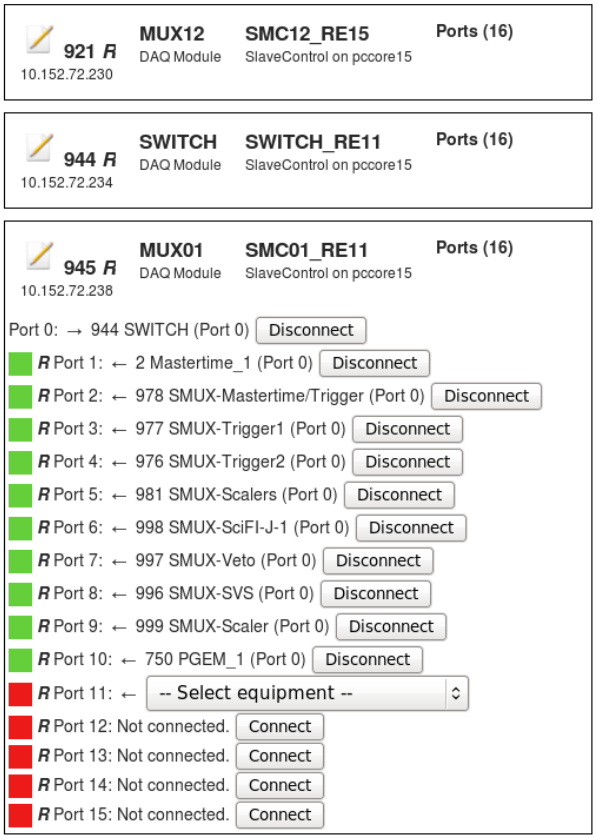


Software Operating Mode

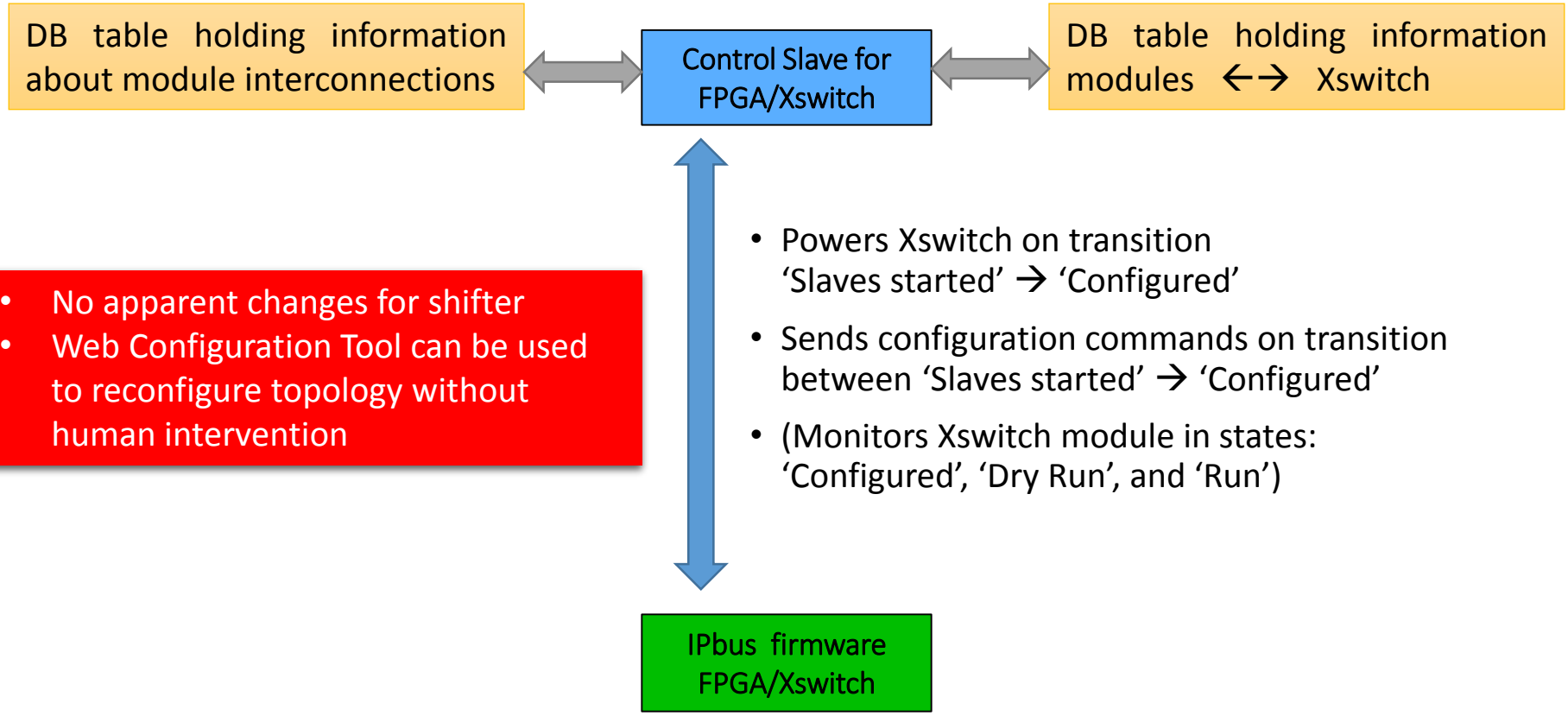
DB table holding information about module interconnections ⟷ Control Slave for FPGA/Xswitch ⟷ DB table holding information modules ←→ Xswitch

web configuration interface

XswitchUI



Software Operating Mode



Affected DB tables

Existing table

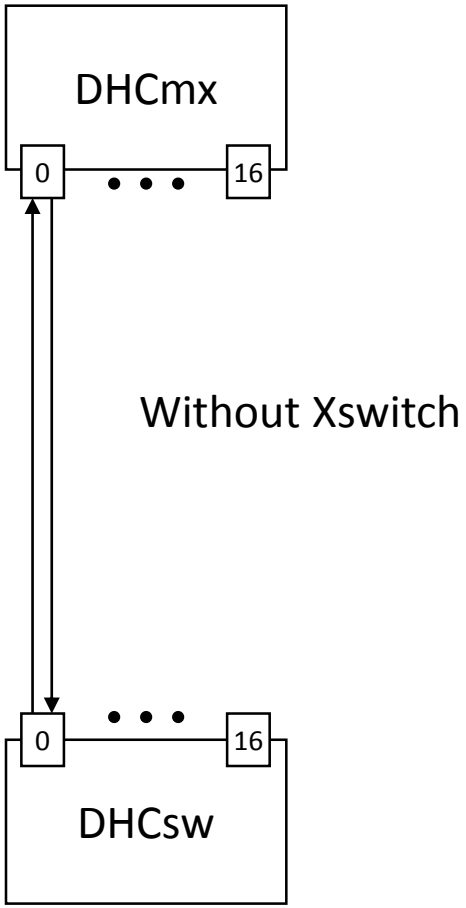
Port connection		
Port out	Port in	Runtype
357	587	4

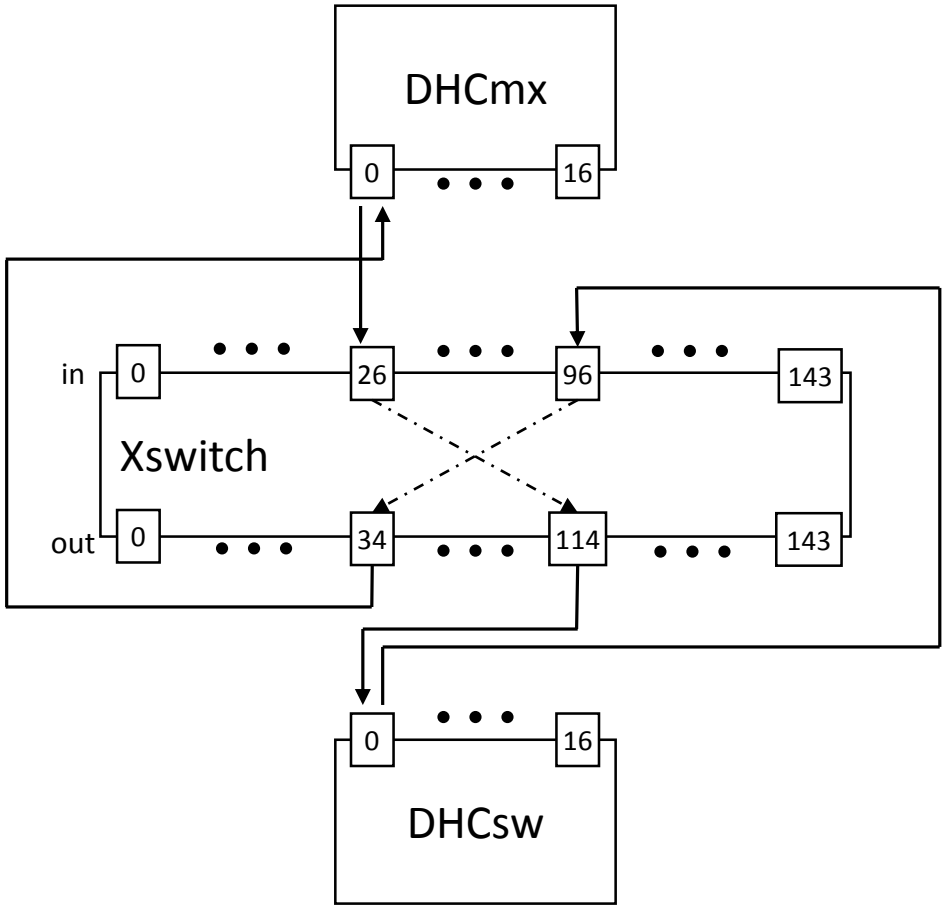
New tables

Xswitch connections	
Port id	In
357	892
587	888

Xswitch pairs				
Port id	In	Out	Cage	Fiber
892	26	34	2	11
888	96	114	3	2

Interconnection example





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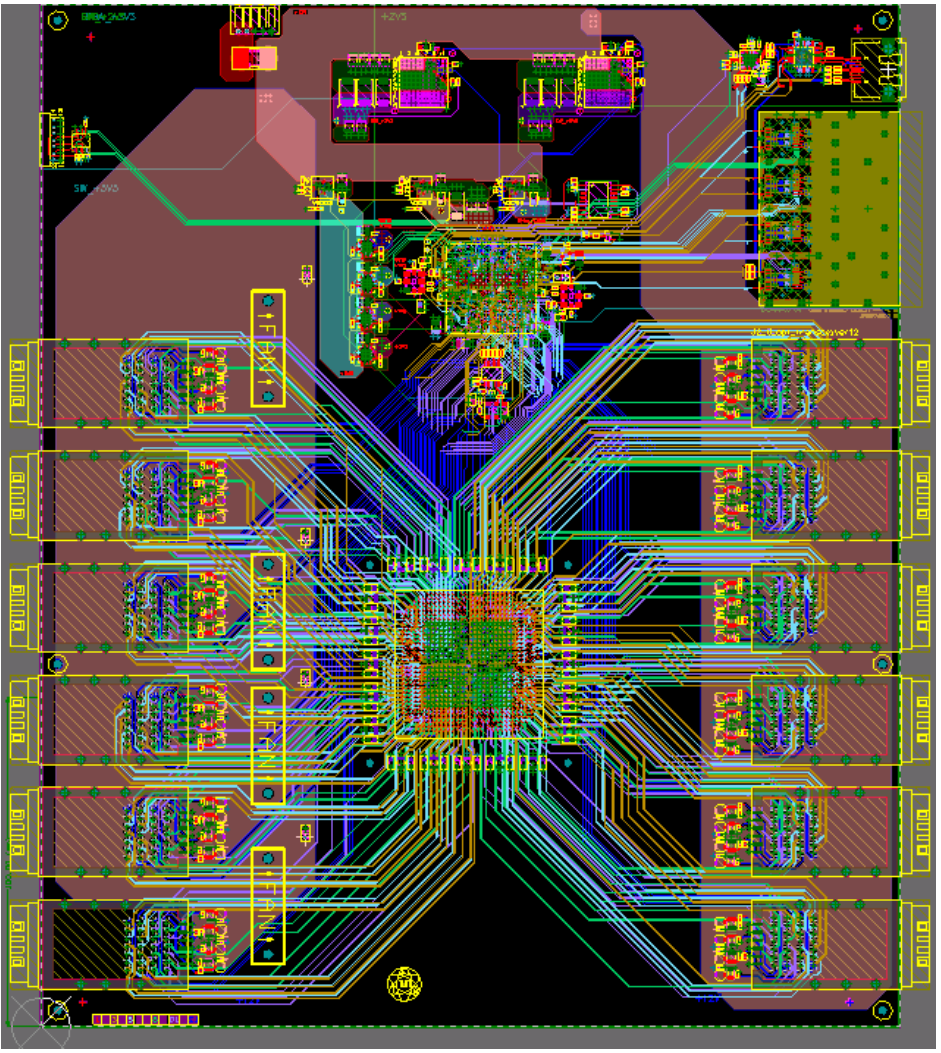

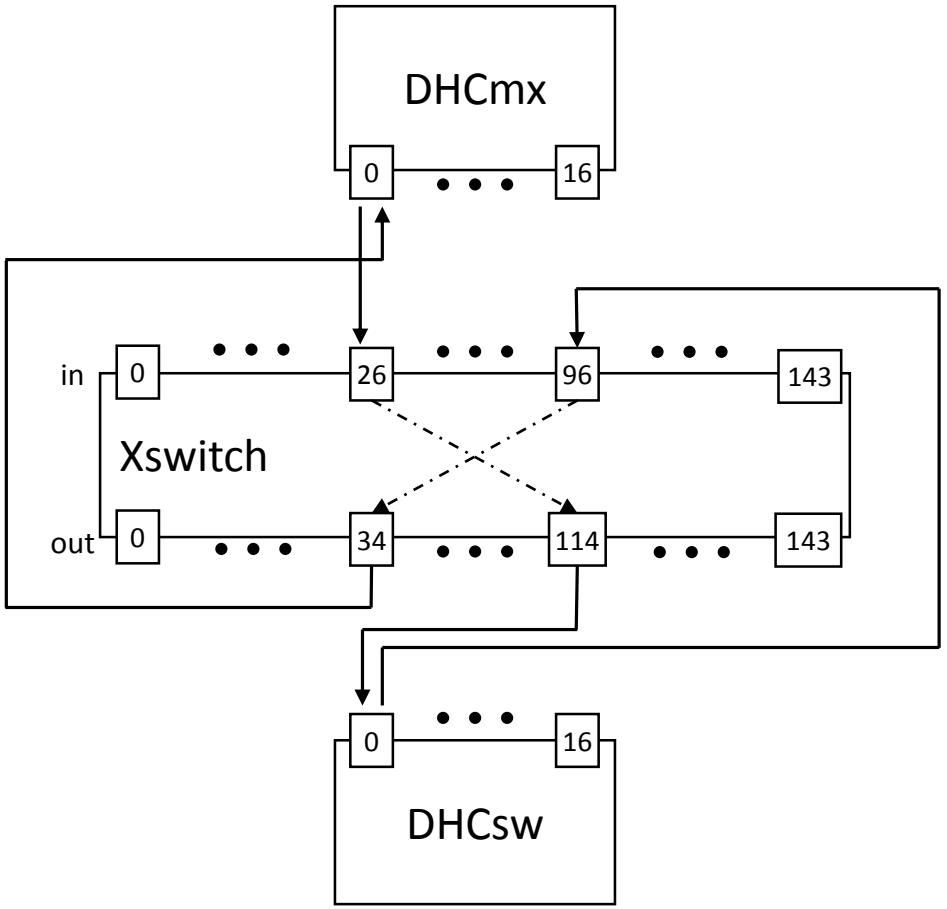

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Performance during 2018

- First installation attempt in April failed due to wrong mapping
- Step-by-step installation starting from June
- Incidents during run: 2 (over 5.5 months)
  - Wrong powering procedure during start-up after power cut led to failing programming of interconnections => Bug fixed in software
  - One “unknown” failure => Fixed by reset of the X-switch, not reproducible in the Lab, did not repete

Xswitch – Spare Situation

- 2 working modules in Munich
- 1 module broken (damage caused by water)
- VSC3144 module discontinued by manufacturer

  => alternatives for future modules by MACOM:

Part Nmb	Max Data Rate	Switch Matrix	Unit Price [$]
M21601G-12	12.5 Gbps	120x120	897.44
M21605G-12	12.5 Gbps	160x160	1217.95

- Fully non-blocking array crosspoint switch
- Four integrated temperature sensors with programmable alarm
- JTAG boundary scan
- Programmable input equalization to compensate for up to 27 dB of loss at 6.25 GHz
- Low latency, less than 2 ns